# HIGH SPEED DATA PRODUCTS

## IC Handbook

PLESSEY
Semiconductors

# Foreword

Plessey Semiconductors has long been recognised as a leading source of high speed data conversion ICs. Our renowned **SP9600** series comparators led to the development of 4-bit and 6-bit ADCs capable of conversion rates in excess of 100MHz. Alongside these the award-winning **SP9768** 150MHz 8-bit DAC set the scene for the 10-bit **SP9770** and the even faster **SP97618** 250MHz 8-bit Graphics DAC.

There are four new ADCs all offering 8-bit resolution with conversion rates ranging from the 20MHz **SP94308** Video System ADC through to the flagship **SP97508** which guarantees 100MHz operation. We are also launching video speed CMOS DACs with graphics controls and a stunning 450MHz 8-bit DAC which is ideal for waveform synthesis and frequency-agile communication systems. Perhaps most impressive of all is a range of subnanosecond comparators in dual, quad and octal configurations, all featuring glitch capture and adjustable hysteresis. And supporting this rapidly growing range of data conversion products are the recently introduced **SL9999** ADC driver and now the **SP92701** 700MHz line receiver/driver.

The range of **64 word** FIFOs now provides for both cascade and standalone requirements with a range of guaranteed operating frequencies from 10MHz to 35MHz.

Three **1K word** by 9-bit FIFOs are being introduced: the **MV61901** offers pin and function compatibility with existing industry standard parts while the **MV61902** and **MV61903** provide tremendous applications advantages with the programmable flag (DIPSTICK) and PARITY features. The DIPSTICK FIFO allows users to design programmable delay lines with just a single AND gate while the PARITY FIFO offers parity checking and generation circuits that give value for money in their own right.

The 50MBit Fibre Optic circuits are generating interest worldwide especially since the Manchester encoding/decoding techniques employed ensure clock and data integrity. Not content with this Plessey Semiconductors now have available samples of three 200MBit chips: an LED driver **(SP9954)**, Transimpedance Amplifier **(SL9904)** and a Dataslice **(SP9944)**.

# Contents

# Product index - Data communications

## Data Control and Automation

| Type | Function | Frequency | Supply Voltage | Process | Page |
|---|---|---|---|---|---|
| **MV6001**[1] | HDLC/DMA controller (e.g. for ISDN) | 128Kbits/s (data), 8MHz (DMA) | 5V | CMOS | 17 |
| **MV6101** | Dual quadrature counter | 10MHz | 5V | CMOS | 26 |

1. Manufactured under licence from British Telecom

## Fibre Optics/LAN/High Speed Serial Data

| Type | Function | Frequency | Supply Voltage | Process | Page |
|---|---|---|---|---|---|
| **SP9960** | Encoder/LED driver | 50M bit | +5V or -5.2V | Bipolar | 29 |
| **SL9901** | Trans-impedance amplifier | 50MHz | +5V or -5.2V | Bipolar | 34 |
| **SP9920** | Manchester decoder with idle code detect | 50M bit | +5V or -5.2V | Bipolar | 36 |
| **SP9921** | Manchester biphase-mark decoder | 5M bit | +5V or -5.2V | Bipolar | 39 |

# Product index - Data conversion

## Analog to Digital converters

| Type | Function | Guaranteed Minimum Clock Rate | Process | Page |
|---|---|---|---|---|
| **SP97508** | 8-bit flash ADC | 110MHz | Bipolar | 45 |
| **SP97308E** | 8-bit flash ADC, ECL outputs | 30MHz | Bipolar | 51 |
| **SP97308T** | 8-bit flash ADC, TTL/CMOS outputs | 30MHz | Bipolar | 54 |
| **SP94308** | 8-bit video system ADC | 20MHz | Bipolar | 58 |
| **SP9756**[1] | 6-bit wide input bandwidth ADC (250MHz - 3dB) | 110MHz | Bipolar | 64 |
| **SP9754** | 4-bit expandable ADC | 110MHz | Bipolar | 70 |

1. 6- and 8-bit accurate versions available

## Digital to Analog Converters

| Type | Function | Guaranteed Minimum Clock Rate | DAC Max Rise Time (10 % - 90 %) | Process | Page |
|---|---|---|---|---|---|
| **SP98608** | 8-bit multiplying DAC | 450MHz | 800ps | Bipolar | 75 |
| **MV95408** | 8-bit video DAC | 50MHz | 5.5ns | CMOS | 80 |
| **SP97618C** | 8-bit graphics DAC | 200MHz | 1.1ns | Bipolar | 84 |
| **SP9768** | 8-bit multiplying DAC | 100MHz | 2.0ns | Bipolar | 90 |
| **SP9770** | 10-bit multiplying DAC | 50MHz | 3.0ns | Bipolar | 94 |

# Product index - Data conversion (contd.)

## Comparators

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **SP93808**[1] | Octal comparator | 10V | ±4V | ±5mV | 950ps | 150ps (typ) | Bipolar | 98 |
| **SP93804**[1] | Quad comparator | 10V | ±4V | ±5mV | 950ps | 150ps (typ) | Bipolar | 107 |
| **SP93802**[1] | Dual comparator | 10V | ±4V | ±5mV | 950ps | 150ps (typ) | Bipolar | 116 |
| **SP9687** | Dual comparator | +5V,-5.2V | ±2.5V | 5mV | 3ns | 1ns (min) | Bipolar | 125 |
| **SP9685** | Single comparator | +5V,-5.2V | ±2.5V | 5mV | 3ns | 1ns (min) | Bipolar | 130 |
| **SP9680** | Single comparator | +5V,-5.2V | ±2.5V | 6mV | 4ns | - | Bipolar | 135 |

1. Adjustable hysteresis, Glitch capture

## Support

| | | | | |
|---|---|---|---|---|
| **SP92701** | Single subnanosecond ECL line receiver and driver | -5.2V | Bipolar | 137 |
| **SL9999** | 400MHz ADC driver operational amplifier | +9V to +15V/ -5V to -15V | Bipolar | 140 |

# Product index – Specialised memory products

## First In/First Out Memories

| Type | Function | Max. Clock Frequency | Supply Voltage | Process | Page |
|---|---|---|---|---|---|
| **MJ2812** | 32 x 8-bit cascadable FIFO | 2MHz | 5V | NMOS[1,2] | 151 |
| **MJ2812HS** | 32 x 8-bit cascadable FIFO | 5MHz | 5V | NMOS[1,2] | 156 |
| **MJ2813** | 32 x 9-bit cascadable FIFO | 2MHz | 5V | NMOS[1,2] | 151 |
| **MJ2841** | 64 x 4-bit cascadable FIFO | 1.75MHz | 5V | NMOS[1,2] | 161 |
| **MV66030-25**[3] | 64 x 9-bit cascadable FIFO | 25MHz | 5V | CMOS[1] | 164 |
| **MV66030-10**[3] | 64 x 9-bit cascadable FIFO | 10MHz | 5V | CMOS[1] | 164 |
| **MV65030-35**[3] | 64 x 9-bit standalone FIFO | 35MHz | 5V | CMOS[1] | 171 |
| **MV65030-25**[3] | 64 x 9-bit standalone FIFO | 25MHz | 5V | CMOS[1] | 171 |
| **MV66401-25** | 64 x 4-bit cascadable FIFO | 25MHz | 5V | CMOS[1] | 177 |
| **MV66401-10** | 64 x 4-bit cascadable FIFO | 10MHz | 5V | CMOS[1] | 177 |
| **MV65401-35** | 64 x 4-bit standalone FIFO | 35MHz | 5V | CMOS[1] | 184 |
| **MV65401-25** | 64 x 4-bit standalone FIFO | 25MHz | 5V | CMOS[1] | 184 |
| **MV66402-25** | 64 x 5-bit cascadable FIFO | 25MHz | 5V | CMOS[1] | 177 |
| **MV66402-10** | 64 x 5-bit cascadable FIFO | 10MHz | 5V | CMOS[1] | 177 |
| **MV65402-35** | 64 x 5-bit standalone FIFO | 35MHz | 5V | CMOS[1] | 184 |
| **MV65402-25** | 64 x 5-bit standalone FIFO | 25MHz | 5V | CMOS[1] | 184 |
| **MV66403-25**[3] | 64 x 4-bit cascadable FIFO | 25MHz | 5V | CMOS[1] | 177 |
| **MV66403-10**[3] | 64 x 4-bit cascadable FIFO | 10MHz | 5V | CMOS[1] | 177 |
| **MV65403-35**[3] | 64 x 4-bit standalone FIFO | 35MHz | 5V | CMOS[1] | 184 |
| **MV65403-25**[3] | 64 x 4-bit standalone FIFO | 25MHz | 5V | CMOS[1] | 184 |
| **MV66404-25**[3] | 64 x 5-bit cascadable FIFO | 25MHz | 5V | CMOS[1] | 177 |
| **MV66404-10**[3] | 64 x 5-bit cascadable FIFO | 10MHz | 5V | CMOS[1] | 177 |
| **MV65404-35**[3] | 64 x 5-bit standalone FIFO | 35MHz | 5V | CMOS[1] | 184 |
| **MV65404-25**[3] | 64 x 5-bit standalone FIFO | 25MHz | 5V | CMOS[1] | 184 |
| **MV61901-50** | 1K x 9-bit cascadable FIFO | 50ns (access) | 5V | CMOS[1] | 190 |
| **MV61901-80** | 1K x 9-bit cascadable FIFO | 80ns (access) | 5V | CMOS[1] | 190 |
| **MV61901-120** | 1K x 9-bit cascadable FIFO | 120ns (access) | 5V | CMOS[1] | 190 |
| **MV61902** | 1K x 9-bit 'Dipstick' FIFO | 10MHz | 5V | CMOS[1] | 201 |
| **MV61903** | 1K x 9-bit 'Parity' FIFO | 10MHz | 5V | CMOS[1] | 210 |

1. TTL compatible 2. CMOS compatible 3. With output enable

## Memory Support

| Type | Function | Supply Voltage | Process | Page |
|---|---|---|---|---|
| **SP9001C** | 4-channel magnetic bubble memory sense amplifier | ±5V | Bipolar | 218 |

# Product index - High speed logic

## Very Fast ECL

| | | | | |
|---|---|---|---|---|
| **SP9131** | Dual D-type flip-flop (ultra-fast version of MC10131) | -5.2V | 520MHz | 227 |
| **SP9210** | 8-bit latch (dual 4) | -5.2V | 200MHz | 231 |
| **SP16F60** | Dual 4-I/P OR/NOR gate (pin/function compatible with MC1660 | -5.2V | 0.55ns | 235 |

## Standard ECL III

| | | | | | |
|---|---|---|---|---|---|
| **SP1648** | Voltage controlled oscillator | +5V or -5.2V | 225MHz | 150mW | 237 |
| **SP1650** | Dual A/D comparator | +5V and -5.2V | 3.5ns | 330mW | 243 |
| **SP1658** | Voltage controlled multivibrator | -5.2V | 155MHz | 130mW | 252 |
| **SP1660** | Dual 4-I/P OR/NOR gate | -5.2V | 1ns | 120mW | 256 |
| **SP1662** | Quad 2-I/P NOR gate | -5.2V | 1ns | 300mW | 258 |
| **SP1664** | Quad 2-I/P OR gate | -5.2V | 1ns | 300mW | 261 |
| **SP1670** | D-type flip-flop | -5.2V | 300MHz | 250mW | 264 |
| **SP1692** | Quad line receiver | -5.2V | 1.1ns | 220mW | 270 |

# Product List – alpha numeric

# Semi-Custom design

For more than a decade Plessey Semiconductors has led and consistently advanced the state of the art in semi-custom technology.

This leadership has been based on the use of comprehensive design software, Plessey Design System (PDS). PDS is independent of both technology and function in that Gate Arrays and cell based designs using CMOS or Bipolar can be developed.

PDS is supported on a DEC *VAX (VMS) based system. However, Plessey supports Daisy, Valid and Mentor workstations, which are all interfaced into PDS, thereby offering an easy design route to meet your needs and costs.

These support routes offer the user the maximum flexibility in their design. However, Plessey also offers a 'turnkey' design function where we will complete the design from start to finish.

We offer a complete range of CMOS and Bipolar processes to meet all requirements of speed, power, packing density and cost and a very comprehensive range of through-hole, surface mount and pin grid array packages.

## Gate Array Families

Plessey offers a complete range of Gate Array families, in both CMOS and ECL, for cost-effective, fast turn-round projects - see tables below.

### CLA 3000 SERIES (CMOS)

- Double layer metal
- 4 micron channel length
- 2.8ns typ. gate delay
- 20MHz system clock
- Fully auto-routed
- 3V to 6V power supply
- Static protected I/O
- Military screening
- >90 % utilization of gates

**PRODUCT FAMILY:**

| | Gates | I/O | Power |
|---|---|---|---|
| **CLA31XX** | 840 | 40 | 4 |
| **CLA33XX** | 1440 | 52 | 4 |
| **CLA35XX** | 2400 | 64 | 4 |

### CLA 5000 SERIES (CMOS)

- Double layer metal
- 2 micron channel length
- 1.2ns typ. gate delay
- 40MHz system clock rate
- Fully auto-routed
- 3V to 6V power supply
- Static protected I/O
- Military screening
- >90% utilization of gates

**PRODUCT FAMILY:**

| | Gates | I/O | Power |
|---|---|---|---|
| **CLA51XX** | 640 | 36 | 4 |
| **CLA52XX** | 1232 | 48 | 8 |
| **CLA53XX** | 2016 | 64 | 8 |
| **CLA54XX** | 3060 | 80 | 8 |
| **CLA55XX** | 4408 | 96 | 16 |
| **CLA56XX** | 5984 | 112 | 16 |
| **CLA57XX** | 7104 | 128 | 16 |
| **CLA58XX** | 8064 | 144 | 16 |
| **CLA59XX** | 10044 | 160 | 16 |

### ELA 60000 (ECL)

- High performance: 1GHz
- 180ps typ. gate speed
- ECL 10K, ECL 100K, TTL and
- CMOS compatible
- Programmable speed/power
- Full military operation

**PRODUCT FAMILY:**

| | Gates | Pads |
|---|---|---|
| **ELA61000** | 660 | 48 |
| **ELA62000** | 1400 | 68 |
| **ELA63000** | 2900 | 96 |
| **ELA65000** | 4500 | 120 |

# Plessey MEGACELL

PLESSEY MEGACELL offers the ASIC designer the opportunity to move to VHSIC gate complexities without losing the simplicity of gate array design methods. MEGACELL also offers design freedom and product innovation through creative design.

## Cell Library

Four types of library elements are available giving functional, dynamic, and physical design flexibility:

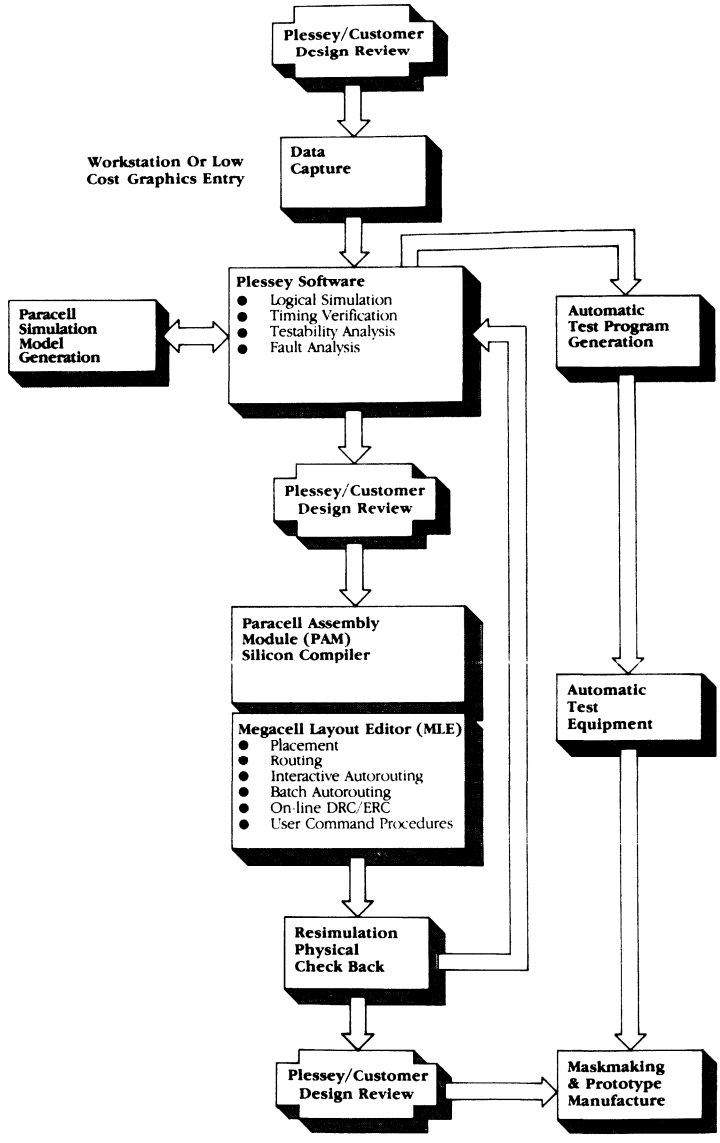
**Microcells** are modular size cells of simple logic functions (gates and flip-flops) similar to those in current standard logic families.

**Macrocells** comprise a user-library of building-blocks (e.g. 74 Series TTL) compiled from Microcells to speed up design entry.

**Paracells** are cells which can be parameterised through their regular composition (e.g. ROM, RAM, PLA). The simple netlist cell code is auto-compiled into a physical entity requiring very little design effort for these types of cells.

**Supracells** are large fixed-function cells pre-designed to replicate or improve existing VLSI standard functions. Many standard products can be incorporated into the Supracell concept.

## Design Route

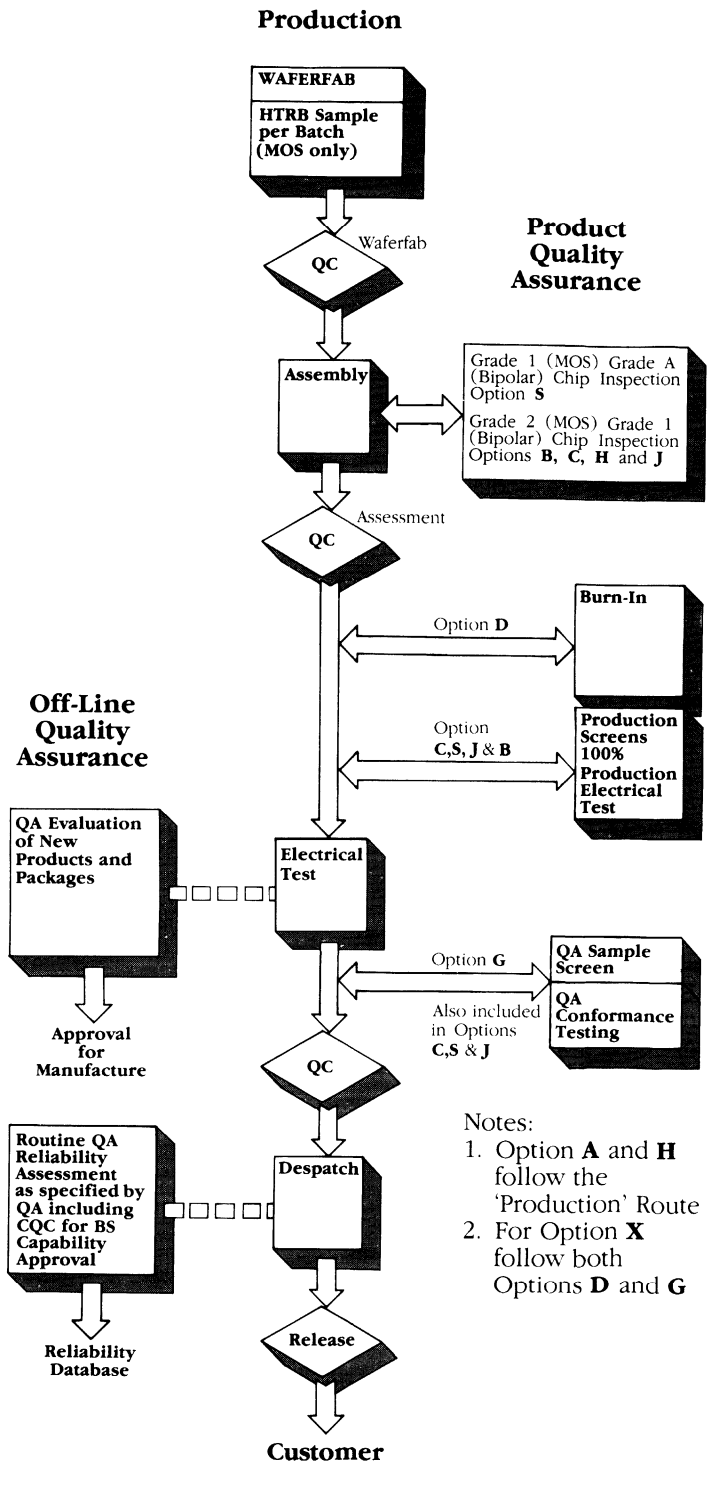


# The Quality Concept

Plessey Semiconductors makes MOS and bipolar integrated circuits of various types for commercial, professional and military customers. However, a single common management system is used to control the manufacturing processes which is planned to meet the requirements of **BS9000** and **DEF-STAN 05-21**. Plessey Semiconductors can supply product meeting the requirements of **MIL-STD-883C**.

This means that all products benefit from the use of reliable processes with strict controls of individual stages and overall quality control. Where customers require even higher quality grades this is achieved by additional screening and testing but all grades are produced on the same manufacturing processes operating under consistent control systems.

At Plessey Semiconductors, quality and reliability are built into the product by rigorous control of all processing operations and by minimizing random defects. Process management involves extensive documentation of procedures, recording of batch data, employment of extensive traceability procedures and the provision of appropriate equipment and facilities.




Notes:
1. Option **A** and **H** follow the 'Production' Route
2. For Option **X** follow both Options **D** and **G**

## Screening Options

Plessey Semiconductors currently offers integrated circuits screened to any of nine options. The ways in which these options are exercised during the manufacturing cycle are shown in the Reliability Assessment Flow diagram opposite.

OPTION A. **Standard Plessey Product.** The devices are 100% electrically tested and have 100% physical inspection applied prior to despatch. AQL for electrical tests is as low as 0.1% on volume product. AQL for physical inspection is 0.4%.

OPTION B is **Plessey Hi-Rel Level B** screening. This involves 100% screening, including 160 hour burn-in (ref. 446/SQ/05742, Issue 1).

OPTION C is the **MIL-STD-883C Class B.** This involves screening, including burn-in, 100 ¼ hot and cold testing plus Groups A, B, C and D Conformance testing.

OPTION D (MOS only) is as for Standard Plessey Product but with 100% static burn-in. 20 hours, 125°C, maximum operating voltage.

OPTION G (MOS only) is a conformance (lot-by-lot) assessment using the methods of **BS9400**. This gives customer assurance that every batch has been assessed by QA. The **BS6001** sampling plan is used with the AQL level from BS9400 (no BS detail specification involved).

OPTION H is **STACK 0001**, which embodies the purchasing recommendations of a leading group of telecommunications equipment manufacturers.

OPTION J (MOS only) is a **BS9450 Assessment Level S2** capability, for which we are currently seeking approval. This specification is recommended for devices destined for applications where the system will be highly stressed, both electrically and physically, or where repair would be difficult.

OPTION S is a **MIL-STD-883C Class S** requirement for space applications, submarine repeaters and satellites where repairs, if not impossible would be extremely difficult and expensive. This involves even more comprehensive screening than Class B and more onerous lot conformance testing.

OPTION X (MOS only) is the same as Option G with regard to lot-by-lot conformance but carried out in conjunction with Option D.

# Technical Data

## 1. Data communications

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PRELIMINARY INFORMATION

# MV6001

## HDLC/DMA CONTROLLER

The MV6001 is a combined HDLC transceiver and DMA controller capable of providing serial communications at rates up to 128K bits/second, and handling direct memory access clock rates up to 8MHz.

### FEATURES

- Data Rates up to 128K Bits/s
- DMA Rate up to 8MHz
- Low Power CMOS
- Simple Interfacing to Popular 8-Bit Processors
- Frame Length up to 2K Bytes
- Low Host-Processor Overhead
- Conforms to ECMA40 and Related Standards (CCITT X.25, X.75, I.440, ISO3309, ANSI X3.66, FED-STD 1003, FIPS71)

### APPLICATIONS

- ISDN Terminals
- LANs
- X25 p.s.s. Networks

### ORDERING INFORMATION

**MV6001 B0 DP** (Commercial Plastic DIP)
**MV6001 B0 DG** (Commercial Ceramic DIP)

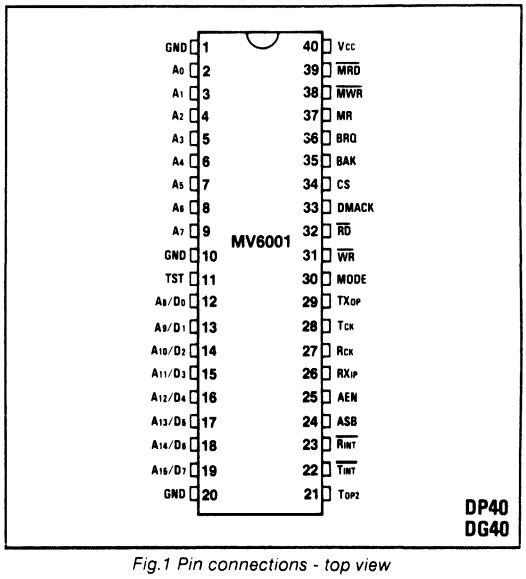



*Fig.1 Pin connections - top view*

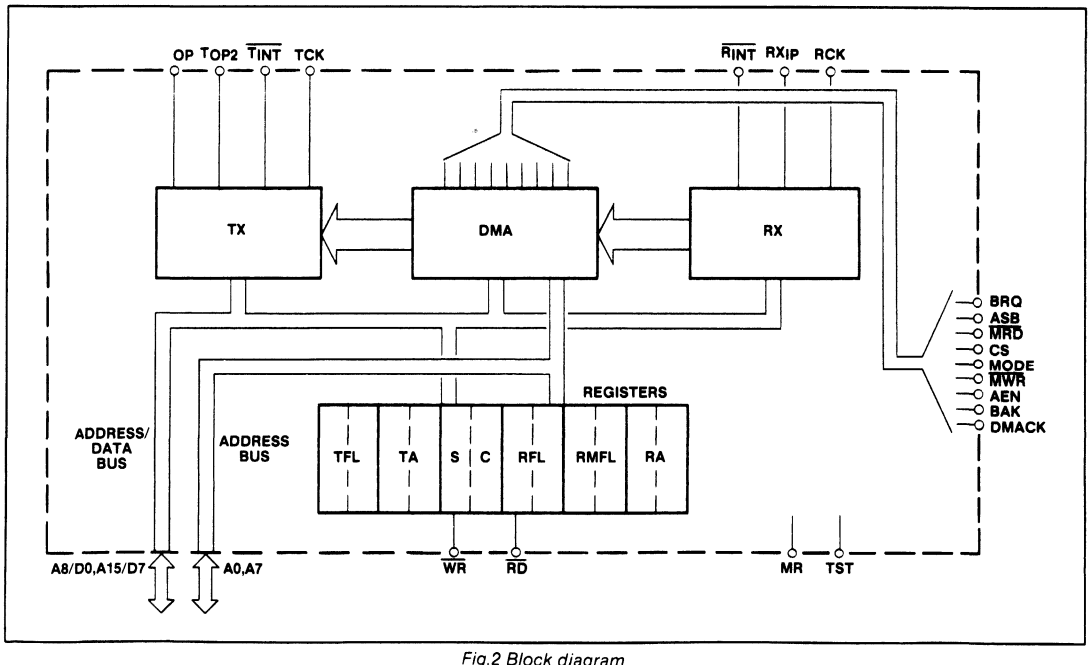
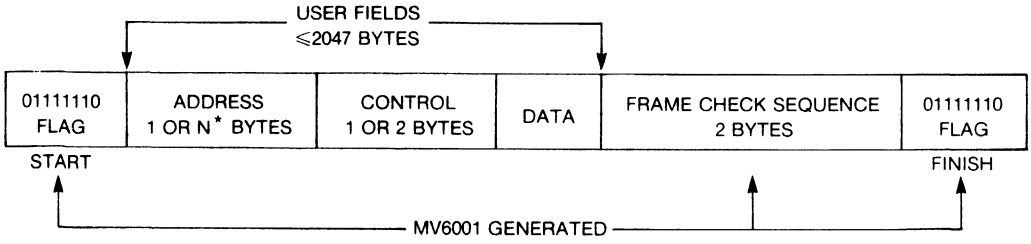



*Fig.2 Block diagram*

## PIN DESCRIPTION

| Pin No. | Name | I/O | Function |
|---|---|---|---|
| 1,10,20 | GND | | **0V supply.** All 3 pins must be connected. |
| 2 - 9 | $A_0$ - $A_7$ | I/O | **Address Bus.** Output for memory $A_0$ - $A_7$ addressing. Input for register addresses $A_0$ - $A_3$. |
| 11 | TST | I | **Test Enable.** Tie to GND for normal operation. |
| 12 - 19 | $A_8/D_0$ - $A_{15}/D_7$ | I/O | **Data Bus/High Order Address.** Multiplexed data and address bus. |
| 21 | $TOP_2$ | O | **Transmitter Out.** Alternative output to $TX_{OP}$. This output is not affected by loop back (see Operating Notes - LOOPBACK). |
| 22 | $\overline{T_{INT}}$ | O | **Transmitter Interrupt.** An interrupt is generated whenever transmission of a frame is ended, either following the last FCS byte of a complete frame of when an abort sequence is transmitted. The interrupt is reset by the control register. |
| 23 | $\overline{R_{INT}}$ | O | **Receiver Interrupt.** An interrupt is generated whenever a frame is received. The interrupt is reset by the counter register. |
| 24 | ASB | O | **Address Strobe.** Strobes the Address High byte from the Data/Address Bus into an external latch. |
| 25 | AEN | O | **Address Enable.** Enables the external address latch. |
| 26 | $RX_{IP}$ | I | **Receiver Input.** Serial HDLC data input, clocked in by RCK. |
| 27 | RCK | I | **Receiver Data Clock.** Provides clock to the receiver section, frequency should be at the required data rate, this need not necessarily the the same as the transmit data rate. |
| 28 | TCK | I | **Transmitter Data Clock.** This input provides a clock signal for the transmitter section and should be set to the desired transmit data rate. |
| 29 | $TX_{OP}$ | O | **Transmitter output.** Main transmitter output for serial data. |
| 30 | MODE | I | **Bus Control Mode Select.** Controls the polarity of BAK and BRQ. MODE = $V_{CC}$ gives active LOW, MODE = GND gives active HIGH. |
| 31 | $\overline{WR}$ | I | **Write Register.** Loads data from data bus into register addressed by $A_0$ - $A_3$. |
| 32 | $\overline{RD}$ | I | **Read Register.** Reads addressed register onto data bus. |
| 33 | DMACK | I | **DMA Clock.** This input provides clock to the DMA section. The DMA clock rate should be at least ten times the sum of the transmit and receive data rates. |
| 34 | CS | I | **Chip Select.** Enables $\overline{RD}$ and $\overline{WR}$ inputs. |
| 35 | BAK | I | **Bus Acknowledge.** Input from processor relinquishing control of bus. See pin 30, Bus Mode Select. |
| 36 | BRQ | O | **Bus Request.** Output to processor requesting the bus for a DMA cycle. See pin 30, Bus Mode Select. |
| 37 | MR | I | **Master Reset.** Resets everything. |
| 38 | $\overline{MWR}$ | O | **Memory Write.** This is a three-state output to write data into memory during DMA cycles. |
| 39 | $\overline{MRD}$ | O | **Memory Read.** 3-state output to read data from memory during DMA cycles. |
| 40 | $V_{CC}$ | | +5V ± 10% supply. |

## HDLC FRAME CONSTRUCTION




*N is any integer

*Fig.3*

Fig.3 shows the construction of an HDLC frame. The start and finish of the frame are determined by FLAGS (the binary pattern 01111110). To prevent spurious recognition of flags in the user fields, the transmitter automatically inserts a '0' after five successive '1's. The inserted '0's are removed by the receiver, and hence are not seen by the user. Each HDLC frame contains a 2 byte frame check sequence produced by a cyclic redundancy generator in the transmitter. This sequence is checked by the receiver to validate the frame.

There are two other sequences which have specific meanings - IDLE and ABORT. The IDLE state is the transmission of at least 15 continuous '1's without inserted zeros. ABORT is 7 to 14 consecutive '1's without inserted zeros sandwiched between two zeros.

## FUNCTIONAL DESCRIPTION

The MV6001 consists of four main sections; transmitter, receiver, DMA unit and register bank. Each of the transmitter, receiver and DMA unit have their own clocks running at the required data rates. There are no restrictions on the relative timing between transmit and receive clocks, the DMA clock rate should be greater than ten times the sum of the transmit and receive clock rates.

### Transmission

In its steady state the transmitter produces a continuous stream of FLAGS until the control register is loaded with a transmit instruction. The transmitter then, at intervals, requests the DMA unit to fetch a byte of data. This is then transferred from the system memory via the data bus to the transmitter. (If the DMA unit should fail to fetch a byte of data by the time the next request arrives then an under-run will occur and the transmitter will transmit an ABORT sequence). Data is converted into a serial stream with inserted zeros after five ones, and the 16-bit frame check sequence is appended at the end of each frame. As soon as the last bit of the FCS has been clocked out, the $\overline{T_{INT}}$ output goes low to inform the processor that transmission has ended.

## INITIALISATION

To start transmission, two items of information are required - the start address for the data to be transmitted, and the length of the user fields are loaded into the TA and TFL registers respectively, after which the transmit enable bit ($D_0$) can be set at any time to start transmission. Once a transmission has been started, the only way it can by stopped is to set the abort bit ($D_1$). The transmitter will then transmit the abort sequence followed by flags. Transmitter reset ($D_2$) resets the transmitter interrupt $\overline{T_{INT}}$, clears the TA and TFL registers and bits $D_0$ and $D_1$ of the status register. Transmitter reset is disabled during a transmission.

### Interrupt

A transmitter interrupt ($\overline{T_{INT}}$) is generated whenever a transmission ceases, the status register can then be read to check if the frame was aborted or not. The interrupt is reset by writing a transmitter reset to the control register. NB. The status register must be read before a transmitter reset as this will alter the contents of the status register.

### Status

The transmitter has two status bits - transmitting data ($D_0$) and abort ($D_1$). The transmitting data bit should always be low after $\overline{T_{INT}}$ signifying that transmission is ended. The abort bit will be high whenever a frame is aborted either by an abort instruction to the control register, or internally due to an under-run.

### Reception

The receiver accepts serial data, removes inserted zeros and checks the frame check sequence. For each byte of data received, the receiver section generates a DMA request to transfer the data to memory. If the DMA controller fails to make the transfer before the next request from the receiver, then the receiver will drop out and give a receiver interrupt with the code in the status register for overrun. If the number of bytes received reaches the number in the receive maximum frame length register the receiver will drop out and give an interrupt with the code in the status register for frame too long.

### Initialisation

The RA register (2 bytes) is loaded with the address where the first received byte of data is to be stored. The RMFL register (11 bits) is loaded with the maximum number of bytes in the user fields plus 3 bytes ( +2 bytes for the FCS, +1 byte because an interrupt will occur when the frame length is equal to the length set by the number in the register).

### Control

The receiver has two control bits in the control register, receive enable ($D_3$) and receive reset ($D_4$). Once the RA and RMFL registers have been loaded, the receive enable bit can be set at any time to allow the receiver to receive a frame. Once set, the receive enable bit cannot be overwritten and receive reset is disabled until a frame has been received.

Receiver reset will reset the $R_{INT}$ interrupt bit, registers RFL, RMFL, RA and bits $D_2$ - $D_7$ of the status register.

### Interrupt

A receive interrupt ($\overline{R_{INT}}$) is generated whenever a frame is received. The status register can then be read to check the status of the received frame. The interrupt is reset by writing a receiver reset to the control register. Since the reset will clear the receiver bits in the status register, the register must be read before writing the reset to the control register.

### Status

The receiver uses bits $D_2$ - $D_7$ of the status register (see Figs. 5 and 6). A valid frame is indicated by both 'overrun' ($D_6$) and 'frame too long' ($D_7$) bits being high. Following $\overline{R_{INT}}$ the 'free to receive' bit ($D_2$) should be low, indicating that a frame has been received. The abort, overrun and long frame bits will be set according to the state of the frame received. The flag ($D_4$) and idle ($D_3$) bits monitor the incoming signal continuously even when the receiver is disabled.

### Frame Length Register

Having received a frame and read the status register, the received frame length can be read from the RFL register. The frame length is given as an eleven bit number and includes the 2 FCS bytes in the count. The register should be read before a receiver reset.

### Loopback

Bit $D_7$ of the control register, the loopback bit is provided for testing purposes. When the bit is set high an internal connection is made between the transmitter output and receiver input. The main transmitter output ($TX_{OP}$) transmits IDLE (transmitted data is always available on $T_{OP2}$). The receiver is clocked from TCK. The loopback bit will respond to every write to the control register.

### Direct Memory Access (Fig.11)

All data transfers to or from memory are carried out by the DMA controller. Each time it receives a request from the transmitter or receiver it will carry out one DMA cycle, i.e. only one byte is transferred at a time. Clashes between transmitter and receiver are resolved in favour of the receiver, otherwise operation is on a first come, first served basis.

### Registers

Fig.7 shows the addresses for the various instruction and status registers. All registers are readable from and writable to except for S, C and RFL. The S and C registers have the same address, which one is accessed is determined by whether a read (status) or write (control) operation is carried out. Transmitter registers should not be written to when transmitting (except to ABORT a frame), likewise receiver registers should not be written to when receiving. The TA and RA registers update continuously during transmission and reception respectively, giving the next address to be read from or written to.

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| LOOPBACK ENABLE | DON'T CARE | DON'T CARE | RECEIVE RESET | RECEIVE ENABLE | TRANSMIT RESET | TRANSMIT ABORT | TRANSMIT ENABLE |

*Fig.4 Control register*

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| RECEIVED FRAME TOO LONG | RECEIVED OVERRUN FRAME | RECEIVED ABORT | RECEIVING FLAGS | RECEIVING IDLE | FREE TO RECEIVE | TRANS-MISSION ABORTED | TRANS-MITTING DATA |

RECEIVE BITS — TRANSMIT BITS

*Fig.5 Status register*

| Status Register | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | Condition |
| X | X | X | X | X | X | 0 | 1 | Currently transmitting data |
| X | X | X | X | X | X | 0 | 0 | Transmitter disabled, transmission COMPLETE (status read after an interrupt) |
| X | X | X | X | X | X | 1 | 0 | Transmitter disabled, transmission ABORTED (status read after an interrupt) |
| X | X | X | X | X | 1 | X | X | Receiver enabled, free to receive |
| X | X | X | 0 | 0 | X | X | X | Currently receiving data |
| X | X | X | 0 | 1 | X | X | X | Receiving IDLE |
| X | X | X | 1 | 0 | X | X | X | Receiving FLAGS |
| 0 | 0 | 1 | X | X | 0 | X | X | Receiver disabled, ABORTED frame received (status read after an interrupt) |
| 0 | 1 | 0 | X | X | 0 | X | X | Receiver disabled, OVERRUN frame received (status read after an interrupt) |
| 1 | 0 | 0 | X | X | 0 | X | X | Receiver disabled, TOO LONG frame received (status read after an interrupt) |
| 1 | 1 | 0 | X | X | 0 | X | X | Receiver disabled, VALID frame received (status read after an interrupt) |

*Fig.6 Status conditions*

| Register | Function | Length (Bits) | Address (Hex) | $A_3$ | $A_2$ | $A_1$ | $A_0$ | R/W |
|---|---|---|---|---|---|---|---|---|
| TFL | Transmitter Frame Length LS Byte | 8 | 2 | 0 | 0 | 1 | 0 | R/W |
| | Transmitter Frame Length MS Byte | 3 | 3 | 0 | 0 | 1 | 1 | R/W |
| TA | Transmitter Address LS Byte | 8 | 6 | 0 | 1 | 1 | 0 | R/W |
| | Transmitter Address MS Byte | 8 | 7 | 0 | 1 | 1 | 1 | R/W |
| S | Status | 8 | 9 | 1 | 0 | 0 | 1 | R |
| C | Control | 8 | 9 | 1 | 0 | 0 | 1 | W |
| RFL | Receiver Frame Length LS Byte | 8 | A | 1 | 0 | 1 | 0 | R |
| | Receiver Frame Length MS Byte | 3 | B | 1 | 0 | 1 | 1 | R |
| RMFL | Receiver Maximum Frame Length LS Byte | 8 | C | 1 | 1 | 0 | 0 | R/W |
| | Receiver Maximum Frame Length MS Byte | 3 | D | 1 | 1 | 0 | 1 | R/W |
| RA | Receiver Address LS Byte | 8 | E | 1 | 1 | 1 | 0 | R/W |
| | Receiver Address MS Byte | 8 | F | 1 | 1 | 1 | 1 | R/W |

*Fig.7 Register addresses*

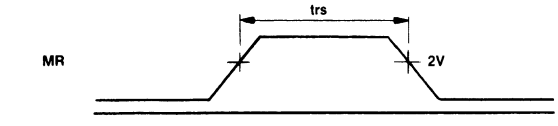



Fig.8(a)

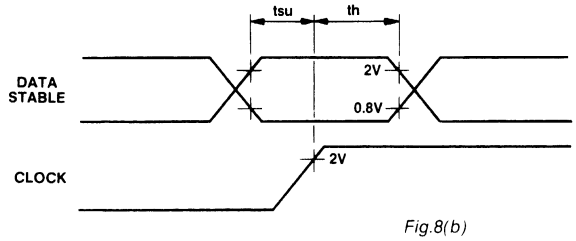



Fig.8(b)

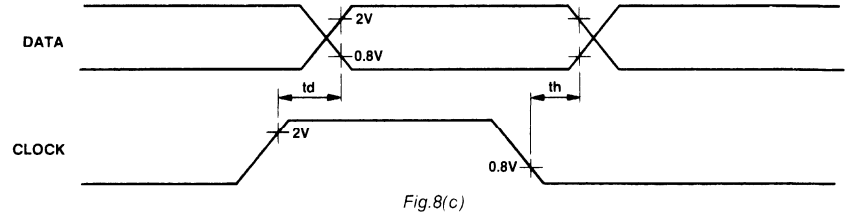



Fig.8(c)

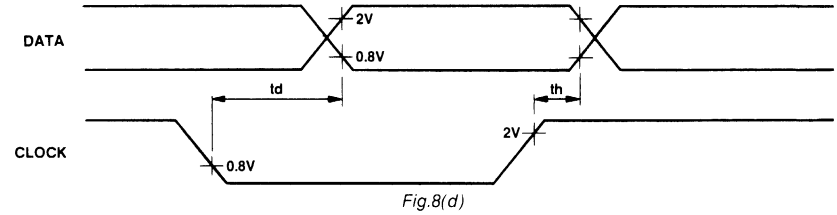



Fig.8(d)

Fig.8 Timing diagram

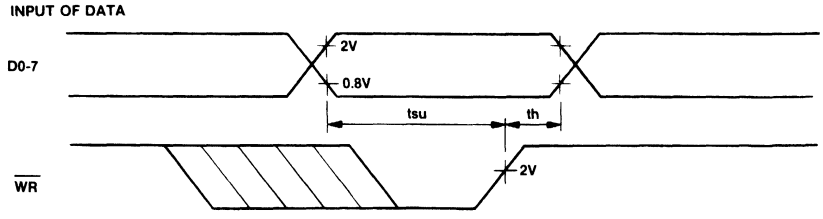



*Fig.9(a)*

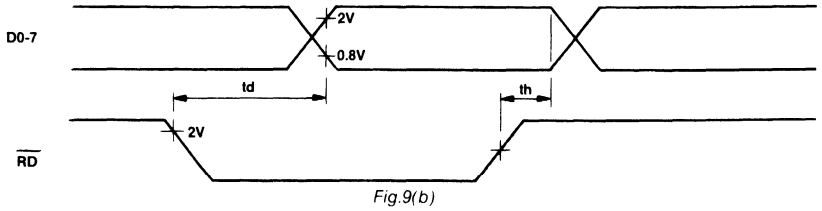



*Fig.9(b)*

*Fig.9 Register timing*

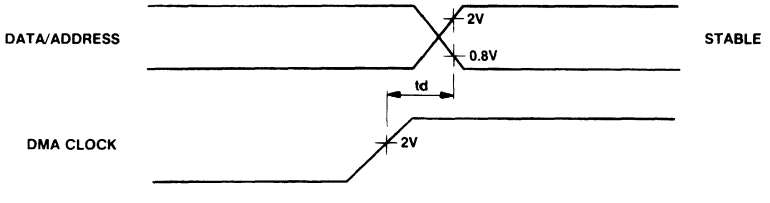



*Fig.10 DMA timing*

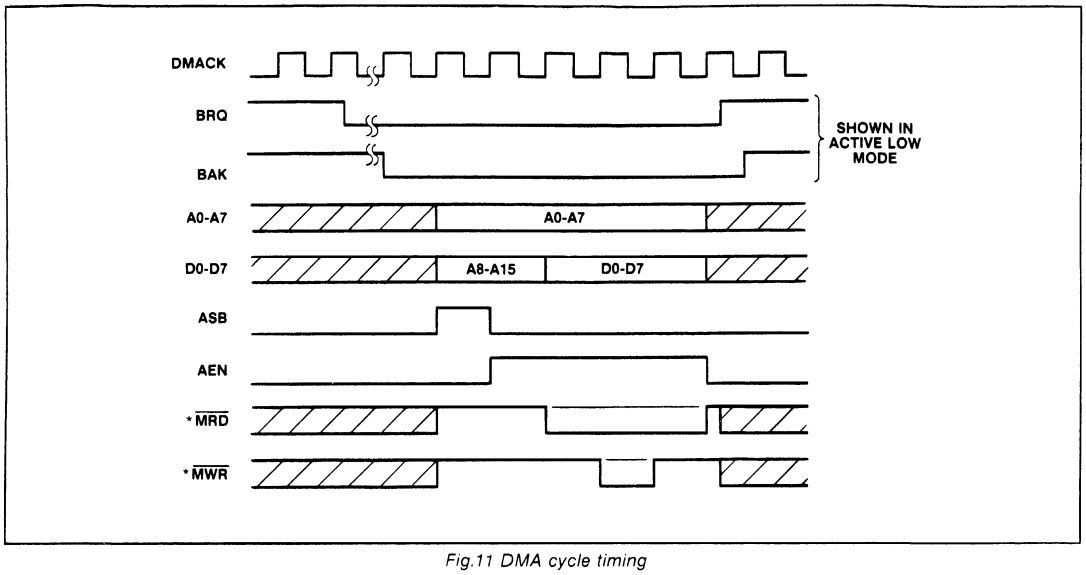



*Fig.11 DMA cycle timing*

* During a read cycle, $\overline{MWR}$ stays high and similarly during a write cycle $\overline{MRD}$ stays high. All other external signals are the same for both cycles.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.3V to 7.0V |
| Input voltage $V_{IN}$ | -0.3V to $V_{CC}$ +0.3V |
| Output voltage $V_{OUT}$ | -0.3V to $V_{CC}$ +0.3V |
| Clamp diode current per pin $I_K$ (See Note 2) | ±18mA |
| Static discharge voltage | |
| Storage temperature $T_S$ | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -40°C to +85°C |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 10%, Ground = 0V

### Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output high voltage | $V_{OH}$ | $V_{CC}$-2 | | | V | $I_{OH}$ = 0.8mA |
| Output low voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6mA |
| Input high voltage | $V_{IH}$ | 2.2 | | | V | |
| Input low voltage | $V_{IL}$ | | | 0.8 | V | |
| Input leakage current | $I_L$ | -10 | | +10 | μA | GND ≤ $V_{IN}$ ≤ $V_{CC}$ |
| $V_{CC}$ current | $I_{CC}$ | | | 1 | mA | $T_{amb}$ = -40°C to +85°C |
| Output leakage current | $I_{OZ}$ | -50 | | +50 | μA | GND ≤ $V_{OUT}$ ≤ $V_{CC}$ |
| Output S/C current | $I_{OS}$ | 15 | | 80 | mA | $V_{CC}$ = Max |

**Switching Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum DMA clock frequency | FDMACK | 8 | | | MHz | |
| Maximum TX clock frequency | FTCK | 128 | | | kHz | |
| Maximum RX clock frequency | FRCK | 128 | | | kHz | |
| Minimum MR duration | $t_{rs}$ | | | | ns | Fig.8(a) |
| RXIP to RCK set-up time | $t_{su}$ | 0 | | | ns | Fig.8(b) |
| RXIP to RCK hold time | $t_h$ | 90 | | | ns | Fig.8(b) |
| BAK to DMACK set-up time | $t_{su}$ | 0 | | | ns | Fig.8(b) |
| BAK to DMACK hold time | $t_h$ | 25 | | | ns | Fig.8(b) |
| Delay DMA clock to $\overline{MRD}$ | $t_d$ | | 40 | 55 | ns | Fig.8(c) |
| Delay DMA clock to $\overline{MWR}$ | $t_d$ | | 40 | 55 | ns | Fig.8(c) |
| Delay RCK ↓ to $\overline{R_{INT}}$ | $t_d$ | | 50 | 110 | ns | Fig.8(d) |
| Delay, TCK to $\overline{T_{INT}}$ | $t_d$ | | 60 | 90 | ns | Fig.8(c) |
| Delay, TCK ↓ or RCK ↓ to BRQ | $t_d$ | | 70 | 90 | ns | Fig.8(c) & (d) |
| Delay, DMACK to AEN | $t_d$ | | 40 | 55 | ns | Fig.8(c) |
| Delay, DMACK to ASB | $t_d$ | | 40 | 55 | ns | Fig.8(c) |
| Delay, TCK to $TX_{OP}$ | $t_d$ | | 70 | 115 | ns | Fig.8(c) |
| Delay, TCK to $T_{OP2}$ | $t_d$ | | 60 | 115 | ns | Fig.8(c) |
| Hold, DMACK to $\overline{MRD}$ | $t_h$ | | 90 | 130 | ns | Fig.8(d) |
| Hold, DMACK to $\overline{MWR}$ | $t_h$ | | 50 | 75 | ns | Fig.8(d) |
| Hold, DMACK to BRQ | $t_h$ | | 60 | | ns | Fig.8(d) |
| Hold, DMACK to AEN | $t_h$ | | 30 | 55 | ns | Fig.8(d) |
| Hold, DMACK to ASB | $t_h$ | | 40 | 55 | ns | Fig.8(d) |
| Data to WR set-up | $t_{su}$ | | | | ns | Fig.9(a) |
| WR to data hold | $t_h$ | | | | ns | Fig.9(a) |
| RD to data delay | $t_d$ | | 50 | | ns | Fig.9(b) |
| RD to data hold | $t_h$ | | | | ns | Fig.9(b) |
| DMACK to data/address delay | $t_d$ | | 60 | | ns | Fig.10 |

# MV6101

## DUAL QUADRATURE COUNTER

The MV6101 provides interfacing facilities for connecting one or two rotary or linear encoders to a microprocessor bus. The device can be configured as either a 1 x 32- or 2 x 16-bit counter, and is capable of counting in either BCD or binary.

Each channel of the device consists of a direction discriminator, a 16-bit counter, and a 16-bit latch. The outputs from the two latches go to a MUX which feeds an 8-bit bidirectional I/O port. The two counters can be pre-loaded from the I/O port. Direct count mode available for up/down event counting.

### FEATURES

- Complete Interface between Encoder and Microprocessor System — Requires no Additional Logic
- X and Y Axis Interface in One Device
- Low Power CMOS
- 2 x 16 or 1 x 32 Operation
- Capable of Clock Rates up to 10MHz
- Counters can be loaded by Microprocessor
- Marker Pulse Input

### APPLICATIONS

- Rotary and Linear Encoders
- Batch Counting/Flow Metering
- Mouse/Tracker Ball Interface
- Frequency/Rate Measurement
- Robotics/CNC Machines

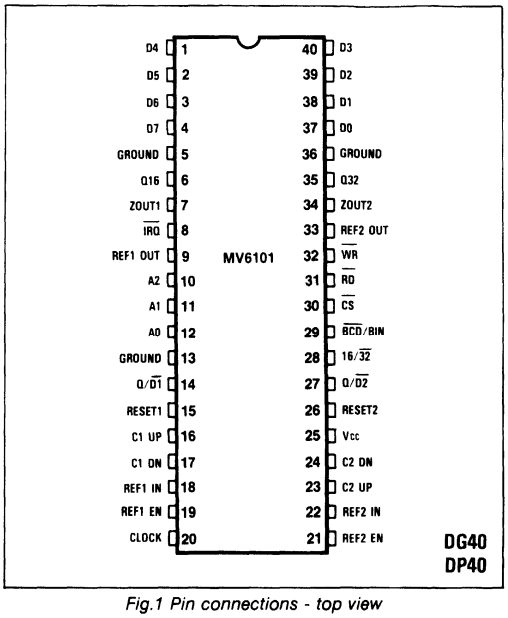



*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**MV6101 B0 DG** (Industrial - Ceramic DIL package)
**MV6101 B0 DP** (Industrial - Plastic DIL package)

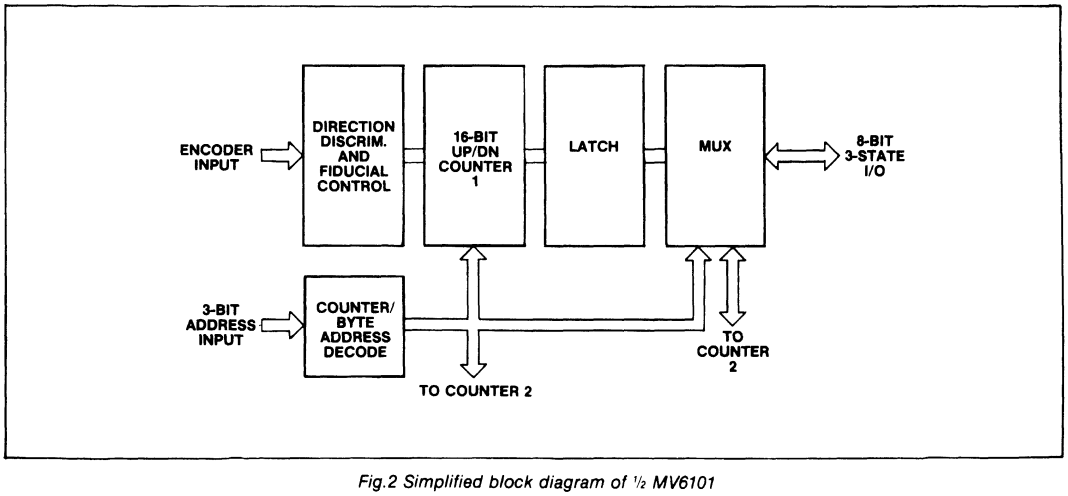



*Fig.2 Simplified block diagram of ½ MV6101*

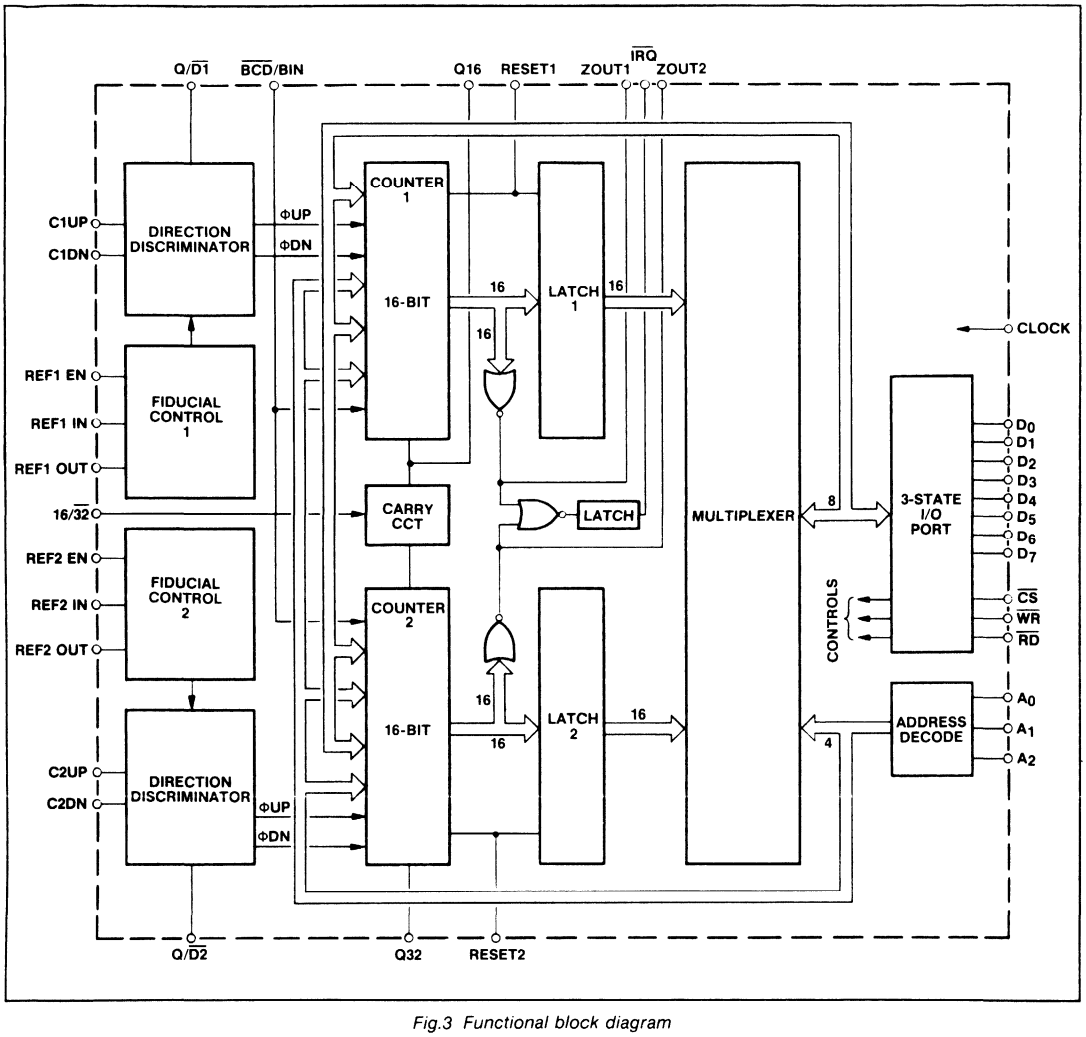



*Fig.3 Functional block diagram*

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| Supply voltage | -0.3V to 7V | Storage temperature | -65°C to +150°C |
| Input voltage | -0.3V to $V_{DD}$ +0.3V | Operating temperature | -40°C to +85°C |
| Output voltage | -0.3V to $V_{DD}$ +0.3V | | |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = 0°C to +85°C, $V_{DD}$ = 5V ± 10%

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Input high voltage | 2.0 | | | V | |
| Input low voltage | | | 0.8 | V | |
| Input leakage current | -10 | | 10 | μA | |
| Output high voltage | 4 | | | V | $I_{out}$ = -1.6mA |
| Output low voltage | | | 0.4 | V | $I_{out}$ = +3.2mA |
| 3-state leakage current | -40 | | 40 | μA | $V_{out}$ = 1.4V |

## PIN DESCRIPTIONS

| Symbol | Pin No. | Pin name and description |
|---|---|---|
| **Inputs** | | |
| $\overline{CS}$ | 30 | **Chip Select**, active low. |
| A0/A2 | 12,11,10 | **Address Lines**, allow access to the four internal latches when reading from the device,and access to the counter stages when writing to it. When reading from address 100, the counter values are transferred to the latches. See Table 1. During a READ operation the data contained in the latches is tranferred to the data bus. During a WRITE operation, the data on the data bus is loaded into the counter addressed. |
| Q/$\overline{D1}$,Q/$\overline{D2}$ | 14,27 | Selects quadrature x 4 or direct counting mode. |
| RESET1,2 | 15,26 | A High on one of these lines resets the clocking circuitry and all counters to zero. The line must be taken low again for counting to recommence. In the 1 x 32 mode, RESET1 resets all counters and latches. |
| CLOCK | 20 | This line is used to clock the count input signals into the steering circuit on its negative going edge. The next positive going edge transfers data from the counters to the latches when address 000 is read. |
| 16/$\overline{32}$ | 28 | Selects 16 or 32 bit counting. In the 32 bit mode all lines referring to counter 2 are inactive. |
| $\overline{BCD}$/BIN | 29 | **BCD or Binary Select**. In the BCD mode the counters are configured as either two 4-decade counters or one eight decade counter depending on the state of the 16/32 select line. |
| C1UP,C2UP, C1DN,C2DN | 16,23,17,24 | These are the input lines to the counters. In the quadrature mode, the phase relationship between the signals on lines UP and DN determine the direction of count. In the direct mode, input UP or DN will cause a count up or down if the other input is held High. Holding one input Low in this mode will disable the other input. In the quadrature mode, the maximum count rate will be slightly less than $f_{CLOCK}/4$, and in DIRECT mode $f_{CLOCK}/2$. |
| REF1 EN, REF2 EN | 19,21 | **Reference Latch 1,2,Enable**. A High level will enable the fiducial circuit for Counter 1 or 2 respectively. |
| REF1 IN, REF2 IN | 18,22 | **Reference 1,2 Input**. If one of the fiducial circuits is enabled, a positive transition on REF1 or 2 IN will freeze the count for that particular counter. The next positive edge on REF1 or 2 IN will unfreeze the counter, after REF. LATCH ENABLE goes low. |
| D0/D7 | 37,38,39,40, 1,2,3,4 | **I/O Data Lines**. When $\overline{CS}$ is High these lines are high impedance, when Low these lines can be inputs or outputs depending on the state of $\overline{WR}$ and $\overline{RD}$. |
| $\overline{WR}$ | 32 | **Write** control line, used to write to counters. |
| $\overline{RD}$ | 31 | **Read** control line, used to read latches. |
| **Outputs** | | |
| ZOUT1, ZOUT2 | 7,34 | **Zero Out 1/2**. A High on one of these lines indicates that the respective counter is at zero. |
| $\overline{IRQ}$ | 8 | **Interrupt Request**. A Low output signifies that either counter is at zero. $\overline{IRQ}$ is cleared whenever the device is read. |
| REF1 OUT, REF2 OUT | 9,33 | These lines indicate that the fiducial circuits are active and set. REF1,2 OUT can be reset by either the relevant RESET or by putting REFERENCE LATCH ENABLE low, followed by a positive transition on REF INPUT. |

| $\overline{CS}$ | A0 | A1 | A2 | ACTION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | READ/WRITE LOW BYTE COUNTER 1 |
| 0 | 1 | 0 | 0 | READ/WRITE HIGH BYTE COUNTER 1 |
| 0 | 0 | 1 | 0 | READ/WRITE LOW BYTE COUNTER 2 |
| 0 | 1 | 1 | 0 | READ/WRITE HIGH BYTE COUNTER 2 |
| 0 | 0 | 0 | 1 | LATCH DATA |
| 1 | X | X | X | NONE |

*Table 1 Truth table for address lines*

# SP9960

## 50 MBIT MANCHESTER BIPHASE-MARK ENCODER AND LED DRIVER

The SP9960 is a Manchester biphase-mark encoder and LED driver, designed for use in fibre-optic links at up to 50Mbit/s.

It encodes TTL or ECL data and outputs the result as a current at either the large or the small LED driver output. The LED driver and the current output are selectable.

### FEATURES

- Up to 50Mbit/s Operation
- TTL or ECL Inputs
- Choice of LED Drivers - Large or Small
- Choice of LED Drive Currents
- LED Driver Enable Control
- Single Supply Voltage
- —40°C to +85°C Operating Temperature Range

### APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface

### ORDERING INFORMATION

**SP9960B DG** (Industrial - Ceramic DIL package)
**SP9960B MP** (Industrial - Miniature Plastic DIL package)
**SP9960B LC** (Industrial - LCC package)

### ASSOCIATED PRODUCTS

**SP9920** Decoder with Idle Detect
**SP9921** Decoder
**SL9901** Transimpedance Amplifier

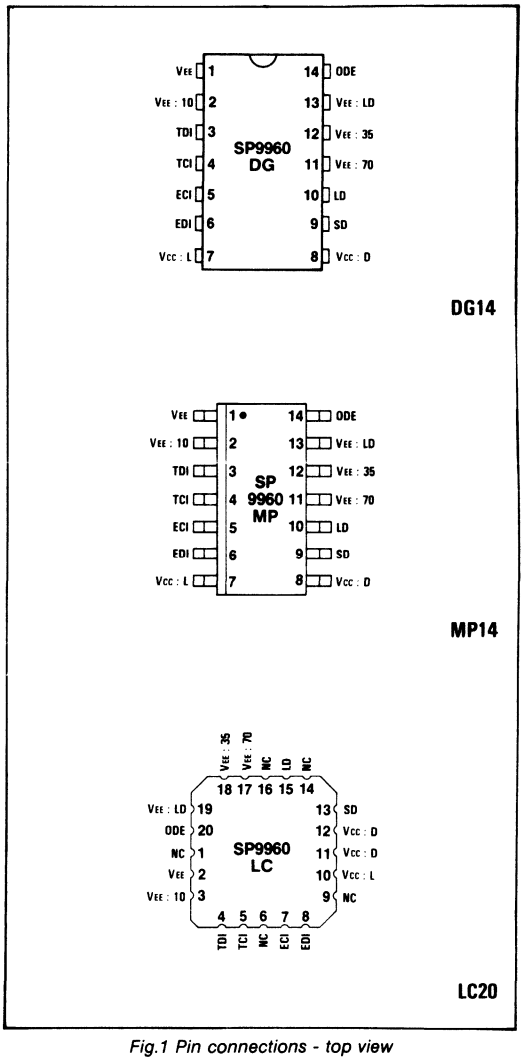



*Fig.1 Pin connections - top view*

## FUNCTIONAL DESCRIPTION

Fig.2 shows the simplified block diagram of the device. Data arriving at a data input (TDI or EDI pin) is sampled by the positive edge of the appropriate clock (TCI or ECI pin), encoded into a biphase-mark signal, and output as a current at the chosen LED driver (SD or LD pin).

If TTL inputs are to be used (TDI and TCI pins) then the ECL inputs (EDI and ECI) should be left unconnected and vice versa.

### Biphase-Mark Encoding

Fig.3 shows how the biphase-mark encoding scheme works. The input data is sampled by the positive edge of the clock. If the data is high (logic 1) then the driver switches to its opposite state (i.e. off if it was previously on, or on if it was previously off). If the data is low (logic 0) then the driver does not switch to its opposite state on the positive clock edge.

Regardless of the sampled input data, the driver always switches to its opposite state on the negative edges of the clock.

This form of encoding ensures a high number of transitions in the signal which simplifies the task of clock recovery at a remote detector. Since the data is encoded in terms of transitions, rather than as absolute levels, the signal can be given a net inversion without corrupting the information carried.

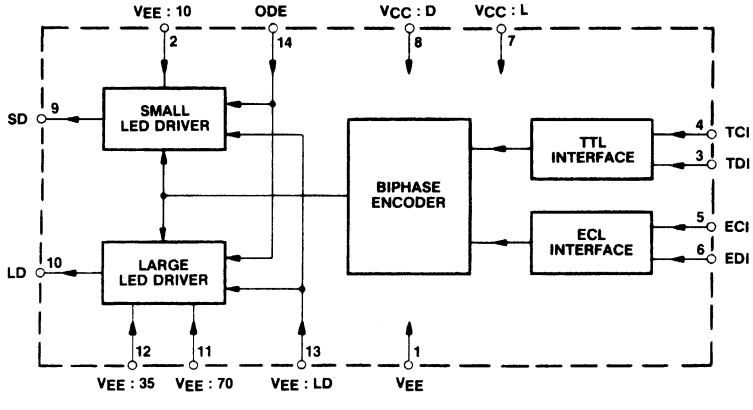
### LED Drivers

There are two LED driver outputs, the small driver (SD pin) and the large driver (LD pin). The driver used is chosen by the $V_{EE}$ : LD pin, which should be tied to the $V_{EE}$ pin to select the large driver and left unconnected to select the small driver.

The small driver outputs either 15 or 25mA (typically) when on. If the $V_{EE}$ : 10 pin is tied to $V_{EE}$ then the output is boosted by 10mA to 25mA. If the $V_{EE}$ : 10 pin is unconnected then the output remains at 15mA.

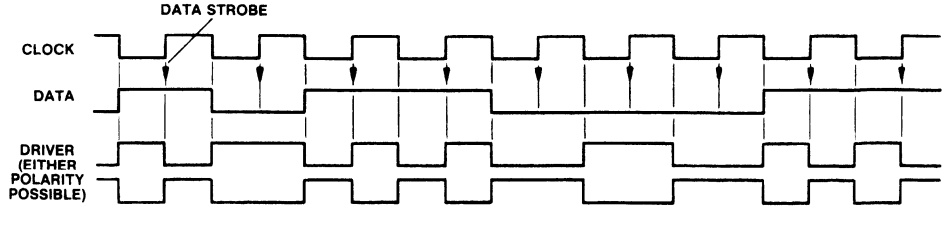
The large driver outputs 45, 80, 115 or 150mA (typically) when on. If the $V_{EE}$ : 35 pin is tied to $V_{EE}$ then the output is boosted by 35mA and if the $V_{EE}$ : 70 pin is tied to $V_{EE}$ then it is boosted by 70mA. If both these pins are left unconnected then the output remains at 45mA.

The drivers are disabled by pulling the ODE pin low. They are enabled if the ODE pin is left unconnected or pulled high.




N.B. Pin Numbers refer to Ceramic DIL (DG) and Miniature Plastic (MP) Packages

*Fig.2 Functional block diagram*




N.B. The polarity of the driver is determined by the previous data transmitted.

*Fig.3 Encoding alignment*

## PIN DESCRIPTIONS

| Symbol | Pin No. | | Pin Name and Description |
|---|---|---|---|
| | DG,MP | LC | |
| $V_{EE}$ | 1 | 2 | **Negative Supply (Power Input).** 0V. |
| $V_{EE}$ : 10 | 2 | 3 | **10mA Negative Supply (Power Input).** 0V or no connection. This pin should be tied to the negative supply ($V_{EE}$) to increase the current sinked at the small current LED output driver (SD pin) by 10mA (typically) if the small driver is selected. It should be left unconnected otherwise. |
| TDI | 3 | 4 | **TTL Data Input (TTL Input with Internal Pull-down).** Transitor-transitor logic (TTL) data is strobed in at this pin by the positive edges of the TTL clock input (TCI pin). This pin should be left unconnected if the TTL inputs are not to be used. |
| TCI | 4 | 5 | **TTL Clock Input (TTL Input with Internal Pull-Down).** The rising edge of this clock is used to strobe the TTL data input (TTI pin). This pin should be left unconnected if the TTL inputs are not to be used. |
| ECI | 5 | 7 | **ECL Clock Input (ECL Input with Internal Pull-down).** The rising edge of this clock is used to strobe the ECL data input (EDI pin). This pin should be left unconnected if the ECL inputs are not to be used. |
| EDI | 6 | 8 | **ECL Data Input (ECL Input with Internal Pull-down).** Emitter-coupled logic (ECL) data is strobed in at this pin by the positive edges of the ECL clock input (ECI pin). This pin should be left unconnected if the ECL inputs are not to be used. |
| $V_{CC}$ : L | 7 | 10 | **Logic Positive Supply (Power Input). This is the positive supply for the input** buffers and logic. |
| $V_{CC}$ : D | 8 | 11,12 | **Driver Positive Supply (Power Input).** This is the positive supply for the output drivers. |
| SD | 9 | 13 | **Small Driver (Current Sink Output).** This is the small current LED output driver. Data supplied at the clock and data pins is encoded and output as a current at this pin if the large driver negative supply pin ($V_{EE}$ : LD) is left unconnected. |
| LD | 10 | 15 | **Large Driver (Current Sink Output).** This is the large current LED output driver. Data supplied at the clock and data pins is encoded and output as a current at this pin if the large driver negative supply pin ($V_{EE}$ : LD) is tied to the negative supply ($V_{EE}$). |
| $V_{EE}$ : 70 | 11 | 17 | **70mA Negative Supply (Power Input).** 0V or no connection. This pin may be used in conjunction with the $V_{EE}$ : 35 pin. It should be tied to the negative supply ($V_{EE}$) to increase the current sinked at the large current LED output driver (LD pin) by 70mA (typically) if the large driver is selected. It should be left unconnected otherwise. |
| $V_{EE}$ : 35 | 12 | 18 | **35mA Negative Supply (Power Input).** 0V or no connection. This pin may be used in conjunction with the $V_{EE}$ : 70 pin. It should be tied to the negative supply ($V_{EE}$) to increase the current sinked at the large current LED output driver (LD pin) by 35mA (typically) if the large driver is selected. It should be left unconnected otherwise. |
| $V_{EE}$ : LD | 13 | 19 | **Large Driver Negative Supply (Power Input).** 0V or no connection. This pin should be tied to the negative supply ($V_{EE}$) if the large current LED output driver (LD pin) is to be used. It should be left unconnected if the small current LED output driver (SD pin) is to be used. |
| ODE | 14 | 20 | **Output Driver Enable (Programming Input with Internal Pull-up).** This pin should be left unconnected for normal operation. If it is low then the LED output driver is disabled. |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{CC}$ = +5V ± 0.5V, $T_{amb}$ = -40°C to +125°C.
All voltages are with respect to $V_{EE}$ (Ground).

### Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[1] | Max. | | |
| Supply current | $I_{CC}$ | | 25 | 40 | mA | Outputs disabled |
| Programming input low voltage | $V_{ILP}$ | 0 | | 0.4 | V | |
| Programming input high voltage | $V_{IHP}$ | 2.0 | | $V_{CC}$ | V | |
| TTL input low voltage | $V_{ILT}$ | 0 | 0.4 | 0.8 | V | |
| TTL input high voltage | $V_{IHT}$ | 2.0 | 2.4 | $V_{CC}$ | V | |
| ECL input low voltage | $V_{ILE}$ | 0 | | $V_{CC}$ -1.65 | V | |
| ECL input high voltage | $V_{IHE}$ | $V_{CC}$ -0.96 | | $V_{CC}$ | V | |
| Programming input current | $I_P$ | | | 10 | mA | $0 < V < V_{CC}$ |
| TTL input current | $I_T$ | | | 100 | μA | $0 < V < V_{CC}$ |
| ECL input current | $I_E$ | | | 250 | μA | $0 < V < V_{CC}$ |
| Small driver on current (sink) | $I_{SD}$ | 12 | 15 | 18 | mA | $1 < V < V_{CC}$, default |
| | | 22 | 25 | 28 | mA | +10mA |
| Large driver on current (sink) | $I_{LD}$ | 40 | 45 | 50 | mA | $1 < V < V_{CC}$, default |
| | | 70 | 80 | 90 | | +35mA |
| | | 105 | 115 | 125 | | +70mA |
| | | 135 | 150 | 165 | | +105mA |
| Driver off leakage (sink) | $I_L$ | | | 5 | μA | $0 < V < V_{CC}$ |
| Pin capacitance | $C_P$ | | 7 | 15 | pF | |

### Digital Switching Characteristics (see Fig.4)

| Characteristc | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[1] | Max. | | |
| Clock frequency | $f_C$ | | 50 | 60 | MHz | |
| Clock high period | $t_{CH}$ | 5 | | | ns | |
| Clock low period | $t_{CL}$ | 5 | | | ns | |
| Input data set-up time | $t_{IS}$ | 5 | | | ns | |
| Input data hold time | $t_{IH}$ | 5 | | | ns | |
| Output data hold time | $t_{OH}$ | 0 | | | ns | |
| Output data delay | $t_{OD}$ | | 3 | 5 | ns | |

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

## ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied. Voltages are with respect to $V_{EE}$ (Ground).

| | |
|---|---|
| Positive supply voltage, $V_{CC}$ | 0V to +8V |
| Input voltage, $V_I$ | -0.3V to $V_{CC}$ +0.3V |
| Output voltage, $V_O$ | -0.3V to $V_{CC}$ +0.3V |
| Storage temperature, $T_{TS}$ | -55°C to +125°C |
| Package power dissipation, $P_P$ | 380mW |

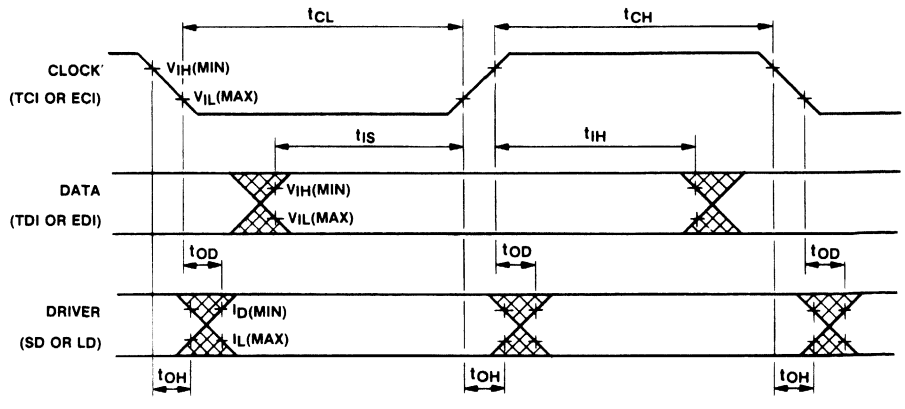
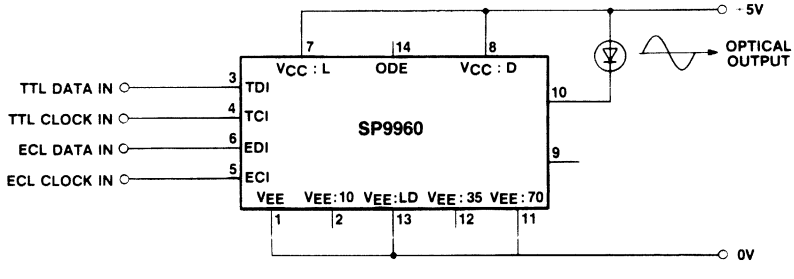



*Fig.4 Digital switching characteristics*




N.B. Pin Numbers refer to Ceramic DIL (DG) and Miniature Plastic (MP) Packages

*Fig.5 Typical application circuit - Large driver at 115mA (nominal) chosen*

# SL9901

## 50MHz TRANSIMPEDANCE AMPLIFIER

The SL9901 is a monolithic silicon integrated circuit designed to interface between a detector diode and a decoder in a Fibre Optic Receiver system.

In the SL9901, the photocurrent generated by a PIN diode is converted to a voltage suitable for driving a comparator input stage in a decoder/detector circuit. The SL9901 has a 3dB electrical bandwidth of 50MHz enabling NRZ data rates of up to 100Mbit/s to be received.

### FEATURES

- High Sensitivity
- 50MHz Bandwidth (100Mbits/NRZ Data Rate)
- Wide Dynamic Range
- 5 Volt Supply
- Usable in Systems with $10^{-9}$ BER at −36dBm Average Optical Power

### APPLICATIONS

- Fibre Optic Data Links
- Nucleonics
- Instrumentation
- Current/Voltage Conversion

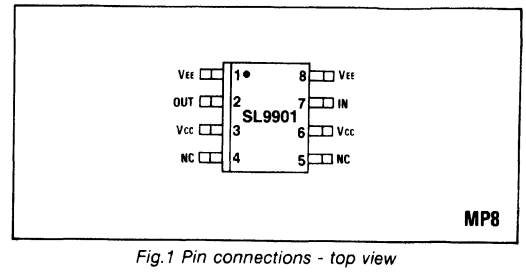



*Fig.1 Pin connections - top view*

### ASSOCIATED PRODUCTS

**SP9920** Decoder with Idle Detect
**SP9921** Decoder
**SP9960** Encoder and LED Driver

### ORDERING INFORMATION

**SL9901B MP** (Industrial - Miniature Plastic DIL package)

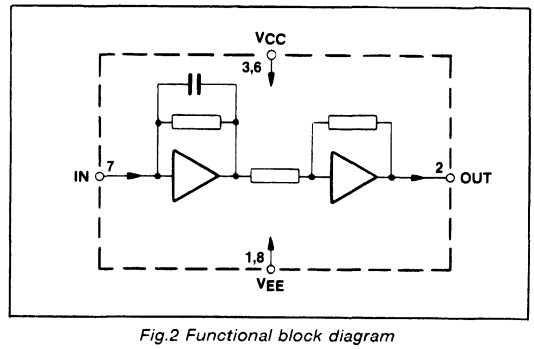



*Fig.2 Functional block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{CC}$ +5V ± 0.5V, $T_{amb}$ = -40°C to +85°C, Input current $I_I$ = 0.3μA to 10μA.
All voltages are with respect to $V_{EE}$ (Ground)

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[1] | Max. | | |
| Supply current | $I_{CC}$ | | 12 | | mA | Output unloaded |
| Input bias voltage | $V_{IB}$ | | 1.5 | | V | |
| Input impedance | $Z_I$ | | 400 | | Ohms | |
| Input current at clipping | $I_{IC}$ | 10 | | | μA | |
| Transimpedance gain | $G_T$ | | 40 | | kohms | |
| Bandwidth | $f_B$ | 50 | | | MHz | 3dB point |
| Output impedance | $Z_O$ | | | 50 | Ohms | |
| Output noise over band | $N_O$ | | | 2 | mV | 1 < f < 160MHz (See Note 2) |
| Pin capacitance | $C_P$ | | 1.5 | | pF | |

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The noise figure quoted here is adequate for approximate performance calculations, but it should be noted that the noise is not purely white.

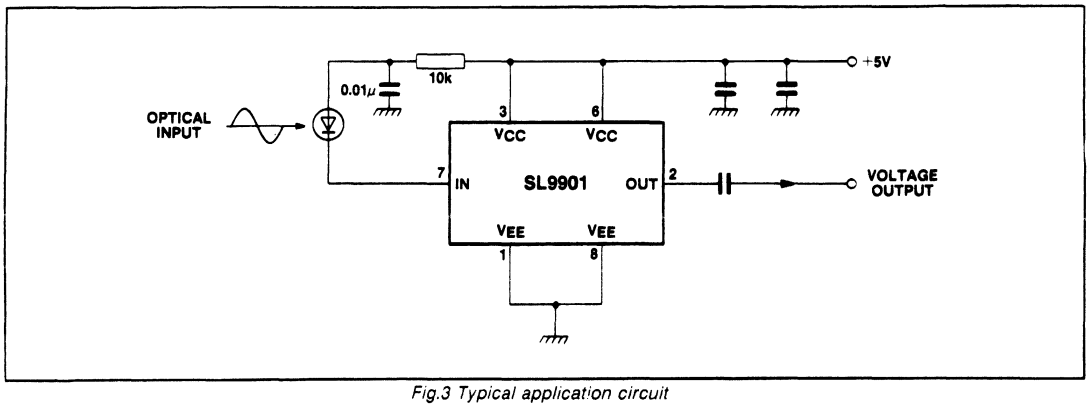



*Fig.3 Typical application circuit*

## ABSOLUTE MAXIMUM RATINGS

*Exceeding these ratings may cause permanent damage.*
Functional operation under these conditions is not implied.
Voltages are with respect to $V_{EE}$ (Ground).

| | |
|---|---|
| Positive supply voltage, $V_{CC}$ | 0V to +7V |
| Input voltage (device sourcing current), $V_I$ | 0V |
| Input current (device sinking current), $I_I$ | 1mA |
| Output voltage (device sinking current), $V_O$ | $V_{CC}$ |
| Output current (device sourcing current), $I_O$ | 10mA |
| Storage temperature, $T_{ST}$ | -55°C to +125°C |

# SP9920

## 50MBIT MANCHESTER DECODER WITH IDLE CODE DETECT

The SP9920 is a monolithic silicon integrated circuit for clock and data recovery from a Manchester biphase mark encoded input signal. It operates from a single 5V supply with ECL outputs, and has an Idle Code Detect output.

### FEATURES

- 20M-50M Operating Range
- Single 5V Supply
- Sensitive Differential Input
- ECL Output
- Input Signal Detection from Lock Detect
- Output
- No False Frequency Lock
- Idle Code Detect

### APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | 7.5V |
| Storage temperature | -55°C to +125°C |
| Operating temperature range | -40°C to +85°C |

### ORDERING INFORMATION

**SP9920 DG** Ceramic Package
**SP9920 MP** SO Package
**SP9920 LC** Chip Carrier Package

### ASSOCIATED PRODUCTS

**SP9921** 50MBit Manchester Decoder
**SP9960** 50MBit Manchester Decoder + LED Drive
**SP9901** 50MBit Transimpedance Amplifier

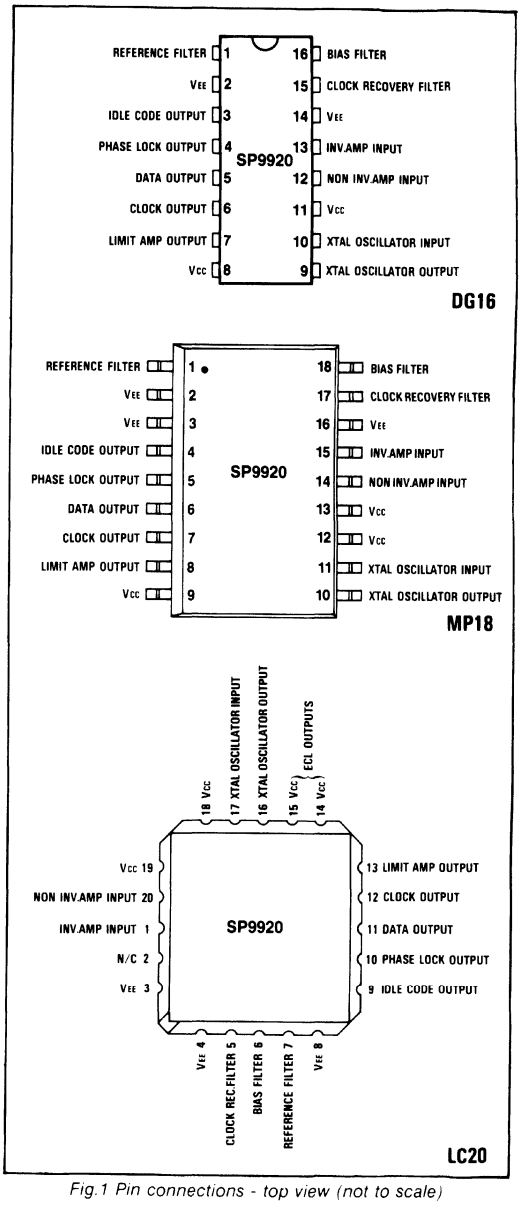



*Fig.1 Pin connections - top view (not to scale)*

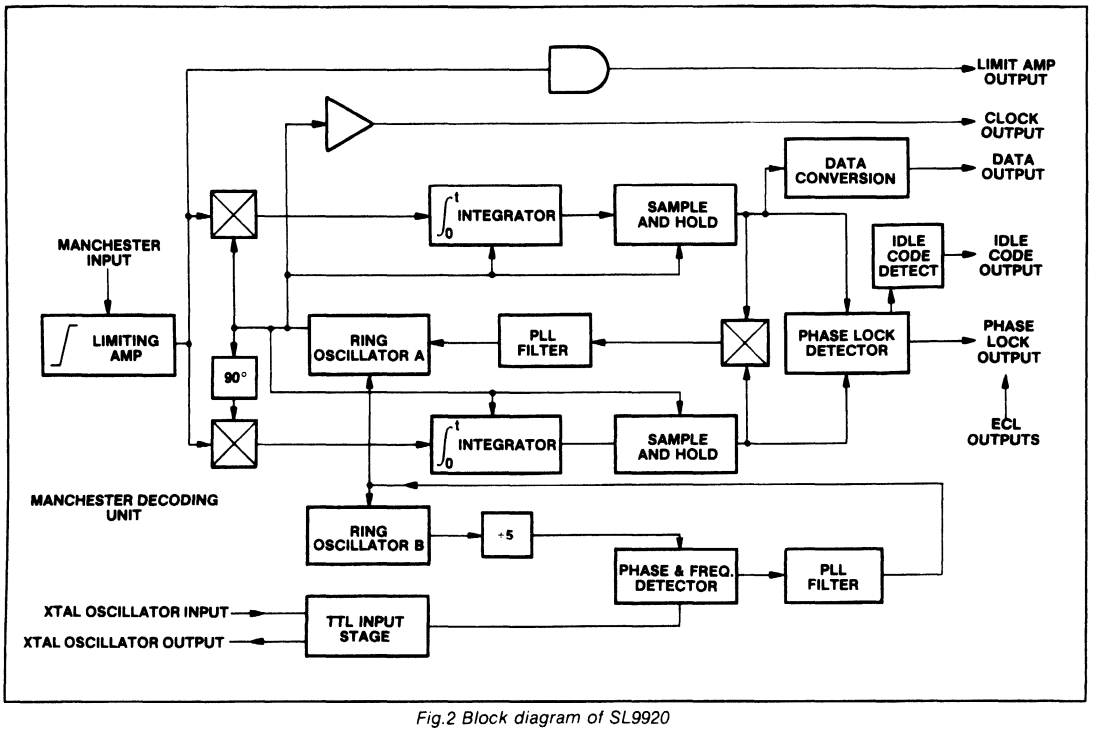



*Fig.2 Block diagram of SL9920*

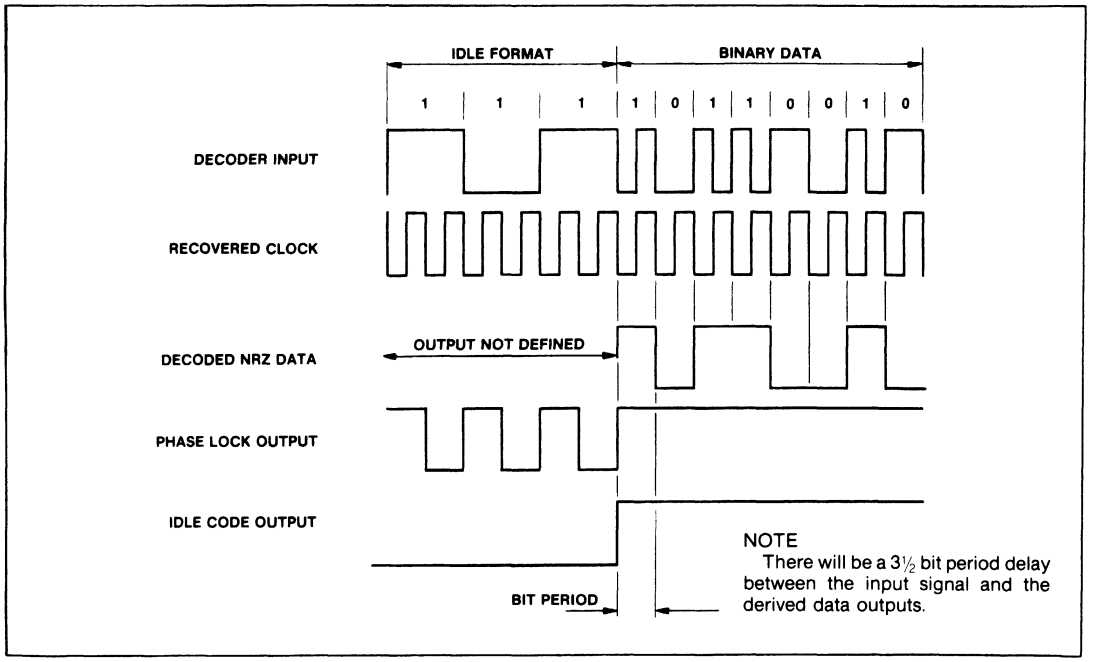



*Fig.3 Timing diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Supply voltage = 5V ± 10%. $T_{amb}$ = -40°C to +85°C
Voltages measured with respect to positive supply

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Power supply** | | | | | |
| Pins 2 & 15 - 8 & 11 | | | | | |
| Supply voltage | -4.5 | | -5.5 | V | |
| Supply current | | 100 | | mA | |
| **Limiting amplifier** | | | | | |
| Pins 12 & 13 | | | | | |
| Differential input drive | 10 | | 1000 | mV | rms |
| Input offset voltage | | | 5 | mV | |
| Input bias voltage | | -2.5 | | V | ½ supply voltage |
| Differential input impedance | | 1000 | | Ohms | |
| Pin 10 | | | | | |
| Clock rate/REF frequency ratio | | 5 | | | TTL clock ref |
| **Clock recovery PLL** | | | | | |
| PLL pull in/pull off | ±10% | | | | From centre frequency defined by REF frequency input |
| **ECL outputs (10k)** | | | | | |
| Pins 3, 4, 5, 6 & 7 | | | | | |
| Output high voltage | -0.96 | | -0.81 | V | |
| Output low voltage | -1.85 | | -1.65 | V | |
| Internal pull down current | | 2 | | mA | |
| Output drive current | | | 10 | mA | |

## OPERATING NOTES

The circuit incorporates two phase locked loops, one acting as a frequency comparator providing bias to determine the centre operating frequency of the clock recovery circuit. The operating frequency is modified by the second loop to produce a clock signal locked to the input signal.

The SP9920 uses a crystal oscillator reference. The reference frequency is ⅕ of the signal clock frequency. The input signal is amplified by a differential limiting amplifier, with an ECL output. NRZ data output together with a clock output is provided, also with ECL levels.

A phase lock detector provides input signal detection.

Decoding is accomplished by means of a Costas loop incorporating on-chip integrate and hold circuits. The loop response characteristics are determined by external resistor and capacitor forming the phase lock loop filter.

The circuit incorporates a differential limiting amplifier as an input stage, which is capable of operating with a 10mV input signal. Output drive of the clock, data and phase lock signals are ECL compatible. A logic '1' signal is generated at the phase lock output when the data signal is greater than the error signal in the Costas loop, thus indicating the clock is in phase with the signal input. An offset is incorporated such that when no signal is present on the input the phase lock output is logic '0'.

Also provided on-chip is a crystal oscillator maintaining circuit operating at ⅕ of the input clock frequency, and an Idle Code Detect output which is an ECL 10K logic level.

The second phase lock loop is used to set up the centre operating frequency of the ring oscillator circuits. This is achieved by comparing a divided down sister oscillator (Ring Oscillator B) output with an external clock reference signal derived from the internal crystal oscillator. The ring oscillator in the Costas loop is designed such that its frequency can be pulled ±10% off the reference frequency by the phase correcting signal from the PLL filter.

# SP9921

## 50 MBIT MANCHESTER BIPHASE-MARK DECODER

The SP9921 is a bipolar monolithic silicon integrated circuit for clock and data recovery from a Manchester biphase-mark encoded input signal. It operates from a single 5V supply and has ECL outputs.

### FEATURES

- 20 to 50Mbit/s Operating Range
- Single Supply Voltage
- Sensitive Differential Input
- ECL Outputs
- Input Signal Detection from Lock Detect Output
- No False Frequency Lock
- —40°C to +85°C Operating Temperature Range

### APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface

### ORDERING INFORMATION

**SP9921B DG** (Industrial - Ceramic DIL package)
**SP9921B MP** (Industrial - Miniature Plastic DIL package)
**SP9921B LC** (Industrial - LCC package)

### ASSOCIATED PRODUCTS

**SL9901** Transimpedance Amplifier
**SP9920** Decoder with Idle Detect
**SP9960** Encoder and LED Driver

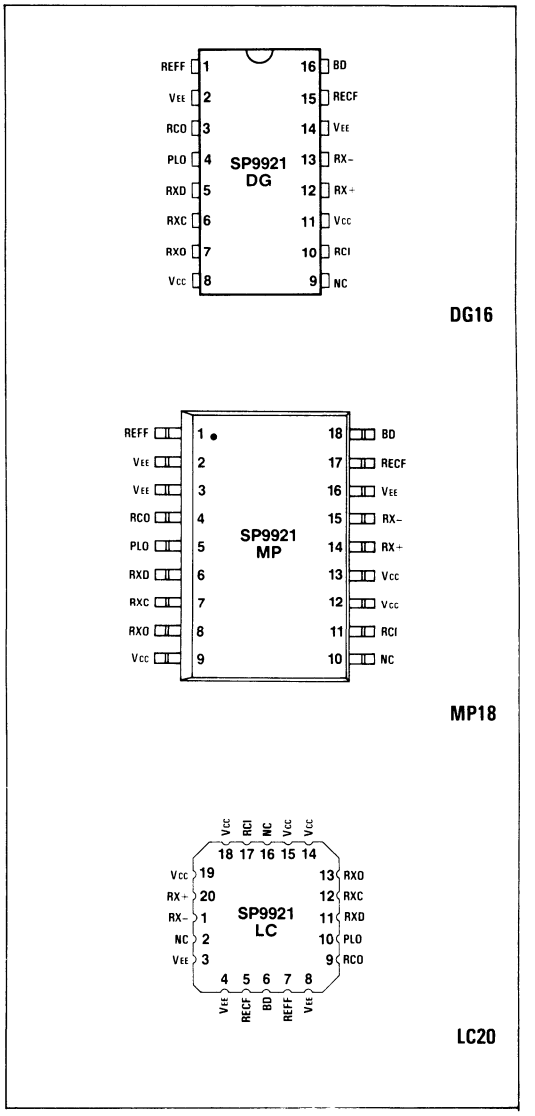



*Fig.1 Pin connections - top view*

## FUNCTIONAL DESCRIPTION

Fig.2 shows the simplified block diagram of the device. It locks onto incoming data, recovers the clock and decodes the data making use of a reference clock input at approximately one fifth of the data rate.

### Receive Path

Data is received at the differential input pins (RX + and RX-) of the limiting amplifier which outputs the digital received signal for monitoring at the amplifier output pin (RXO). This signal is fed into a Costas loop which outputs the recovered clock (RXC pin) and the decoded data (RXD pin).

Fig.3 shows how the input signal is decoded. The Manchester biphase-mark code uses a transition at the centre of the bit to indicate a one and the absence of a transition to indicate a zero. In addition there is always a transition at the end of the bit.

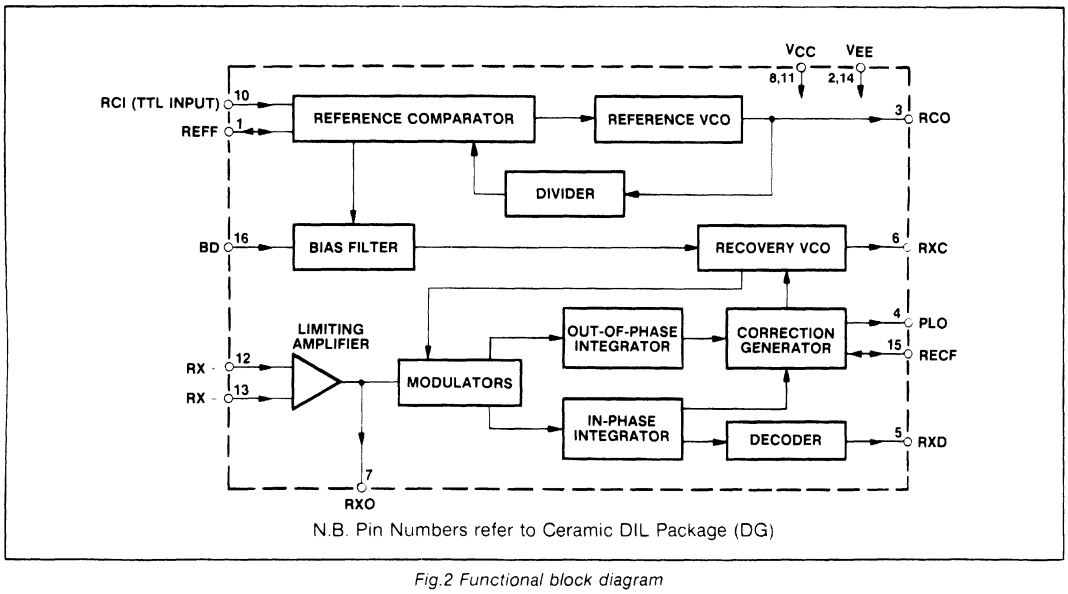
### Phase-Locking and Signal Recovery

The SP9921 can be used in systems operating over a wide range of data rates without false frequency lock. This is achieved using a reference VCO and a recovery VCO.

The reference VCO is phase-locked to the reference clock input (RCI pin). This generates an internal clock at 5 times the frequency of the reference clock input. The output of this VCO is output for monitoring on the reference clock output (RCO pin). Filtering of the bias control signal to the VCO is performed at the reference filter pin (REFF).

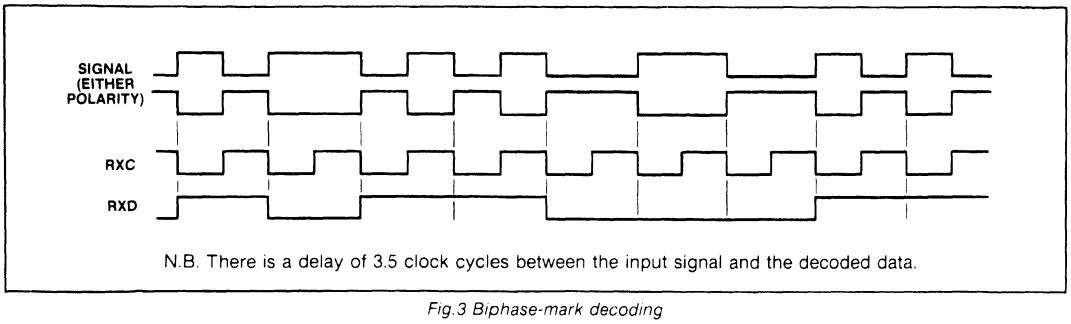
The bias control signal for the reference VCO is filtered at the bias decoupling pin (BD) and used to set the free-running frequency of the recovery VCO. The recovery VCO drives the receive clock (RXC pin) and the modulators which in turn drive the integrators. The integrators analyse the components of the signal which are in phase and 90° out of phase and so obtain the recovered data and the correction signal for the Costas loop. The correction signal is filtered at the recovery filter pin (RECF).

The Costas loop also pulls the phase-lock output pin (PLO) low when the transition at the end of the encoded data bit is not detected. This can occur when there is a loss of data, if there is enough noise on the link (even if no data is corrupted) or if the Costas loop has difficulty locking (for instance if the time constant at the recovery filter pin is too great).




N.B. Pin Numbers refer to Ceramic DIL Package (DG)

*Fig.2 Functional block diagram*




N.B. There is a delay of 3.5 clock cycles between the input signal and the decoded data.

*Fig.3 Biphase-mark decoding*

## PIN DESCRIPTIONS

| Symbol | Pin No. | | | Pin Name and Description |
|---|---|---|---|---|
| | DG | MP | LC | |
| REFF | 1 | 1 | 7 | **Reference Filter (Current Output/Voltage Input).** A series RC network should be connected between this pin and ground ($V_{EE}$) to provide the filtering for the control of the reference VCO. |
| $V_{EE}$ | 2 | 2,3 | 8 | **Negative Supply (Power Input).** 0V. |
| RCO | 3 | 4 | 9 | **Reference Clock Out (ECL Output).** This pin should output a clock which is phase-locked to the reference clock input (RCI pin) but which is 5 times its frequency. |
| PLO | 4 | 5 | 10 | **Phase Lock Out (ECL Output).** This pin goes low when the device fails to detect a transition at the end of the undecoded received data. |
| RXD | 5 | 6 | 11 | **Received Data (ECL Output).** This pin outputs the decoded received data. |
| RXC | 6 | 7 | 12 | **Received Clock (ECL Output).** This pin outputs the recovered clock. |
| RXO | 7 | 8 | 13 | **Receive Out (ECL Output).** This pin outputs the undecoded received data. |
| $V_{CC}$ | 8 | 9 | 14,15 | **Positive Supply (Power Input).** 5V. |
| NC | 9 | 10 | 16,2 | **No Connection.** This pin should be left unconnected for normal operation. |
| RCI | 10 | 11 | 17 | **Receive Clock In (TTL Input).** This is the input for the reference clock which sets the free-running frequency for the recovery VCO. Its frequency should be close to one fifth of the received data rate. |
| $V_{CC}$ | 11 | 12,13 | 18,19 | **Positive Supply (Power Input).** 5V. |
| RX +,- | 12,13 | 14,15 | 20,1 | **Receive Plus and Minus (Analog Voltage Inputs).** These are the differential inputs to the limiting receive amplifier. They are self-biasing and would normally be capacitively coupled. For a single-ended input the unused pin should be capacitively coupled to ground. |
| $V_{EE}$ | 14 | 16 | 3,4 | **Negative Supply (Power Input).** 0V. |
| RECF | 15 | 17 | 5 | **Recovery Filter (Current Output/Voltage Input).** A series RC network should be connected between this pin and ground ($V_{EE}$) to provide the filtering for the control of the recovery VCO. |
| BD | 16 | 18 | 6 | **Bias Decoupling (Decoupling Node).** A capacitor should be connected between this pin and ground ($V_{EE}$) to eliminate noise on the bias voltage generated by the reference PLL and which sets the free-running frequency of the recovery VCO. |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$V_{CC}$ = +5V ± 0.5V, $T_{amb}$ = -40°C to +125°C.

All voltages are with respect to $V_{EE}$ (Ground).

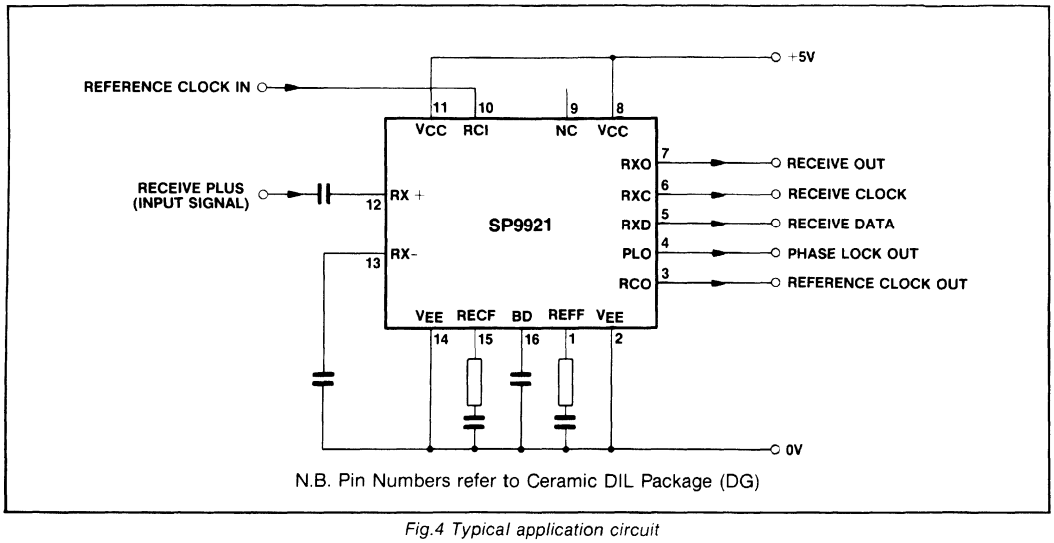
### Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[1] | Max. | | |
| Supply current | $I_{CC}$ | | 100 | | mA | Outputs unloaded |
| TTL input low voltage | $V_{ILT}$ | 0 | 0.4 | 0.8 | V | |
| TTL input high voltage | $V_{IHT}$ | 2.0 | 2.4 | $V_{CC}$ | V | |
| TTL input current | $I_T$ | | 2 | | mA | $0 < V < V_{CC}$ |
| ECL output high voltage | $V_{OH}$ | $V_{CC}$ -0.96 | | $V_{CC}$ -0.81 | mA | I(Source) = 10mA |
| ECL output low voltage | $V_{OL}$ | $V_{CC}$ -1.85 | | $V_{CC}$ -1.65 | mA | I(Sink) = 2mA |
| Pin capacitance | $C_P$ | | 7 | 15 | pF | |

## Dynamic Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[1] | Max. | | |
| Reference frequency | $f_{REF}$ | 20 | | 50 | MHz | |
| Differential receive voltage | $V_{RD}$ | 10 | | 1000 | mV | |
| Receive offset voltage | $V_{RO}$ | | | 5 | mV | |
| Receive bias voltage | $V_{RB}$ | | $V_{CC}/2$ | | mA | |
| Receive input impedance | $Z_{RI}$ | | 1000 | | Ohms | |
| Receive frequency offset | $O_{RF}$ | -10 | | 10 | % | w.r.t. reference |

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.




N.B. Pin Numbers refer to Ceramic DIL Package (DG)

*Fig.4 Typical application circuit*

## ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied. Voltages are with respect to $V_{EE}$ (Ground).

| | |
|---|---|
| Positive supply voltage, $V_{CC}$ | 0V to +8V |
| Input voltage, $V_I$ | -0.3V to $V_{CC}$ +0.3V |
| Output voltage, $V_O$ | -0.3V to $V_{CC}$ +0.3V |
| Storage temperature, $T_{ST}$ | -55°C to +125°C |
| Package power dissipation, $P_P$ | 600mW |

# Technical Data

## 2. Data conversion

# SP97508

## 8-BIT HIGH SPEED ADC

The Plessey SP97508 is an 8-bit flash ECL analog-to-digital converter. It incorporates 255 individual comparators, a reference chain and a full D-type output latch. The ADC is capable of sampling in excess of 110MHz with full (Nyquist) analog bandwidth and has excellent dynamic performance. A conventional unity mark space ratio clock can be used and the output data can be programmed for true or inverse binary and 2s complement coding.

### FEATURES

- Pin Replacement for CX20116 — But Faster
- 110MHz Conversion Rate
- Full Scale Input Bandwidth: 120MHz (-3dB)
- Production Tested with 30MHz Analog Input
- Input Capacitance: 40pF
- No External Sample and Hold Needed
- Low Power Consumption: 1.2W (typ.)
- True/Inverse Binary and Twos Complement Coding
- Operating Temperature Range: -40°C to +85°C
- Unity Mark Space Ratio Clock

### APPLICATIONS

- Radar Video Digitising
- Instrumentation
- Nucleonics
- Studio Quality Video

### ORDERING INFORMATION

**SP97508 B DC** (Industrial - Sidebrazed DILMON package)

### ABSOLUTE MAXIMUM RATINGS ($T_{amb}$ = 25°C)

| | |
|---|---|
| Power Supply $V_{EE}$ | 0 to -7V |
| Analog Input $V_{IN}$ | +0.5 to $V_{EE}$ |
| Reference Voltages $V_{RT}$, $V_{RM}$, $V_{RB}$ | +0.5 to $V_{EE}$ |
| Reference Range \| $V_{RT}$ - $V_{RB}$ \| | 2.5V |
| Digital Inputs CLK, $\overline{CLK}$, MINV, LINV | 0.5 to -4V |
| Mid Ref Input Current I$V_{RM}$ | -10 to +10mA |
| Digital Output Current $I_D$ | 0 to -20mA |
| Voltage between Grounds | |
| AGND to DGND | -50 to +50mV |
| Voltage between Supplies | |
| $AV_{EE}$ to $DV_{EE}$ | -50 to +50mV |

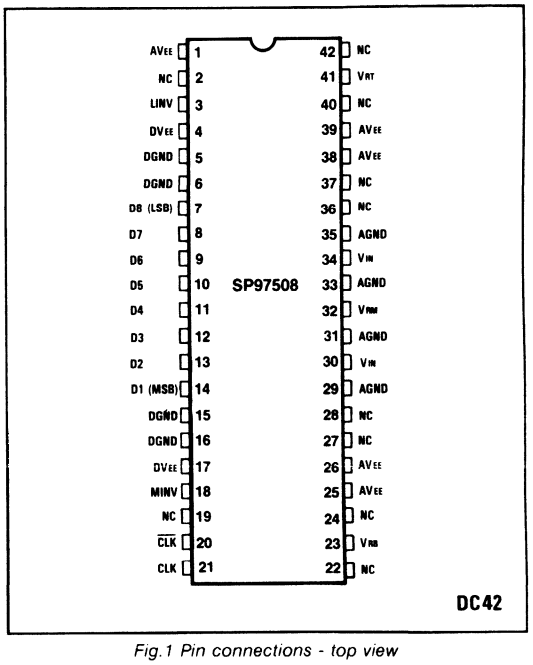



*Fig.1 Pin connections - top view*

### THERMAL CHARACTERISTICS

| | |
|---|---|
| Storage Temperature Range | -65° C to +150° C |
| Maximum Junction Operating Temperature | +175° C |
| Lead Temperature (Soldering 60 seconds) | 300° C |
| $\theta_{JA}$ | 32° C/W |
| $\theta_{JC}$ | 10° C/W |

### RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Supply Voltage | | -5.2V ± 0.25V |
| Reference ($V_{RT}$) | | 0V ± 0.1V |
| Reference ($V_{RB}$) | | -2.0V ± 0.2V |
| $AV_{EE}$ to $DV_{EE}$ | | 0mV ± 50mV |
| AGND to DGND | | 0mV ± 50mV |
| Analog Input | | 2V p-p max. |
| Clock ECL High | tpw1 = 6.8ns | for lowest BER |
| Clock ECL Low | tpw0 = 2.3ns | |
| Output Load | | 680Ω to -5.2V |

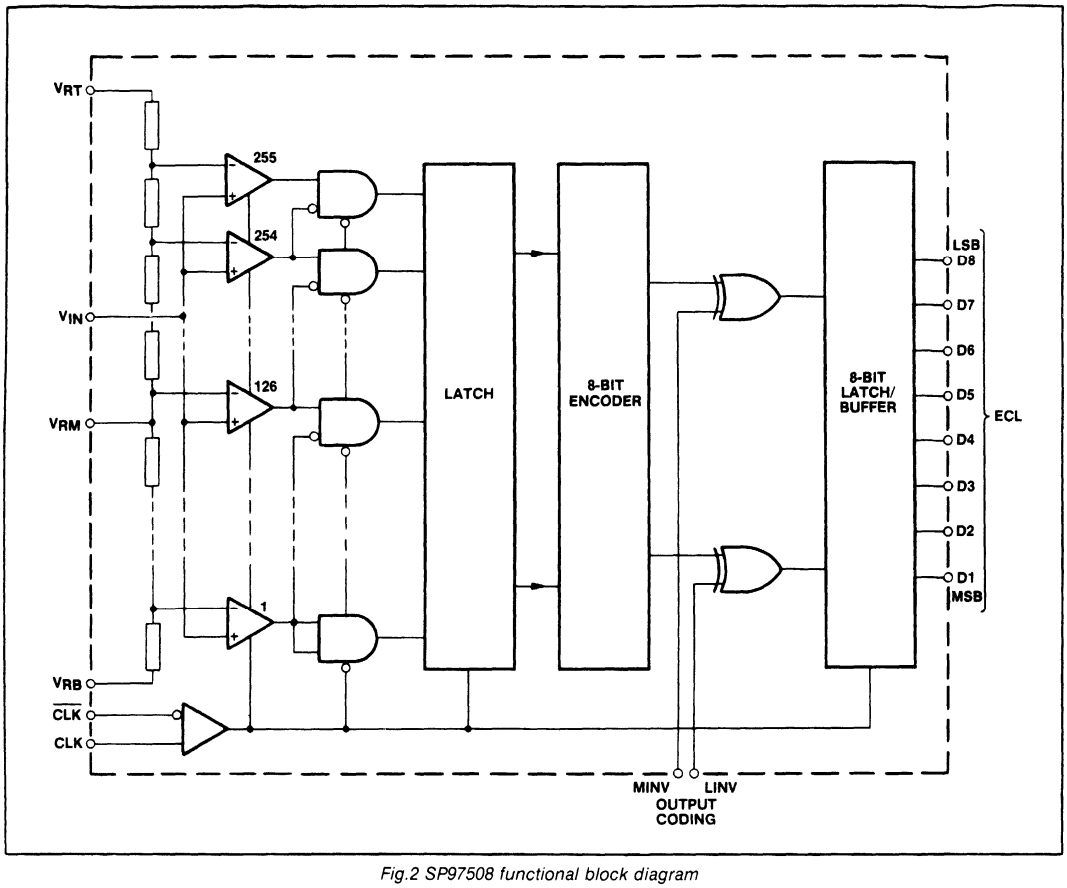



*Fig.2 SP97508 functional block diagram*

## PIN DESCRIPTION

| Symbol | Function |
|---|---|
| AVEE | Analog VEE, -5.2V (typ). |
| LINV | Input pin for output polarity invertion of data (see Table 1). |
| DVEE | Digital VEE, -5.2V (typ). |
| DGND | Digital GND, which is separated from the Analog GND. |
| D0 - D7 | Digital data output pins, ECL level. D0 = LSB. D7 = MSB. Pull-down resistors are necessary externally (typically 620Ω). |
| MINV | Input pin for output polarity inversion of D7 (MSB) (see Table 1). ECL level. '0' is held when it is open circuit. |
| $\overline{CLK}$ | Inverse clock input pin, ECL level. |
| CLK | Clock input pin, ECL level. Analog aquired on rising edge. |
| VRB | Reference voltage (bottom) -2V (typ). |
| AGND | Analog GND. |
| VIN | Analog input, input range is (VRT - VRB) p-p. |
| VRM | Middle point of the reference voltage, it can be used for linearity adjustment. |
| VRT | Reference voltage (top), 0V (typ). |
| NC | Empty pins (Not Connected). 2 and 19 should be grounded to DGND, the others should be grounded to AGND. |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25° C, $V_{EE}$ = -5.2V, $V_{RT}$ = 0V, $V_{RB}$ = -2V

| Characteristic | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum conversion rate | fc | 110 | | | MHz | $V_{IN}$ = 0 to -2V,fin = 1kHz, ramp |
| Analog conversion bandwidth | | | 50 | | MHz | No missing codes |
| Supply current | $I_{EE}$ | -180 | -220 | -260 | mA | |
| Analog input capacitance | $C_{IN}$ | | 35 | | pF | $V_{IN}$ = -1V + 0.07V rms |
| Analog input bias current | $I_{IN}$ | | 150 | 400 | μA | $V_{IN}$ = -1V |
| Reference resistor (see Note 1) | $R_r$ | | 105 | | Ω | |
| Offset voltage at ends of the | $V_{RT}$ | | 9 | | mV | |
| reference cabinet | $V_{RB}$ | | 17 | | mV | |
| Digital input voltage | $V_{IH}$ | -1.0 | -0.9 | -0.7 | V | |
| | $V_{IL}$ | -1.9 | -1.75 | -1.6 | V | |
| Digital input current | $I_{IH}$ | 0 | | 0.4 | mA | $V_{IH}$ = -0.9V |
| | $I_{IL}$ | -0.05 | | 0.35 | mA | $V_{IL}$ = -1.75V |
| Digital output voltage | $V_{OH}$ | -1.0 | | | V | $R_L$ = 620Ω to $V_{EE}$ |
| | $V_{OL}$ | | | -1.6 | V | |
| Output data delay | Td | | 2.5 | | ns | $R_L$ = 620Ω to $V_{EE}$ |
| Integral linearity error (DC) | | | ±0.5 | | LSB | fc = 100MHz<br>$V_{IN}$ = 0 to -2V,<br>fin = 48.8kHz sine |
| Differential linearity (DC) | | | | Note 2 | | fc = 100MHz,fin = 48.8kHz sine |
| Differential gain | DG | | 1.5 | | % | NTSC 40 IRE mod. ramp |
| Differential phase | DP | | 0.5 | | deg. | fc = 100MHz |
| Aperture jitter | | | 30 | | ps | |

NOTES
1. $R_r$ is the total resistance from $V_{RT}$ to $V_{RB}$.
2. Not more than 7 codes outside ±0.5 LSB; no codes in excess of 0.75 LSB.

## APPLICATION NOTES

### Analog Input (Figs. 4 and 9)

The maximum amplitude and offset of the input is defined by the reference voltages ($V_{RB}$ to $V_{RT}$). The optimum input is 2V p-p with a DC offset of -1V.

Input buffering internal to the device results in an input capacitance of 35pF (typ). Gain, offset and low impedance drive can all be provided by the use of a high slew rate ADC driver such as the Plessey SL9999.

### Reference Pins (Figs. 8 and 9)

Between pin 41 ($V_{RT}$) and pin 23 ($V_{RB}$) there are 256 series resistors forming the reference chain. The total resistance may be between 90 and 120Ω. A mid reference pin 32 ($V_{RM}$) is also provided as an option for precision setting of integral linearity. Both $V_{RM}$ and $V_{RB}$ should be adequately decoupled to the analog GND. For optimum performance $V_{RT}$ is connected directly to analog GND and $V_{RB}$ is driven from a -2V DC supply. For precise reference setting this supply should be adjustable by ±0.2V.

### Clock Inputs CLK and $\overline{CLK}$ (Figs.3 and 5)

The Plessey SP97508 can be driven from both differential or single ended ECL clocks. In either mode the clock lines should be terminated with the lines characteristic impedance, close to the device clock pins. Clock signals can be improved by incorporating the Plessey SP92701 line receiver into the circuit, between the clock source and the SP97508.

Single ended drive can be simply provided by adding a 1nF chip or encapsulated chip capacitor from the $\overline{CLK}$ pin to DGND. The $\overline{CLK}$ pin will then self bias at -1.28V which is the mid threshold for ECL. The device can therefore be clocked by an ECL signal into the CLK input.

For full 100MHz operation a conventional unity mark space ratio clock can be used. The device will give optimum performance with ECL CLK input high for 7.5ns and low for 2.5ns.

### 8-Bit ECL Outputs (Figs. 7 and 9)

The outputs are standard ECL open emitters and therefore require pull-down resistors from the outputs to -5.2V or -2V digital supply. Single in-line resistors of value 500 to 1kΩ are recommended. The outputs are capable of driving 100Ω terminations to a -2V supply. For 50Ω applications the Plessey SP9210 can be incorporated.

### Output Coding (Table 1)

With pin 18 (MINV) and pin 3 (LINV) left open circuit, the device output will be coded in standard binary with the all 1s code corresponding to the most positive input. $V_{IN}$ = $V_{RT}$ = 0V. An inverse binary output can be provided by connecting both MINV and LINV to GND. 2s complement coding

(inverted MSB) can be provided by connecting only the MINV pin to GND and inverse 2s complement coding can be achieved by connecting only the LINV pin to GND.

### Timing (Fig.3)

The anlog input is acquired by the device shortly after the rising edge of the CLK signal. The internal latch causes a 1 cycle delay, hence the output data is valid one clock cycle after the acquisition of the analog signal.

The output data is further delayed by the CLK to output delay ($T_d$ = 2.5ns typ). This gives the advantage that the same timing and phase of the SP97508 CLK signal can be used to acquire the output data.

## CIRCUIT BOARD CONSTRUCTION

As with most PCB construction for analog-to-digital conversion, the best performance from the SP97508 can be achieved by separating the ground plane into two sections, analog GND, and digital GND. This aids the device performance by reducing the amount of digital switching noise fed back into the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which ideally should be terminated through a 680Ω load to the -5.2V digital supply, $DV_{EE}$.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. Therefore it is wise to decouple the SP97508 close to the device supply pins with good quality high frequency capacitors.

### Notes on Construction

1. Use split analog and digital ground planes connected together close to the device. Do not run the analog input next to the clock or data lines.
2. All NC pins must be grounded: connect pins 2 and 19 to DGND, all others to AGND.
3. Connect both digital and analog supplies together on the PCB at a point away from the device.
4. Use 10nF capacitors for supply decoupling.
5. Use strip-line techniques for signal paths greater than 5cm (2 inches).
6. Use a 47$\mu$F electrolytic capacitor to decouple the -5.2V $V_{EE}$ supply.

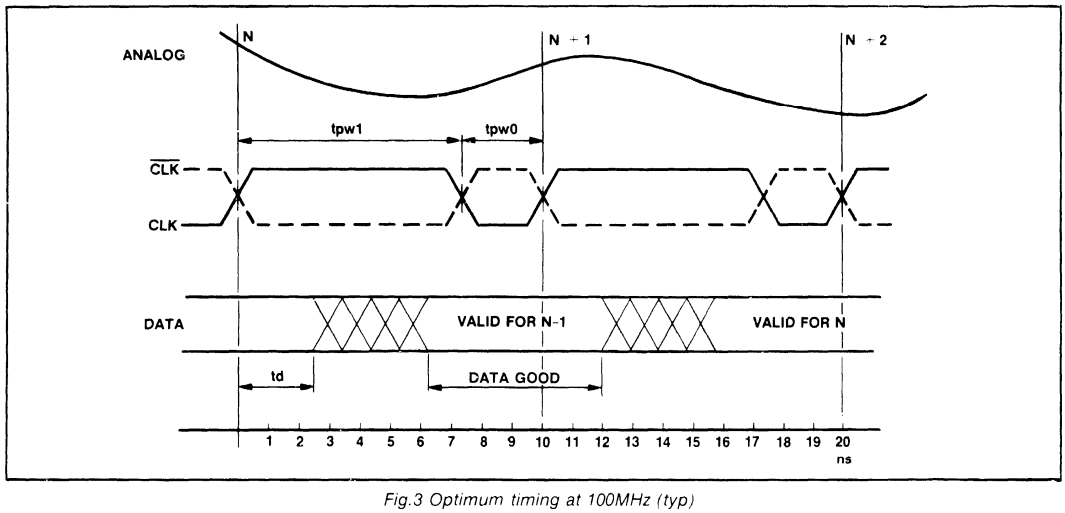



*Fig.3 Optimum timing at 100MHz (typ)*

| | | Binary | Inv '2s' Comp. | '2s' Comp. | Inv Binary |
|---|---|---|---|---|---|
| | MINV = LINV = | OPEN (0) OPEN (0) | OPEN (0) GND (1) | GND (1) OPEN (0) | GND (1) GND (1) |
| $V_{IN}$ | 0V | 111 11 | 100 00 | 011 11 | 000 00 |
| | | 111 10 | 100 01 | 011 10 | 000 01 |
| | | - | - | - | - |
| | | - | - | - | - |
| | | - | - | - | - |
| | | 100 00 | 111 11 | 000 00 | 011 11 |
| | | 011 11 | 000 00 | 111 11 | 100 00 |
| | | - | - | - | - |
| | | - | - | - | - |
| | | - | - | - | - |
| | | 000 01 | 011 10 | 100 01 | 111 10 |
| | -2V | 000 00 | 011 11 | 100 00 | 111 11 |

*Table 1*

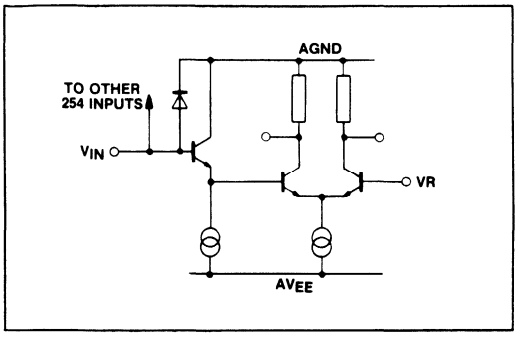



Fig.4 Analog input

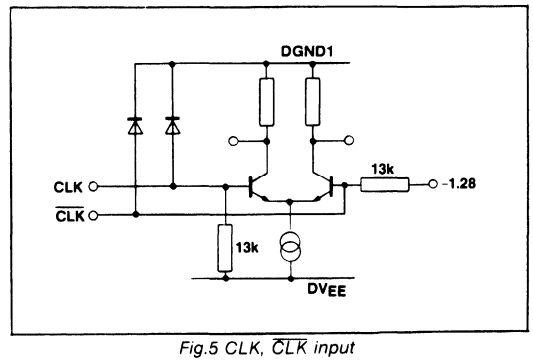



Fig.5 CLK, $\overline{CLK}$ input

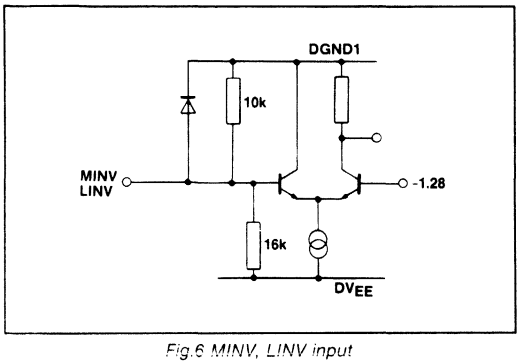



Fig.6 MINV, LINV input

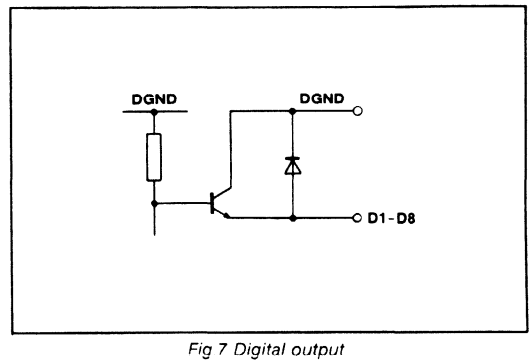



Fig 7 Digital output

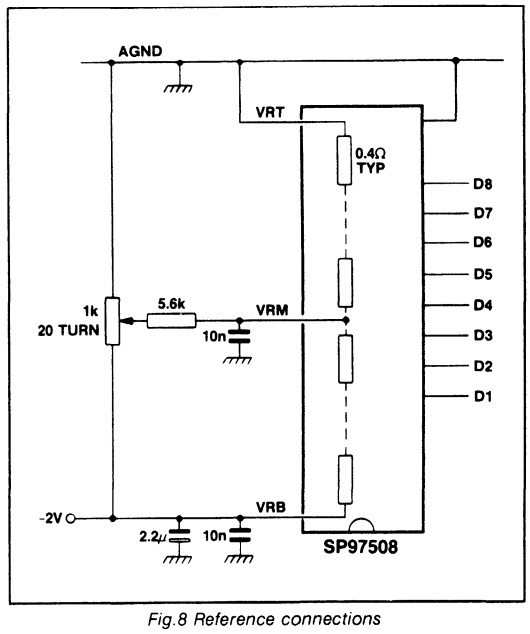



Fig.8 Reference connections

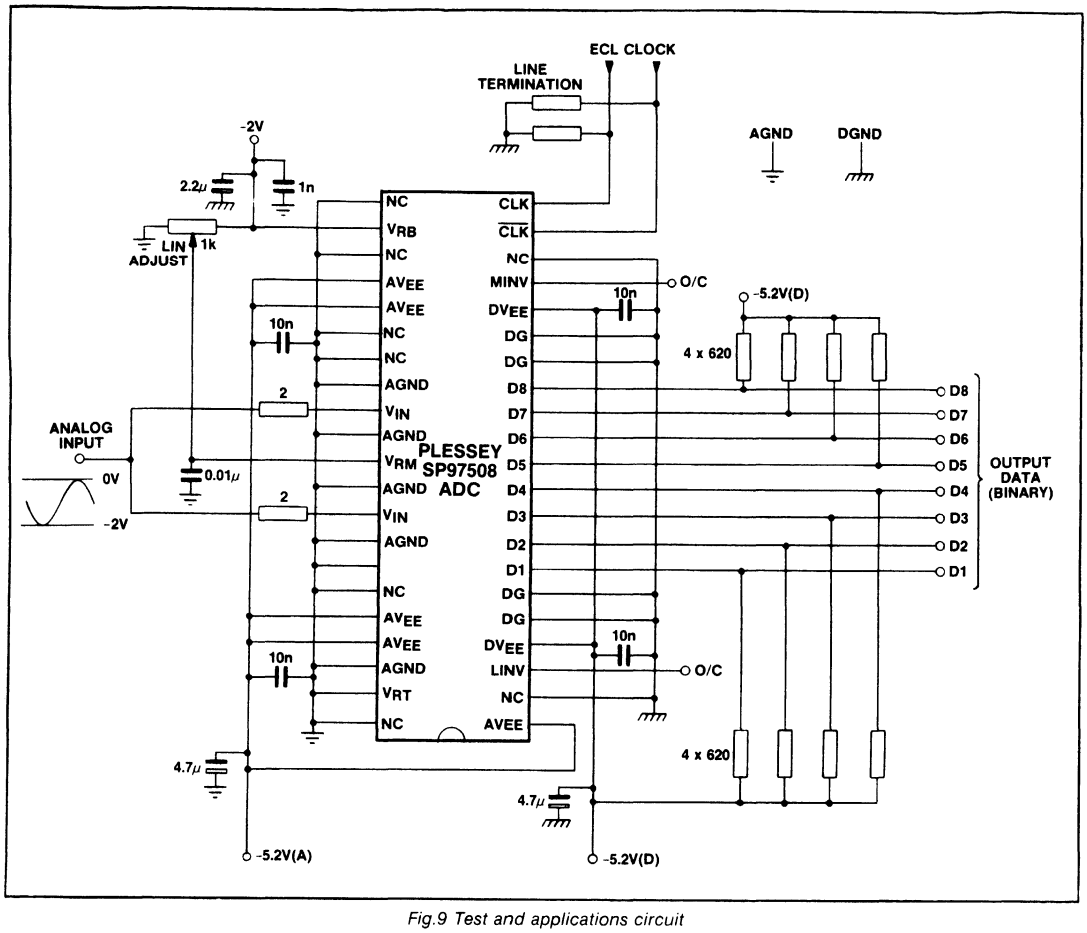



*Fig.9 Test and applications circuit*

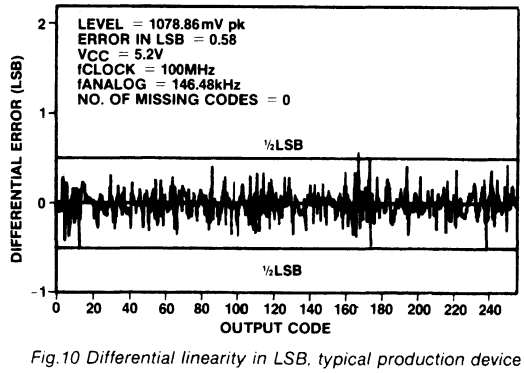



*Fig.10 Differential linearity in LSB, typical production device*

# SP97308E

## 30MHz ECL 8-BIT FLASH ADC

The Plessey SP97308E contains 255 high speed comparators which form a full flash analog to digital converter and requires no sample and hold.

Its wideband input allows singals with frequencies up to the Nyquist limit to be digitised with high accuracy, and an on-chip bandgap voltage reference gives low DC drift over a wide operating temperature range (-40°C to +125°C in DG package).

Also within the device is a full 8-bit D-type latch, which ensures that the 8 ECL outputs are accurately registered and have a good data valid time at high clock speeds. The output data can therefore be acquired with ease. The SP97308E is available in two variants: the SP97308E B has ±½ LSB differential linearity and the SP97308E C has ± LSB differential linearity, with a consequent cost advantage.

The ADC is designed for applications where power consumption is at a premium (500mW typ).

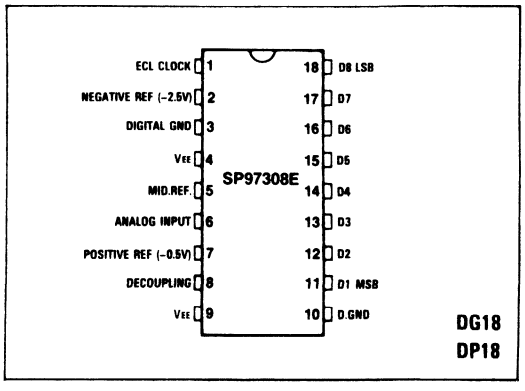



*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**SP97308E B DG** (Industrial - Ceramic DIL package)
**SP97308E C DP** (Industrial - Plastic DIL package)

### FEATURES

- High Speed: 30MHz (Typ.)
- Flash Converter No Sample and Hold Required
- Low Power Consumption (450mW Typ.)
- Latched ECL Compatible Outputs
- Band Gap for Good Temperature Stability
- Wide Operating Temperature Range
- Full Static Protection

### APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{EE}$ | 12V |
| Output current | 10mA |
| Input voltage | $V_{EE}$ |
| Storage temperature | -55°C to +175°C |
| Operating temperature | <150°C |

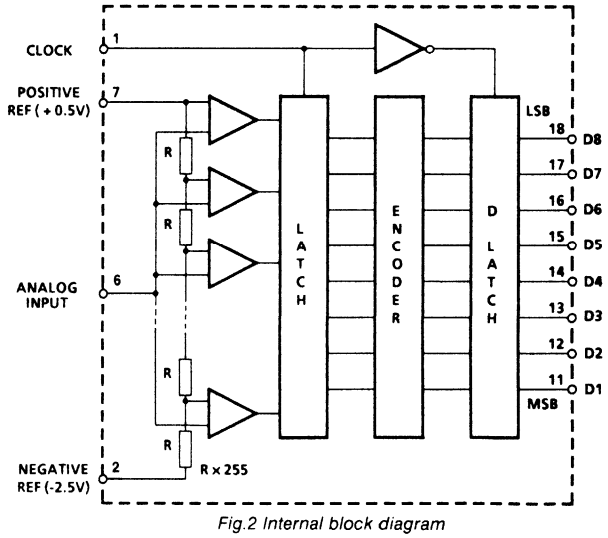



*Fig.2 Internal block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 0°C to 70°C, $V_{EE}$ = -5.2V ± 0.25V

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply current | $I_{EE}$ | | 100 | | mA | |
| Power consumption | | | 500 | 650 | mW | |
| Clock frequency | $f_C$ | 30 | | | MHz | ECL |
| Digital output level high | $V_H$ | -0.96 | | -0.81 | V | 1K load, 25°C |
| Digital output level low | $V_L$ | -1.85 | | -1.62 | V | 1K Load, 25°C |
| Reference chain resistance | Rr | | 390 | | Ω | |
| Analog input range | $V_{IN}$ | -2.5 | | -0.5 | V | |
| Analog input capacitance | $C_{IN}$ | | 25 | | pF | |
| Differential linearity | | | | ±0.5 | LSB | SP97308E B (DG package) |
| Integral linearity | | | | ±1.0 | LSB | SP97308E B (DG package) |
| Differential linearity | | | | ±1.0 | LSB | SP97308E C (DG package) |
| Integral linearity | | | | ±1.0 | LSB | SP97308E C (DG package) |
| Aperture uncertainty | | | 25 | | ps | |
| Aperture delay | $t_A$ | | 1 | | ns | |
| Data valid time | $t_V$ | 40 | 45 | | ns | 20MHz clock |
| Clock to output propagation delay | $t_{pd}$ | | | 8 | ns | After ½ cycle delay |
| Differential gain | | | 1 | | % | |
| Differential phase | | | 1 | | Deg | |

## THERMAL CHARACTERISTICS

SP97308EB $\theta JA$ = 92°C/W $\theta JC$ = 21°C/W
SP97308EC $\theta JA$ = 75°C/W $\theta JC$ = 20°C/W

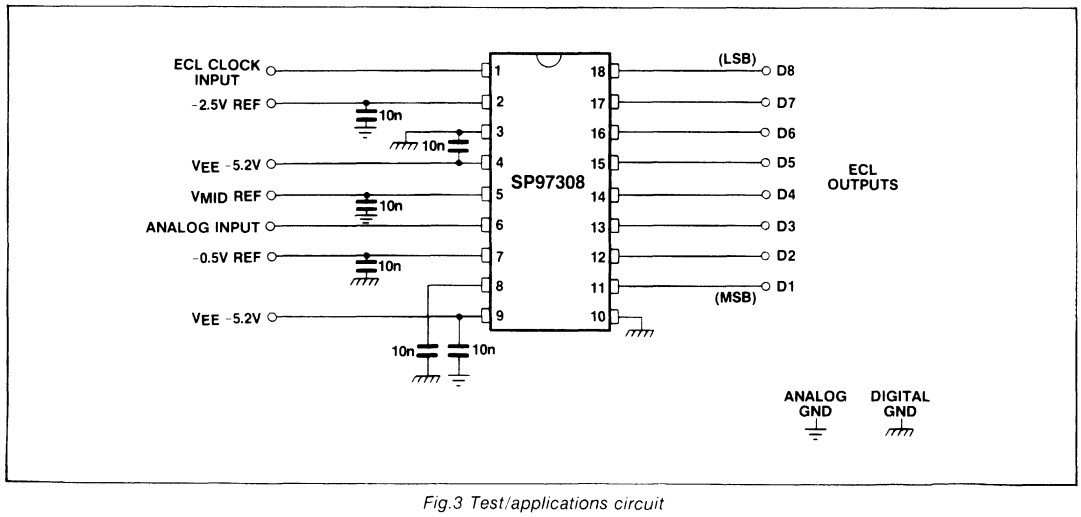



*Fig.3 Test/applications circuit*

## OPERATING NOTES

The SP97308E ADC will operate at frequencies up to and above 30MHz. It is therefore necessary to take care with the ground plane and component placement around the device.

Split analog and digital grounds with good decoupling close to the device pins, will reduce digital to analog crosstalk and hence aid performance. The voltage between $A_{GND}$ and $D_{GND}$ should not be >±50mV.

The optimum differential linearity is achieved using the widest possible reference voltage. Therefore standard applications should use -0.5V on pin 7 and -2.5V on pin 2.

The optimum input signal for use with these recommended reference voltages is 2V p-p biased at -1.5V.

For optimum performance the tolerance on the reference inputs is ±0.1V and on the supplies the tolerance is ±0.25V.

The Plessey SL9999 is a suitable op-amp/ADC driver to provide this offset and drive the SP97308E input at high speed.

The digital outputs can drive 100Ω loads to -2V (or Thevenin equivalent).

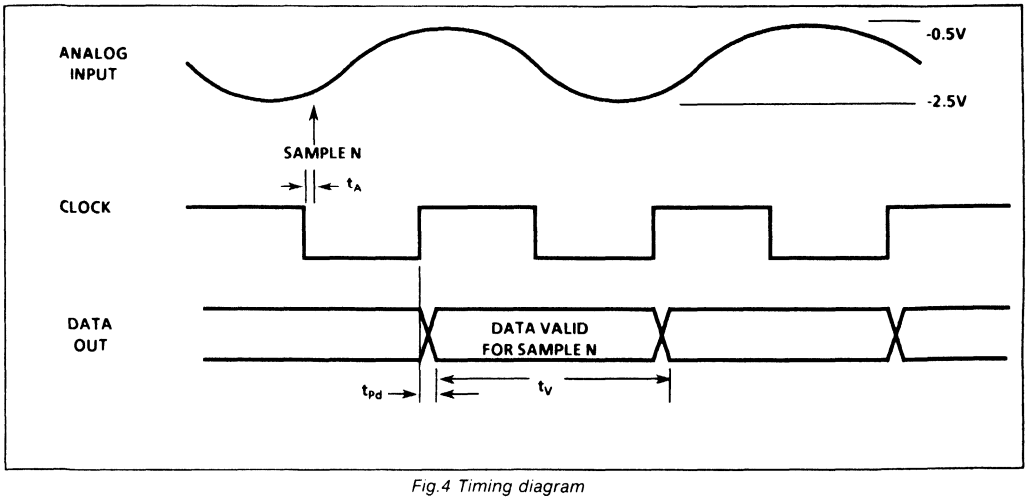



*Fig.4 Timing diagram*

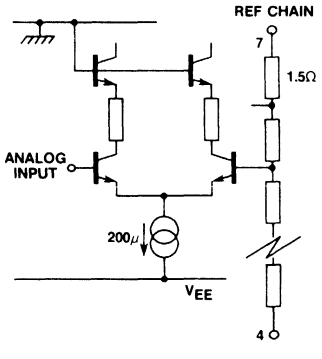



*Fig.5a One of 255 analog inputs connected to pin 8*

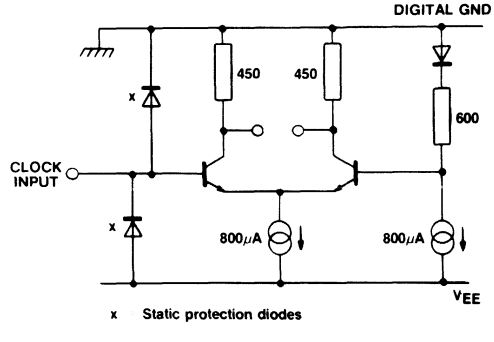



*Fig.5b Clock input*

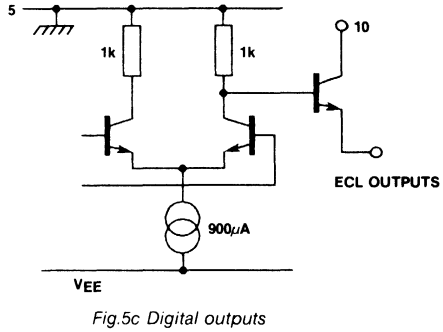



*Fig.5c Digital outputs*

*Fig.5 Input/output internal circuits*

# SP97308T

## 30MHz TTL/CMOS 8-BIT FLASH ADC

The Plessey SP97308T contains 255 high speed comparators which form a full flash analog to digital converter and requires no sample and hold.

Its wideband input allows singals with frequencies up to the Nyquist limit to be digitised with high accuracy, and an on-chip bandgap voltage reference gives low DC drift over a wide operating temperature range (-40°C to +125°C in DG package).

Also within the device is a full 8-bit D-type latch, which ensures that the 8 TTL/CMOS outputs are accurately registered and have a good data valid time at high clock speeds. The output data can therefore be acquired with ease.

The SP97308T is available in two variants: the SP97308TB has ±½ LSB differential linearity and the SP97308TC has ± LSB differential linearity, with a consequent cost advantage.

The ADC is designed for applications where power consumption is at a premium (500mW typ).

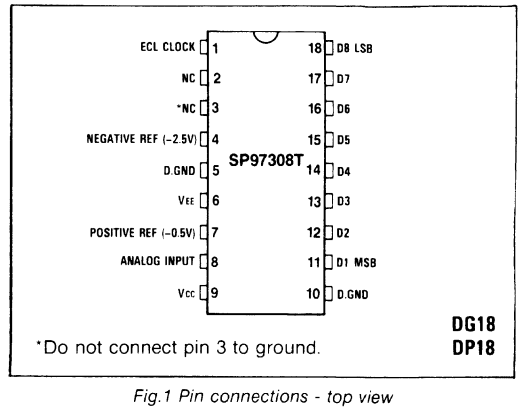



*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**SP97308T B DG** (Industrial - Ceramic DIL package)
**SP97308T C DP** (Industrial - Plastic DIL package)

### FEATURES

- High Speed: 30MHz Guaranteed
- Flash Converter, No Sample and Hold Required
- Low Power Consumption (500mW Typ.)
- Latched TTL/CMOS Compatible Outputs
- Band Gap for Good Temperature Stability
- Wide Operating Temperature Range
- Full Static Protection

### APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}-V_{EE}$ | 12V |
| Output current | 10mA |
| Input voltage | $V_{CC}$ to $V_{EE}$ |
| Storage temperature | -55°C to +175°C |
| Operating temperature | <150°C |

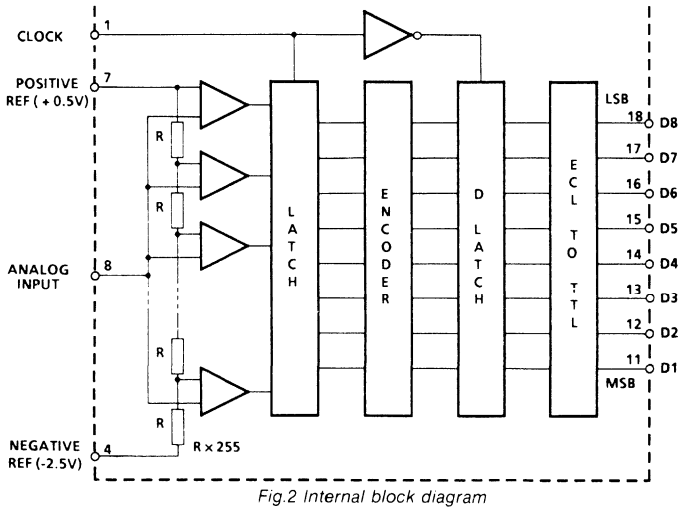



*Fig.2 Internal block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 0°C to 70°C, $V_{CC}$ = +5V ± 0.25V, $V_{EE}$ = -5.2V ± 0.25V

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 10 | | mA | |
| Negative supply current | $I_{EE}$ | | 85 | | mA | |
| Power consumption | | | 500 | 600 | mW | |
| Clock frequency | $f_C$ | 30 | | | MHz | ECL (-1.3V trip level) |
| Digital output level high | $V_H$ | 3.5 | 4.3 | | V | One TTL load. Fig.5 |
| Digital output level low | $V_L$ | | 0.3 | 0.4 | V | One TTL load. Fig.5 |
| Reference chain resistance | Rr | | 390 | | Ω | |
| Analog input range | $V_{IN}$ | -2.5 | | -0.5 | V | |
| Analog input capacitance | $C_{IN}$ | | 25 | | pF | |
| Differential linearity | | | | ±0.5 | LSB | SP97308TB (DG package) |
| Integral linearity | | | | ±1.0 | LSB | SP97308TB (DG package) |
| Differential linearity | | | | ±1.0 | LSB | SP97308TC (DP package) |
| Integral linearity | | | | ±1.0 | LSB | SP97308TC (DP package) |
| Aperture uncertainty | | | 25 | | ps | |
| Aperture delay | $t_A$ | | 1 | | ns | |
| Data valid time | $t_V$ | 40 | 45 | | ns | 20MHz clock |
| Clock to output propagation delay | $t_{pd}$ | | | 10 | ns | After ½ cycle delay |
| Differential gain | | | 1 | | % | |
| Differential phase | | | 1 | | Deg | |

## THERMAL CHARACTERISTICS

SP97308TB $\theta JA$ = 92°C/W
$\theta Jc$ = 21°C/W
SP97308TC $\theta JA$ = 75°C/W
$\theta Jc$ = 20°C/W

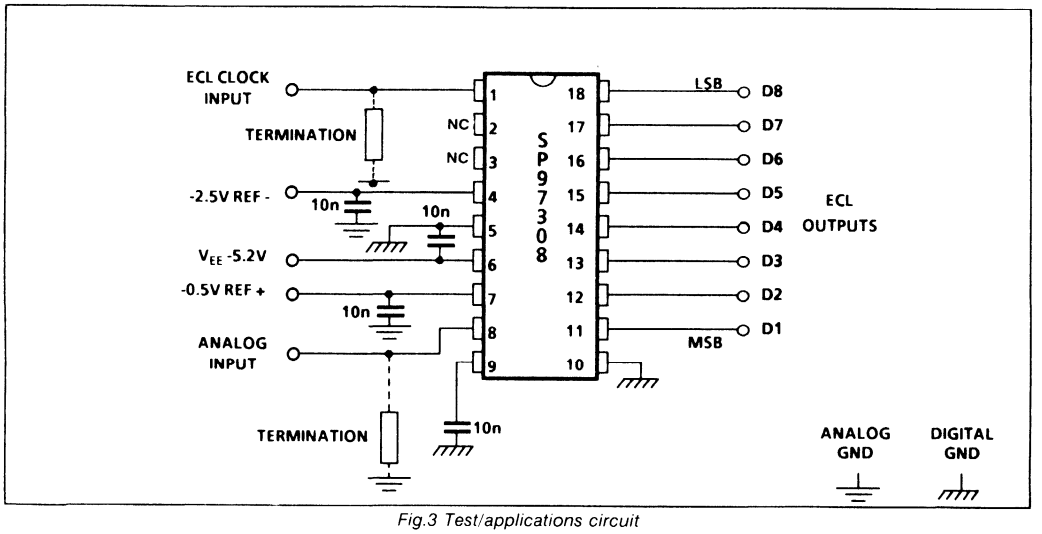



*Fig.3 Test/applications circuit*

## OPERATING NOTES

The SP97308T ADC will operate at frequencies up to and above 30MHz. It is therefore necessary to take care with the ground plane and component placement around the device.

Split analog and digital grounds with good decoupling close to the device pins, will reduce digital to analog crosstalk and hence aid performance.

The optimum differential linearity is achieved using the widest possible reference voltage. Therefore standard applications should use -0.5V on pin 7 and -2.5V on pin 4.

The optimum input signal for use with these recommended reference voltages is 2V p-p biased at -1.5V.

The Plessey SL9999 is a suitable op-amp/ADC driver to provide this offset and drive the SP97308T input at high speed.

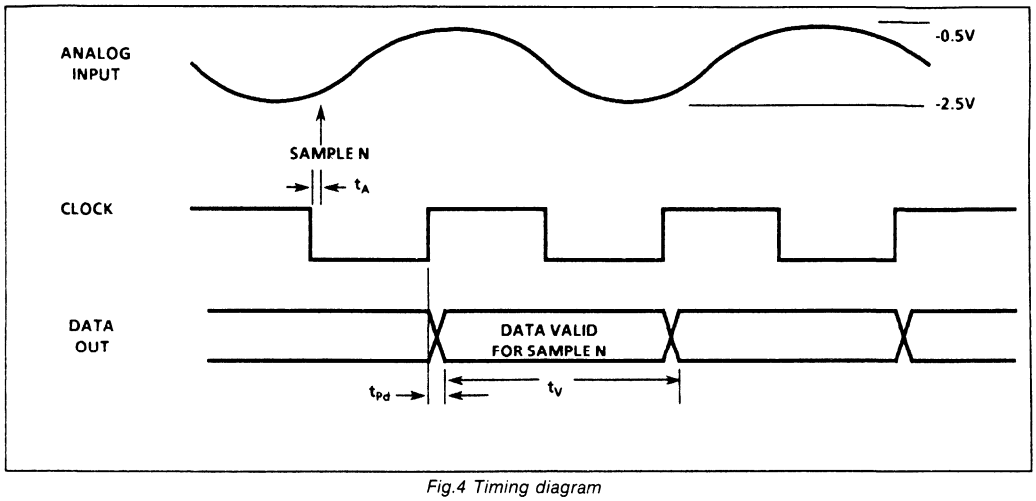



*Fig.4 Timing diagram*

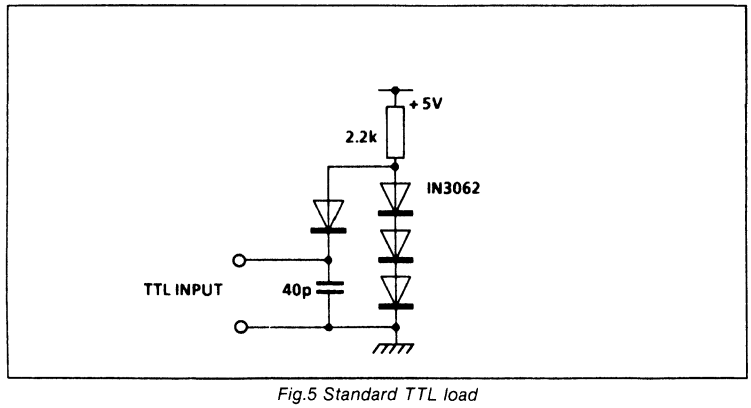



*Fig.5 Standard TTL load*

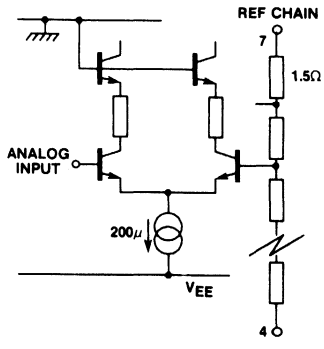



Fig.6a One of 255 analog inputs connected to pin 8

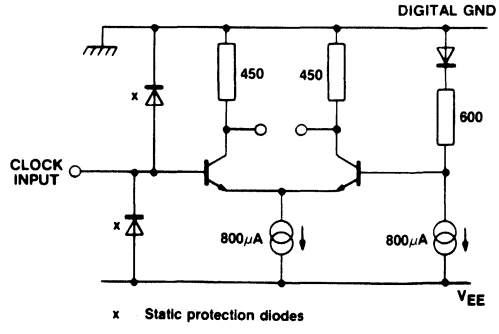



Fig.6b Clock input

Fig.6 Internal circuits

# SP94308

## 8-BIT VIDEO SYSTEM ADC

The Plessey SP94308 analog to digital converter has been specially designed for use with NTSC or PAL video signals.

A 1V video signal is AC coupled to the device input, where it is DC clamped, amplified by two and fed through a buffer which drives the ADC input capacitance.

A sync or burst gate pulse can be used to drive the DC clamp circuit. This circuit can be externally adjusted to provide conversion of video only or video and sync.

This analog to digital converter samples the input waveform on the rising edge of the clock and produces a latched output which can be acquired simply by inverted clock signal.

Also within the SP94308 is an internal clock amplifier and driver. This allows a low level clock signal to be AC coupled directly into the device for applications that may be sensitive to clock radiation.

The clock frequency and analog bandwidth of the SP94308 are compatible with both PAL and NTSC standards where conversion of luma or full composite video signals are required.

### FEATURES

- 8 Bits, 18MHz
- ±0.75 LSB Differential Linearity (Typ.)
- No Sample and Hold or Input Buffer Required
- Internal Clock Amplifier
- Internal Clamp Circuit
- Internal Output Latch
- 6MHz Min. Analog Bandwidth
- Output Levels are TTL/CMOS Compatible
- 0°C to 70°C Temperature Range
- Full Static Protection
- On Chip ×2 Amplifier and ADC Buffer

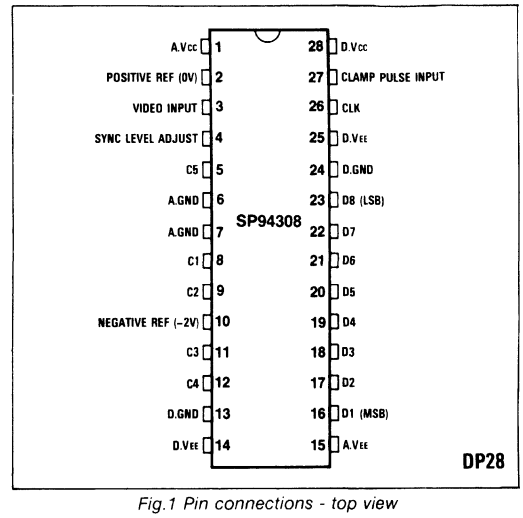



*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**SP94308 DP** (Industrial - Plastic DIL package)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$-$V_{EE}$ | <12V |
| Output current | <20mA |
| Storage temperature | -65°C to +150°C |
| Junction operating temperature | <150°C |

### THERMAL INFORMATION

Chip to ambient temperature $\theta_{JA}$ = 55°C/W

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = 0°C to 70°C, $V_{CC}$ = +5V ± 0.25V, $V_{EE}$ = -5.2V ± 0.25V

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 35 | 44 | mA | |
| Negative supply current | $I_{EE}$ | | 110 | 150 | mA | |
| Power consumption | | | 750 | | mW | |
| Resolution | | 8 | | | Bits | |
| Reference current | $I_{ref}$ | | 7 | 12 | mA | $V_{ref}$ = -2V |
| Maximum clock rate | $f_C$ | 18 | | | MHz | |
| Clock input level | | 0.25 | | 1.0 | V p-p | AC coupled |
| Analog bandwidth | $f_a$ | 6 | | | MHz | |
| Input impedance | $R_{IN}$ | 100K | | | Ω | |
| Differential linearity | | | ±0.75 | ±1.0 | LSB | 25°C |
| Integral linearity | | | | ±1.0 | LSB | 25°C |
| Differential gain | | | | 1.5 | % | $f_C$ = 13.3MHz |
| Differential phase | | | 1 | | Deg | |
| Logic '1' | $V_{IH}$ | $V_{CC}$-1.3 | $V_{CC}$-1 | | V | $I_{source}$ = 1mA |
| | $V_{IH}$ | $V_{CC}$-1.1 | $V_{CC}$-0.9 | | V | $I_{source}$ = 0.1mA |
| Logic '0' | $V_{OL}$ | | 0.3 | 0.4 | V | $I_{sink}$ = 1.6mA (Note 1) |
| Tilt/line | | | -1.5 | | mV | 100nF input capacitor |
| Input level | | | 1 | | V p-p | AC coupled |
| Sync level adjust output | | | -1.4 | | V | Unadjusted (Note 2) |
| Data valid time | $t_V$ | | 45 | | ns | At 20MHz clock |

NOTES
1. Gain of ×2 in input stage.
2. See Fig.7 for equivalent TTL load.

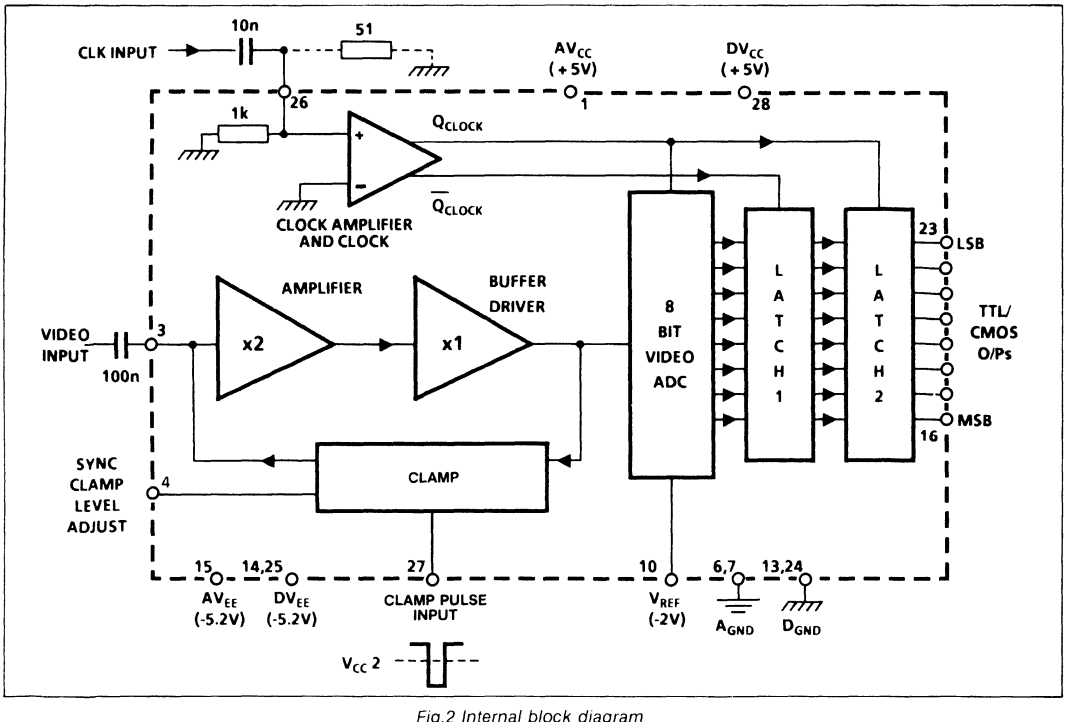



*Fig.2 Internal block diagram*

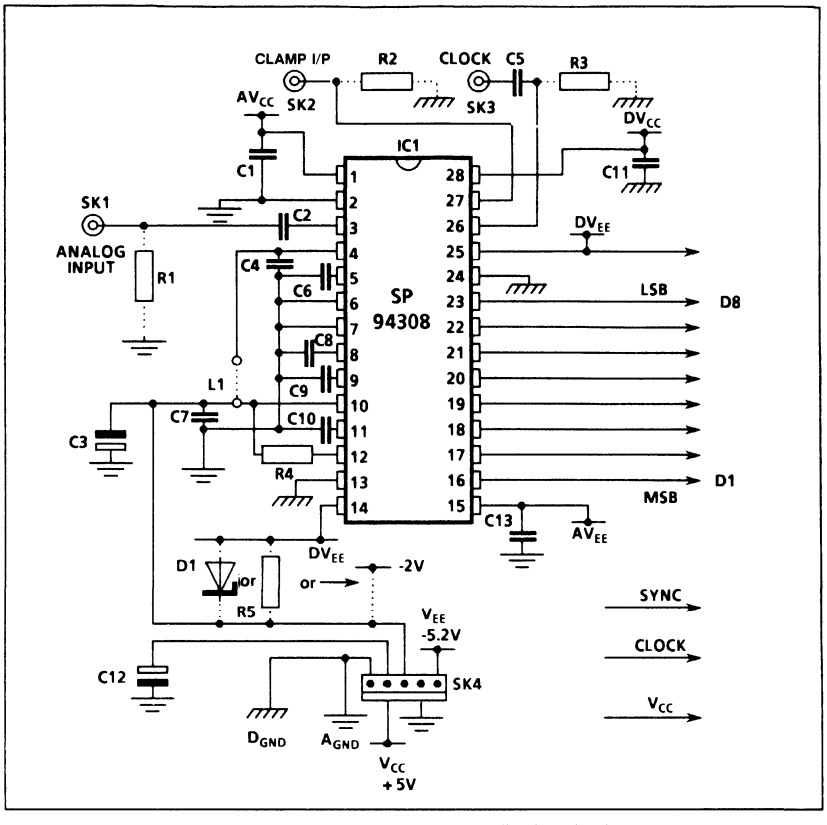



*Fig.3 Minimum component application circuit*

## COMPONENT LIST FOR FIG.4

### Resistors

| | |
|---|---|
| **R1** | 75Ω (optional termination) |
| **R2** | 47Ω (optional termination) |
| **R3** | 47Ω (optional termination) |
| **R4** | 130K (accuracy trim) |
| **R5** | Approx. 560Ω (optional) |

### Semiconductors

| | |
|---|---|
| **IC1** | SP94308 |
| **D1** | BZX79C3V0 (optional) |

### Sockets

| | |
|---|---|
| **S1-S3** | Sub Vis sockets (optional) |
| **S4** | KK Molex socket (optional) |

### Capacitors for ADC, clamp, bias etc.

| | |
|---|---|
| **C1** | 100nF (optional decoupling) |
| **C2** | 100nF (input coupling and line clamp) |
| **C3** | 47μF (electrolytic decoupling) |
| **C4** | 100nF (optional decoupling) |
| **C5** | 100nF (coupling) |
| **C6** | 27pF at 20MHz or 47pF at 10MHz clock |
| **C7** | 100nF (decoupling) |
| **C8** | 100nF (decoupling) |
| **C9** | 100nF (decoupling) |
| **C10** | 100nF (decoupling) |
| **C11** | 100nF (optional decoupling) |
| **C12** | 47μF (electrolytic decoupling) |
| **C13** | 100nF (optional decoupling) |

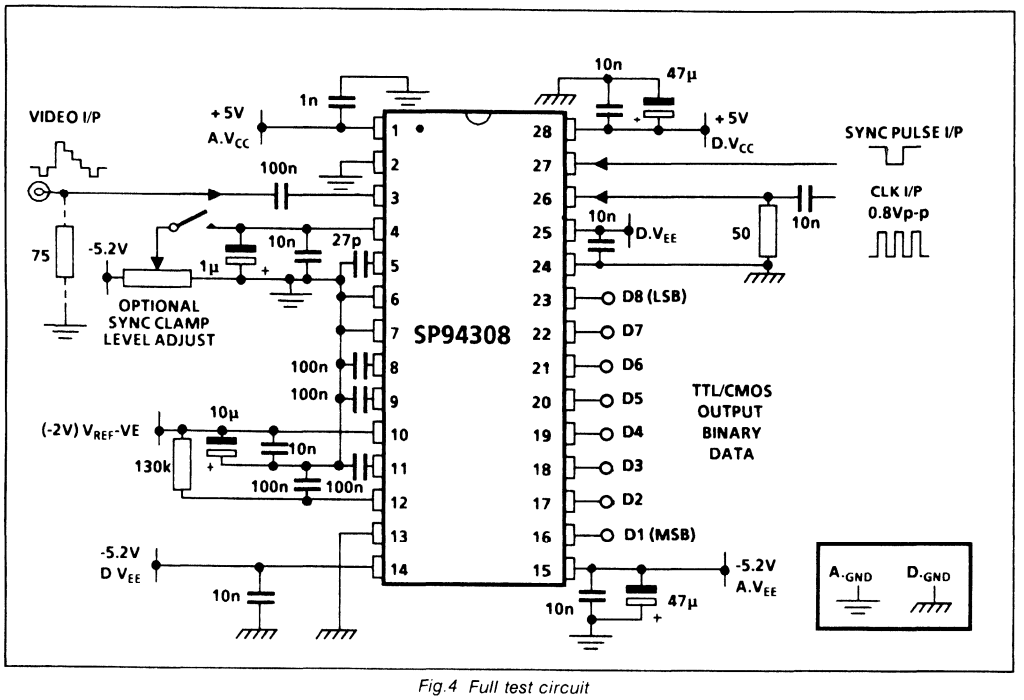



*Fig.4 Full test circuit*

## APPLICATIONS

The SP94308 combines a clamp circuit, sample and hold, x2 amplifier, ADC driver, video ADC and output latch that form a conventional 8-bit video digitising system.

An on-chip clock amplifier allows the device to be clocked from low level sine or square wave signals. This reduces the possibility of patterning due to crosstalk.

The device offers the flexibility for either sync clamping or black level clamping of the video signal.

### Sync Clamp

Sync clamping is provided by applying a negative going clamp pulse to pin 27 during the sync period. This pulse should be more than 1.5µs wide and it should cross the internal switching threshold of $V_{CC}2$. Pin 4 should be connected to $V_{REF}$ (pin 10 -2V) to allow the total video with its sync to be digitised.

### Black Level Clamping

This can be achieved by applying a negative clamp pulse to pin 27 within the back porch of the video signal. The clamp pulse should avoid the colour burst - this ensures no attenuation of the burst signal.

The clamping pulse can be derived from a burst gate pulse or by delaying the sync pulse with a dual monostable (SN74123N).

When using a back porch clamping pulse, pin 4 should be decoupled to analog ground using a 100nF capacitor. The device will then self-bias this pin to -1.4V. This provides full digitisation of the video and its sync.

It is also possible to adjust the voltage on pin 4 and reduce the reference voltage pin 10 to provide digitisation of the active video information only.

If a clamp pulse is not readily available within the application it can be generated from the incoming video signal (see circuit shown in Fig.5). The variable resistor RV can be adjusted for different slice levels of the incoming video sync.

The digital outputs of the SP94308 are latched and have a 90% of CLK, data valid time at 20MHz. This allows the 8-Bit TTL output to be acquired simply by an inverse CLK signal. See Fig.6.

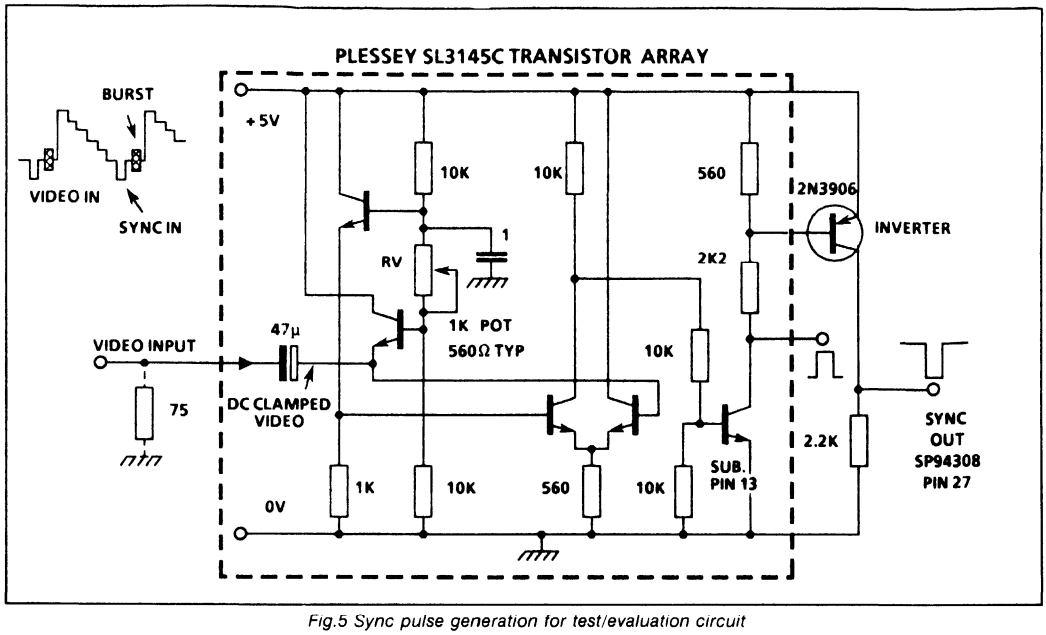



*Fig.5 Sync pulse generation for test/evaluation circuit*

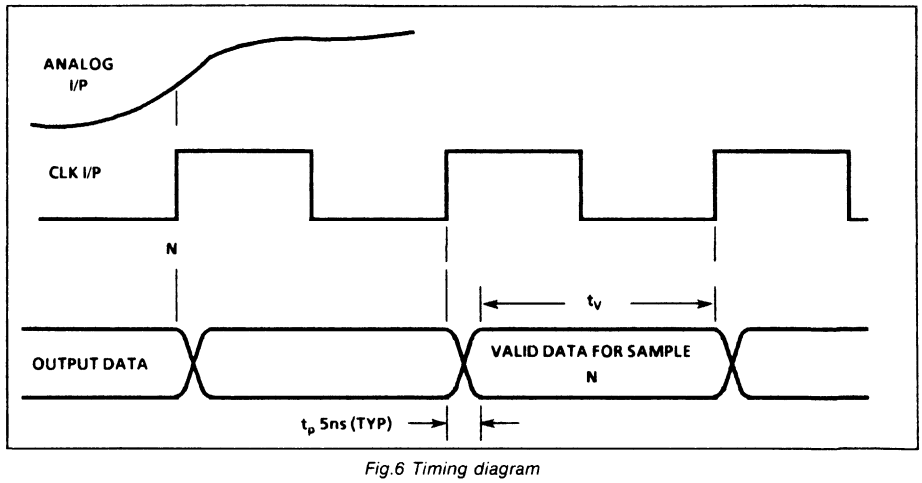



*Fig.6 Timing diagram*

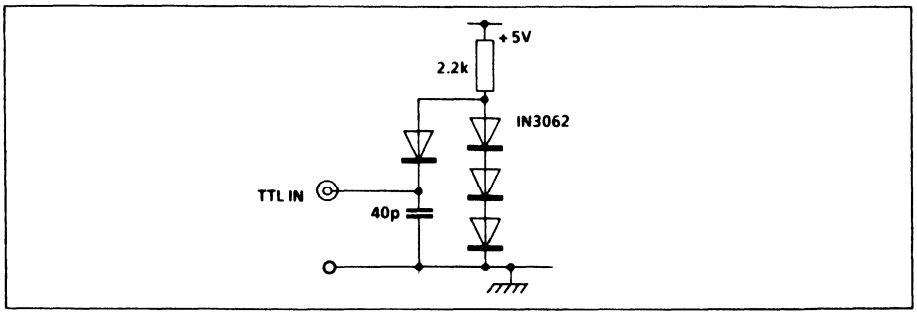



*Fig.7 Equivalent TTL load*

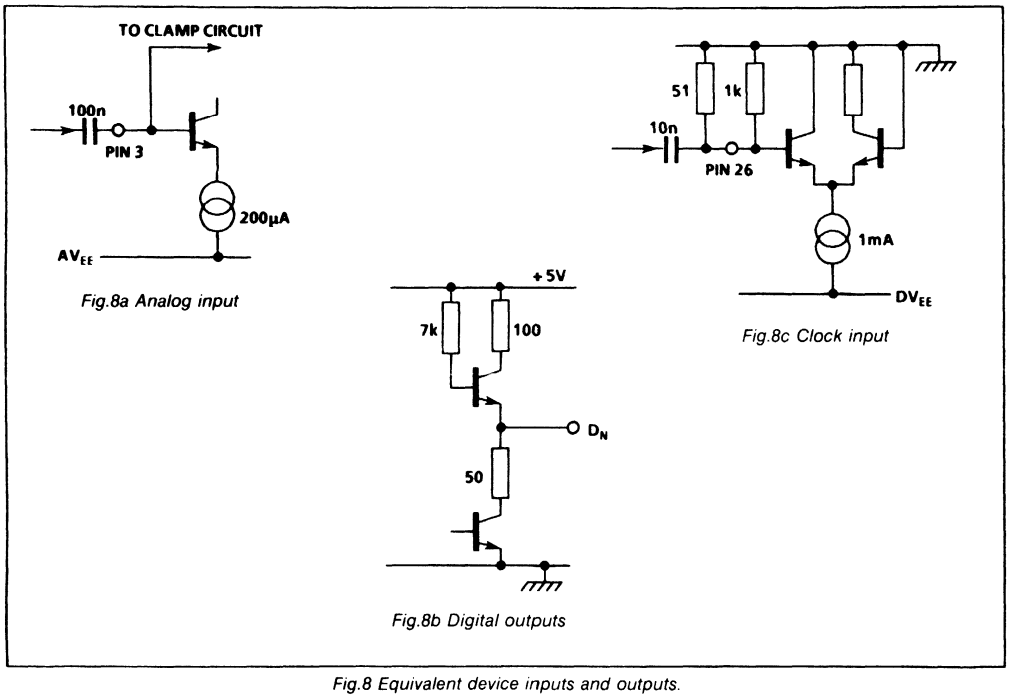



*Fig.8a Analog input*

*Fig.8b Digital outputs*

*Fig.8c Clock input*

*Fig.8 Equivalent device inputs and outputs.*

# SP9756

## 6-BIT HIGH SPEED, HIGH ACCURACY ADC

The Plessey SP9756 is a 6-bit flash ECL analog-to-digital converter. It incorporates 64 individual comparators, a clock driver circuit, reference chain and a D-type output latch. This flash ADC is capable of sampling in excess of 110MHz, with a wide analog bandwidth and good dynamic performance.

A choice of accuracy is available: the accuracy of the SP9756-8 is typically ±⅛ LSB at 2V input and therefore it is ideally suited for use in systems that incorporate expansion to higher resolutions. Alternatively the SP9756-6 is guaranteed to be accurate to ±½ LSB for inputs between 1V and 2V in cost conscious designs.

### FEATURES

- ±½ or ±⅛ LSB Accuracy (-6 and -8 versions)
- Monotonic over the Full Frequency Range
- 110MHz Conversion Rate (130MHz Typ.)
- 250MHz Full Power Bandwidth (To -3dB) at 1V Input
- 50MHz Bandwidth with typically ±½ LSB Accuracy
- Operates on a Single -5.2V Supply
- Internally Latched 6-Bit ECL Outputs (7ns Minimum Valid Data at 100MHz)
- Operating Temperture Range:
  -40°C to +85°C Industrial
  -55°C to +125°C Military
- On-Chip Band-Gap Reference for Good Temperature Stability
- Internal Clock Buffer
- No External Sample and Hold Needed
- On-Chip Reference Chain
- Sense Outputs for Precise Setting of Reference Voltages
- Mode Input to Program Over-Range Condition
- Low Propagation Delay (3ns Typ.)

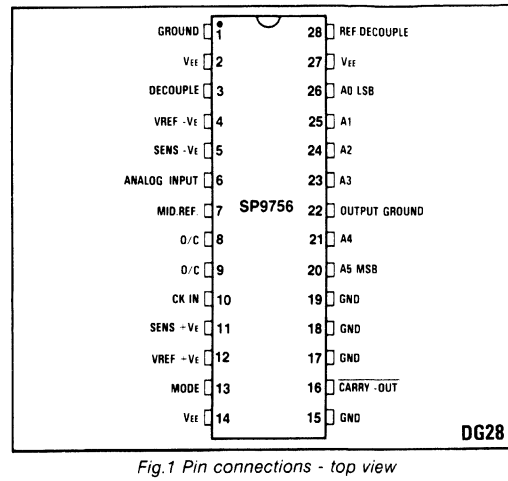



*Fig.1 Pin connections - top view*

### APPLICATIONS

- Instrumentation
- Nucleonics Research
- Radar Video Digitising
- Medical Electronics

### ORDERING INFORMATION

**SP9756-6 DG** (Industrial - Ceramic DIL package)
**SP9756-8 DG** (Industrial - Ceramic DIL package)
**SP9756-8AC DG** (Military - Ceramic DIL package)
NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

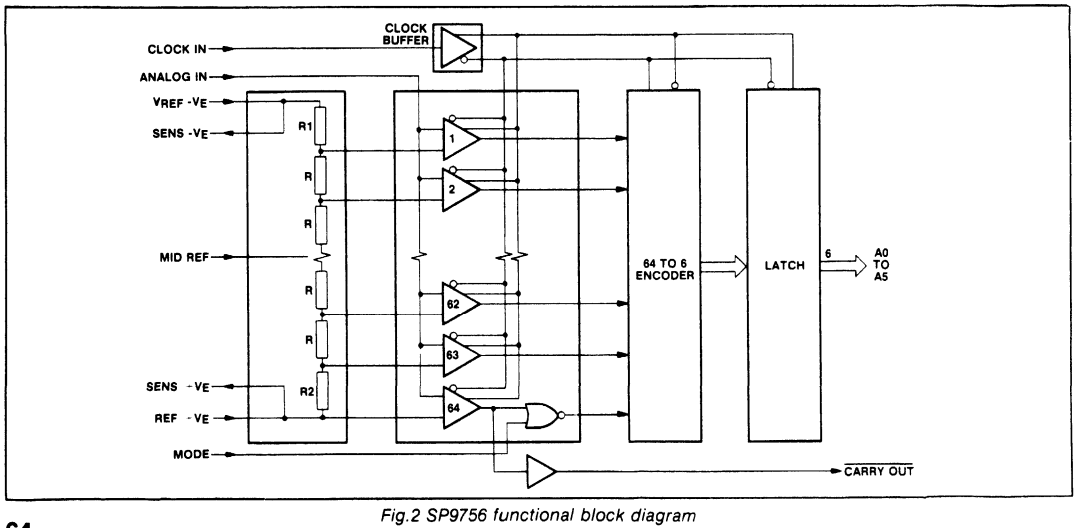



*Fig.2 SP9756 functional block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = +25°C, $V_{EE}$ = -5.2V ± 0.25V

| Characteristic | Pin | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply current, $I_{EE}$ | | | -170 | -250 | mA | Excludes ECL O/P & ref. currents |
| Supply voltage, $V_{EE}$ | 2 | -4.5 | | -5.5 | V | |
| Dynamic range | | | | 2.20 | V | Degrades below -30°C ($V_{EE}$ = -5.20V) |
| Analog input capacitance | | | 22 | | pF | |
| Analog input current | | | | 2.2 | mA | |
| Minimum reference bit size | | | 8 | | mV | |
| Power dissipation | | | 1.2 | 1.7 | W | Outputs loaded |
| Differential linearity SP9756-8 | | | | | | |
| at 7kHz input | | | ±0.125 | ±0.188 | LSB | 2V p-p input, 100MHz clock, measured using histogram test. See Figs.7 to 9 and reference 1 measurement techniques. |
| at 50MHz input | | | ±0.5 | | LSB | |
| Integral linearity SP9756-8 | | | | | | |
| at 7kHz input | | | | ±0.25 | LSB | |
| at 50MHz input | | | ±0.5 | | LSB | |
| Differential linearity SP9756-6 | | | | | | |
| at 7kHz input | | | | ±0.5 | LSB | 1V p-p input, 100MHz clock, measured using histogram test. See Figs.10 and 11 and reference 1 measurement techniques. |
| at 50MHz input | | | | ±0.75 | LSB | |
| Integral linearity SP9756-6 | | | | | | |
| at 7kHz input | | | | ±0.5 | LSB | |
| at 50MHz input | | | | ±0.5 | LSB | |
| Aperture jitter | | | 25 | | ps | |
| Full power 3dB bandwidth | | | 250 | | MHz | |
| S/N rato (RMS) at 50MHz analog, 101MHz sample rate | | 32 | | | dB | |
| Data out $A_0$ to $A_5$ | 20-21, 2326 | | | | | |
| O/P $V_{HIGH}$ | | | -0.9 | | V | |
| O/P $V_{LOW}$ | | | -1.8 | | V | |
| $R_{Chain}$ | 3,12 | | 25 | | Ω | |
| $V_{mode}$ High | 13 | -50 | | +100 | mV | All zero's over-range |
| $V_{mode}$ Low | 13 | -3.5 | | -0.500 | V | All one's over-range |
| Sample rate | 10 | 110 | 130 | | MHz | No missing codes |
| $T_{data}$ | | 7 | | | ns | |
| $T_{prop}$ | | | 3 | | ns | |
| $t_1$ | | | | 1.5 | ns | |
| $t_{sto}$ | | | 1.2 | | ns | |
| $t_{co}$ | | | 2.0 | | ns | |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Clock & Mode input | 0V to -3.5V |
| Supply voltage | -7V |
| Maximum junction temperature | 175°C |
| Storage temperature range | -55°C to +150°C |
| Thermal characteristics:- | |
| $\theta_{JA}$ | 40 deg C/W (typ) |
| $\theta_{JC}$ | 15 deg C/W (typ) |
| $T_{amb}$ | -40°C to +70°C (still air) |
| $T_{amb}$ | -55°C to +125°C (in 500LFPM of air across package) |

## OPERATING NOTES

### Analog Input

The input voltage range is 0.0V to -2.2V. Optimum performance is achieved with an input of 2V p-p i.e. DC offset to -1.0V for symmetrical limiting. At temperatures below -30° C this input range may degrade to 1.8V p-p.

The input capacitance is of the order of 22pF therefore the source impedance should be low. The device is specified using an input drive from a 50Ω generator into a 50Ω termination resistor, i.e. 25Ω looking out of the device. This 25Ω source impedance should be considered as a maximum.

### Reference Voltage

For optimum performance REF +VE (pin 12) should be connected to 0V (analog GND) and REF -VE (pin 4) to -2V supply. This supply should be decoupled with a good quality, high frequency capacitor to the analog GND. The minimum voltage across the reference is 0.5V, below this the linearity of the device will be adversely affected.

An input signal above $V_{REF}$ +VE will give an 'all ones' output provided that pin 13 is connected to a -2V supply (see mode input).

Sense pins (SENS +VE, pin 11 and SENS -VE, pin 5) are available on both REF +VE and REF -VE. These allow Kelvin applied voltages to be used for precision setting of the reference chain.

The reference chain can be used dynamically for applications using ACG on non-linear coding (see Fig.6).

### Clock Input

As the SP9756 features an internal differential clock driver, a single ended ECL clock signal is suitable.

The aperature uncertainty of the device is in the order of 25ps, therefore the clock signal should have low edge jitter to be compatible.

### Clock Timing

The first sample of the analog input is taken approximately 1.2ns after the rising edge of the clock. The input comparators then latch, holding their state until the falling edge.

When the SP9756 receives the first falling edge the device commences decoding and the input comparators are released. The binary data becomes available at the outputs 3.5ns after the second rising edge of the clock.

The SP9756 incorporates an output D-type latch. The data out from this latch is valid for over 70% of the clock cycle, at 100MHz. This greatly simplifies data acquisition of the binary information, as timing is not so critical as with many other ADCs.

### Mode Input

The MODE input (pin 13) selects the output code when $V_{IN}$ is higher than REF +VE. For normal operation this pin should be connected to -2V. The SP9756 will then give an all ones output for any input greater than REF +VE. If the mode input is tied to GND the device will give all zeros when the input is higher than REF +VE.

The mode pin must not be left open circuit.

## CIRCUIT BOARD LAYOUT

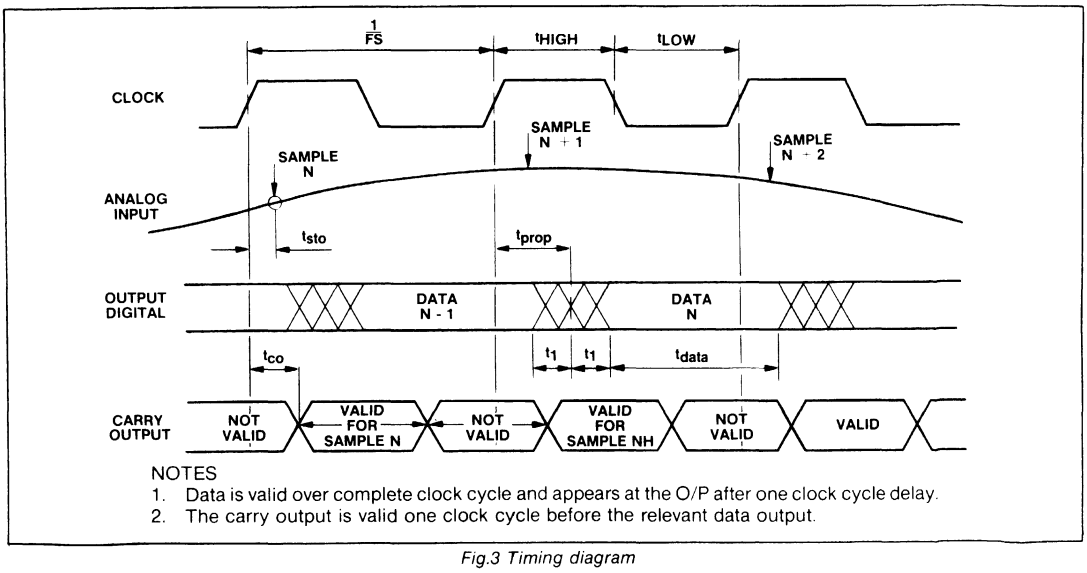
As with most PCB layouts for analog-to-digital conversion, the best performance from the SP9756 can be achieved by separating the ground plane into two sections, analog GND, and digital GND. This aids the device performance by reducing the amount of digital switching noise fed back into the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which ideally should be terminated through a 100Ω load to a -2V supply.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. Therefore it is wise to decouple the SP9756 close to the device supply pins with good quality high frequency capacitors. It is also advisable to direct the current returned from the output load towards pin 22 and away from other digital grounds. One way of achieving this is by creating a second digital ground plane which should connect to the main digital ground at pin 22 of the device, the ground connection between the ADC and the device acquiring the data is then made to this second digital ground plane.

The following should be referred to the digital GND: $V_{EE}$, REF decouple (pin 28), -2V supply for output termination, clock termination, device GND, pins 1, 15 and 22.

The following should be referred to the analog GND: Ref +VE, REF -VE, input termination or buffer.




NOTES
1. Data is valid over complete clock cycle and appears at the O/P after one clock cycle delay.
2. The carry output is valid one clock cycle before the relevant data output.

*Fig.3 Timing diagram*

## SUBRANGING

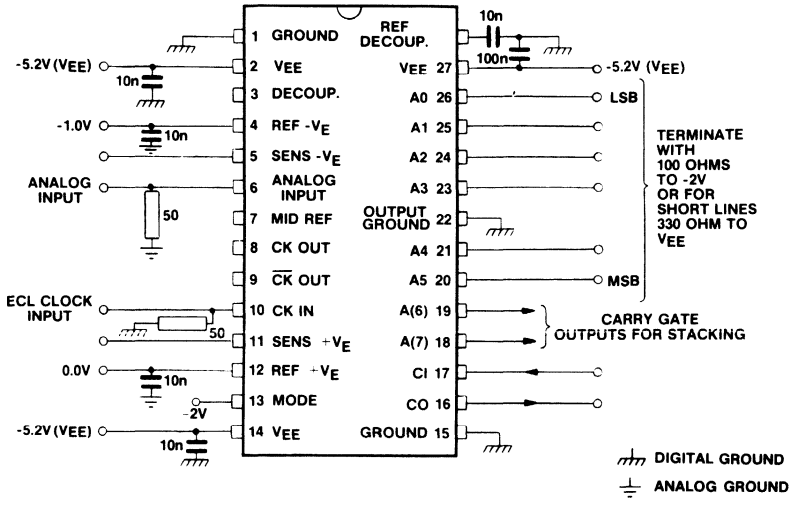
The subranging system uses a two rank method for coarse then fine digitisation of the input signal. The SP9756-8 is ideally suited for subranging systems as the accuracy of the first rank conversion defines the total system accuracy. Systems with 8 bits $\pm\frac{1}{2}$ LSB accuracy can be realised (see Fig.5).

## NON LINEAR CODING (REF.3)

By simply feeding the reference with a proportion of the analog input (as shown in Fig.6) non-linear coding can be produced. The accuracy of the Plessey SP9756-8 allows expansion factors of 4:1 whilst maintaining $\frac{1}{2}$ LSB accuracy. This gives a dynamic range of 49.8 dB from a single six-bit device.

## REFERENCES


1. *Dynamic Performance of A to D Converters, Hewlett Packard Product Note 5180A-Z.*
2. *A Complete 100MHz A/D - D/A Evaluation System, Plessey P.S.2048.*
3. *Cern-EP/79-133, B. Hallgren & H. Verweij.*


NOTES ON APPLICATION

1. MODE drives output either 'all zeros' or 'all ones' on over-range.
2. Kelvin connections can be made to the referenced chain via SENS (+VE) and SENS (-VE).
3. O/C leave open circuit.
4. REF DECOUPLE (Pin 28) gives access to DC bias reference for logic. This gives ability to eliminate possible crosstalk by allowing capacitor to remove edge noise.
5. Keep OUTPUT GROUND separate from GROUND.

*Fig.4 Test and applications circuit*

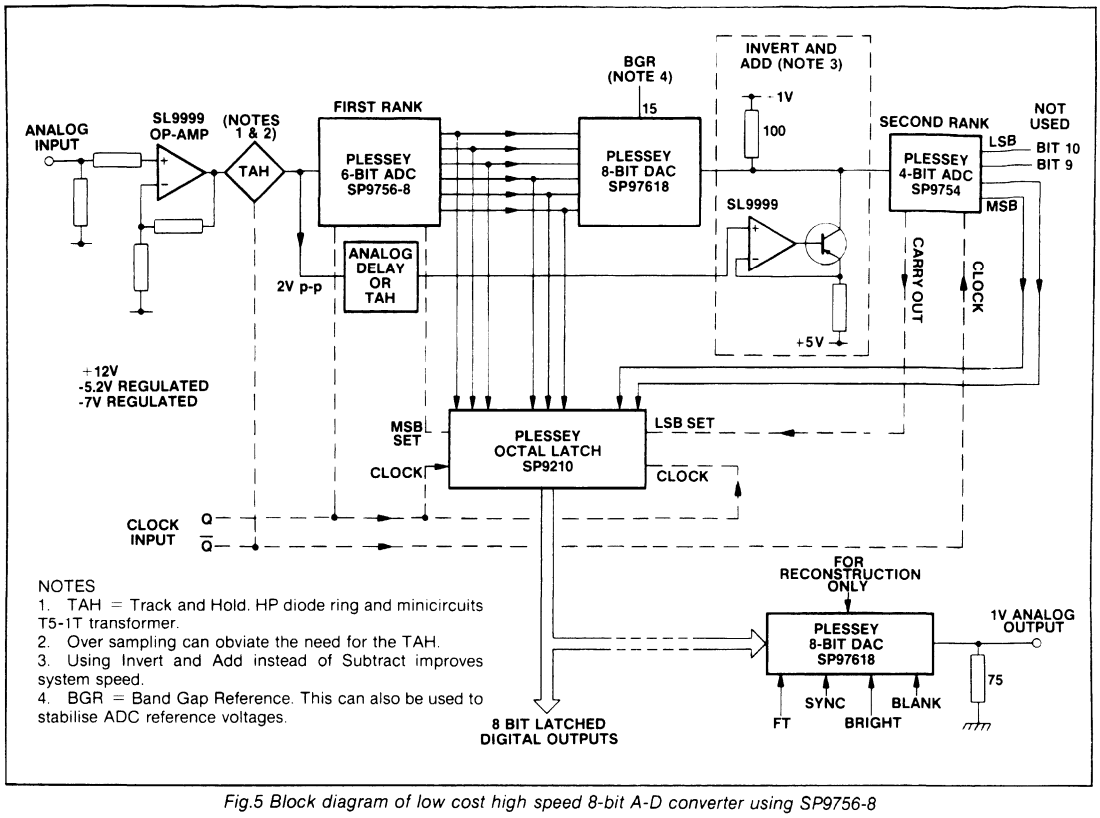



*Fig.5 Block diagram of low cost high speed 8-bit A-D converter using SP9756-8*

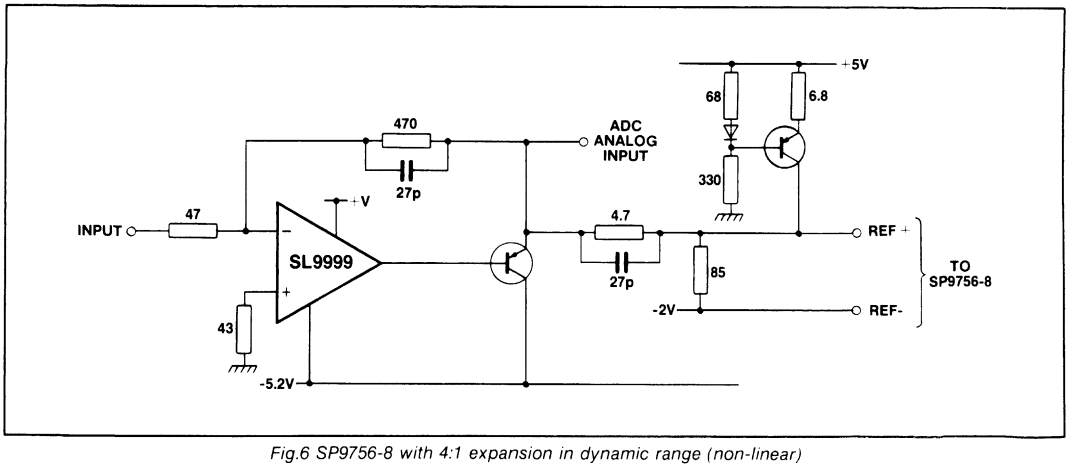



*Fig.6 SP9756-8 with 4:1 expansion in dynamic range (non-linear)*

## TYPICAL ACCURACY DATA

**SP9756-8**

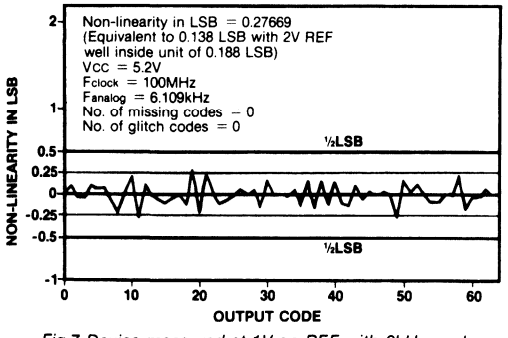



*Fig.7 Device measured at 1V on REF with 6kHz analog and 100MHz clock*

**SP9756-8**

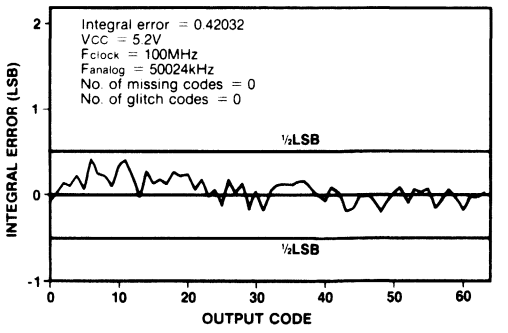



*Fig.8 Measured with 2V REF at 50MHz analog and 100MHz clock proves ±0.5 LSB integral spec and* ±0.5 LSB differential spec

**SP9756-8**

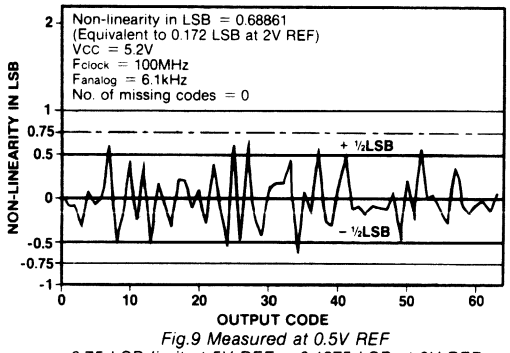



*Fig.9 Measured at 0.5V REF*
*0.75 LSB limit at 5V REF ≡ 0.1875 LSB at 2V REF*
*0.5 LSB limit at 5V REF ≡ 0.125 LSB at 2V REF*

**SP9756-6**

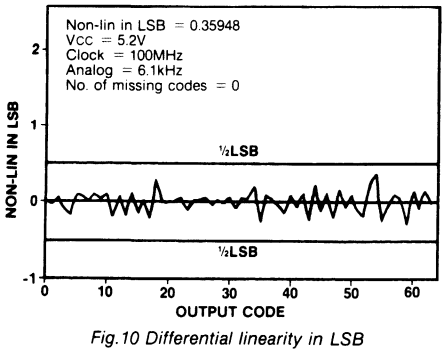



*Fig.10 Differential linearity in LSB*

**SP9756-6**

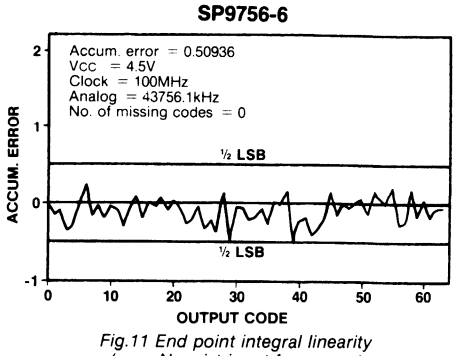



*Fig.11 End point integral linearity (near Nyquist input frequency)*

*THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGNS.*
*USE OF THE PIN-COMPATIBLE SP97504 IS PREFERRED.*

**PLESSEY**
**Semiconductors**

# SP9754

## HIGH SPEED FOUR BIT EXPANDABLE A TO D CONVERTER

The SP9754 is a fast 4 bit A-D converter, expandable up to 8 bits without additional encoding circuitry.

It can convert at sample rates from DC to 110MHz, with analog inputs up to Nyquist frequencies. All output levels are ECL compatible

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous.

The SP9754 operates from a +5V, -7V supply.

### FEATURES

- Operating Temperature Range -30°C to +85°C
- No External Components For 4-Bit Conversion
- 110MHz Conversion Rate
- On-Chip Encoding For Expansion to 8 Bits
- No External Sample and Hold Needed
- On-Chip Resistor Reference Divider
- Bit Size 10-100mV
- ECL Compatible
- Over 100MHz Full Power Bandwidth
- 10ps Aperture Uncertainty Time
- 8-Bit Accuracy (When Expanded)

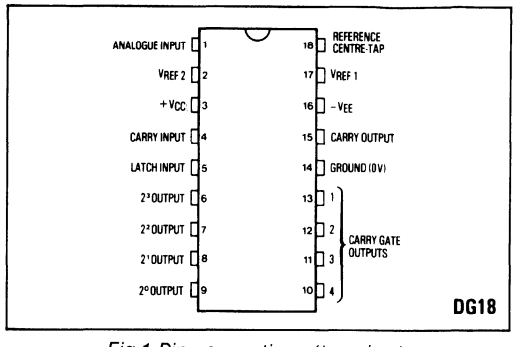



*Fig.1 Pin connections (top view)*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Positive supply voltage | +5.5V |
| Negative supply voltage | -7.5V |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |
| Lead temperature (soldering 60 sec) | 300°C |

### ORDERING INFORMATION

**SP9754DG** (Industrial - Ceramic DIL package)
**SP9754BB DG** (Plessey High Reliability Ceramic DIL package)

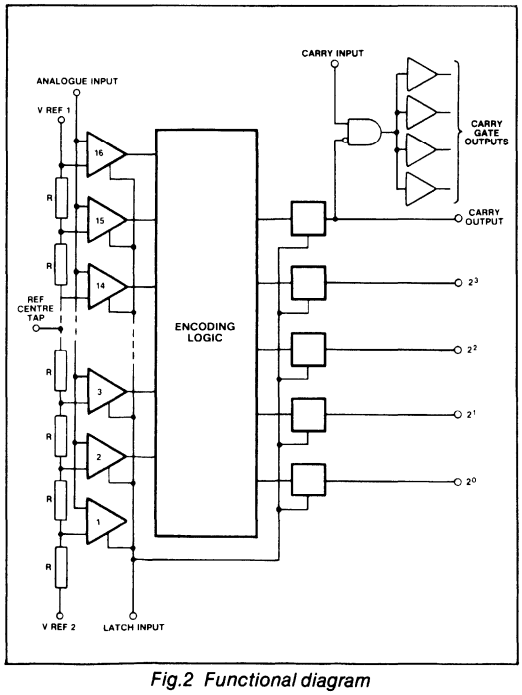



*Fig.2 Functional diagram*

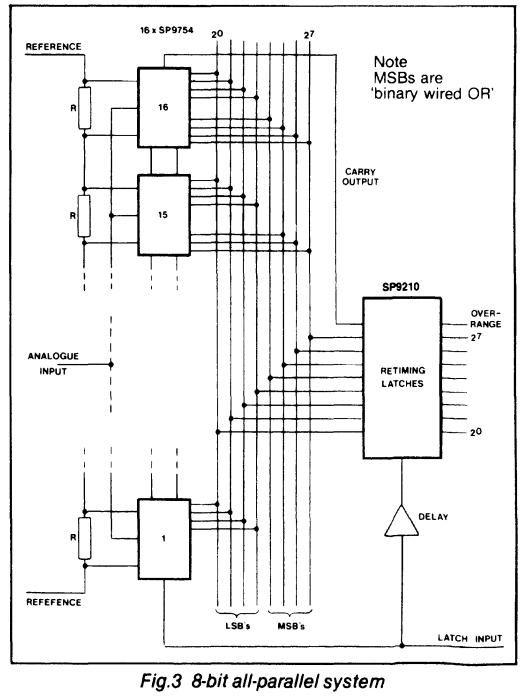



*Fig.3 8-bit all-parallel system*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{AMB}$ = 25°C
$V_{CC}$ = +5V ±0.25V
$V_{EE}$ = -7V ±0.25V
$R_L$ = 100 ohms to -2V

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Analog input current | $I_B$ | | 30 | 100 | μA | $V_{IN}$ = 0V |
| Analog input capacitance | $C_{IN}$ | | 10 | | pF | |
| Common mode range | $V_{CM}$ | -2 | | +2 | V | |
| Maximum input slew rate | | | 1000 | | V/μsec | |
| Latch input capacitance | $C_{IN}$ | | 2 | | pF | |
| Positive supply current | $I_{CC}$ | | 55 | 70 | mA | } See Fig.11 |
| Negative supply current | $I_{EE}$ | | 85 | 100 | mA | } See Fig.11 |
| Reference resistor chain | | | 25 | | Ω | total |
| Reference bit size | | 10 | | 100 | mV | |
| Comparator offset voltage | $V_{OS}$ | -5 | | +5 | mV | |
| Total power dissipation | $P_{DISS}$ | | 950 | 1160 | mW | All outputs loaded |
| Input & output logic levels | | | | | | |
| Logic high | $V_{OH}$ | -0.930 | | -0.720 | V | for 100 ohm load |
| Logic low | $V_{OL}$ | -1.90 | | -1.620 | V | to -2V |
| Min. latch set-up time | $t_S$ | | 1.5 | 2 | nsec | 10mV overdrive |
| Latch to output propagation delay: | | | | | | |
| Latch enable to output high | $t_{pd}$ + (E) | | 6 | 8 | nsec | |
| Latch enable to output low | $t_{pd}$ - (E) | | 5 | 8 | nsec | |
| Carry input to MSB delay | $t_{pd}$ (C) | | 3 | 5 | nsec | |
| Max. sample rate | $F_{c\,max.}$ | 100 | 110 | | MHz | |
| Aperture uncertainty time | $t_a$ | | 10 | | psec | |

Thermal characteristics $\theta_{JA}$ = 86°C/W
$\theta_{JC}$ = 36°C/W

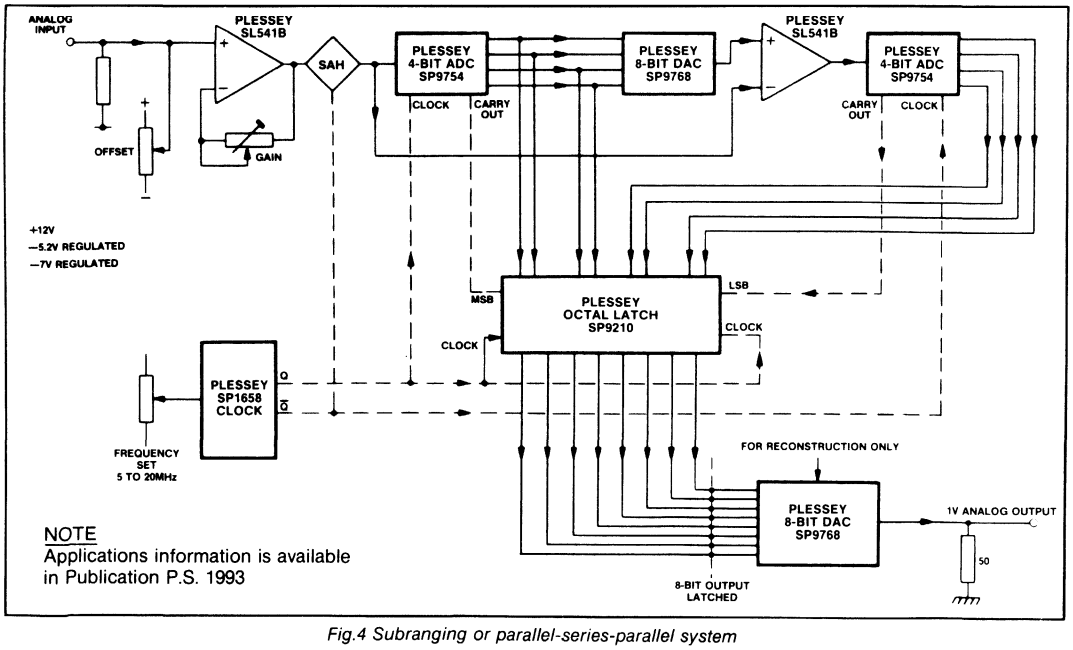



*Fig.4 Subranging or parallel-series-parallel system*

## PERFORMANCE CURVES

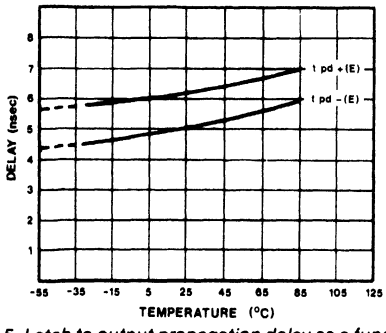



*Fig.5 Latch to output propagation delay as a function of temperature*

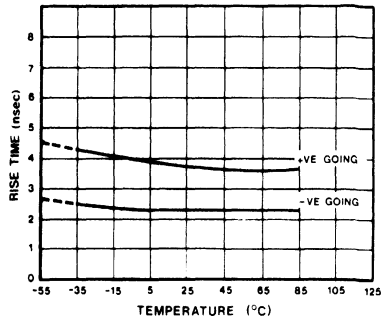



*Fig.6 Output rise/fall times as a function of temperature*

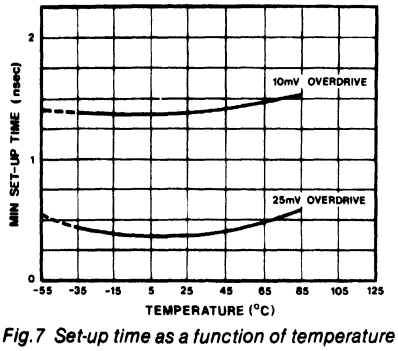



*Fig.7 Set-up time as a function of temperature*

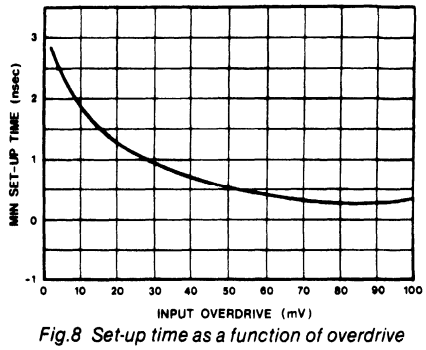



*Fig.8 Set-up time as a function of overdrive*

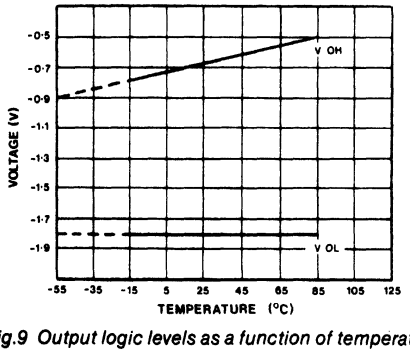



*Fig.9 Output logic levels as a function of temperature*

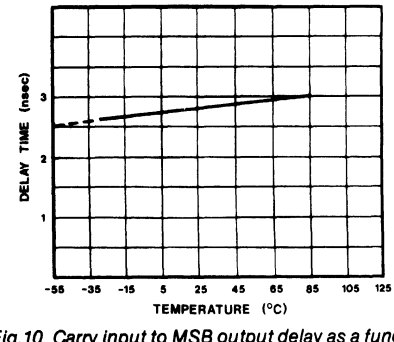



*Fig.10 Carry input to MSB output delay as a function of temperature*

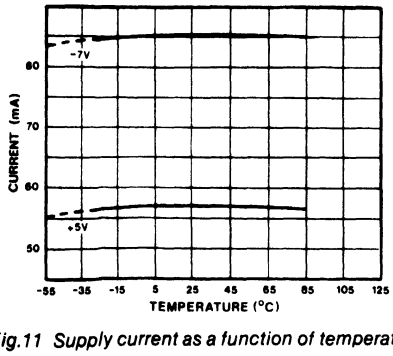



*Fig.11 Supply current as a function of temperature*

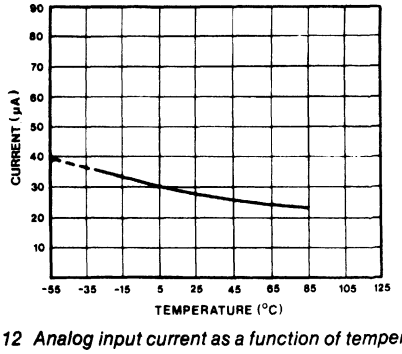



*Fig.12 Analog input current as a function of temperature*

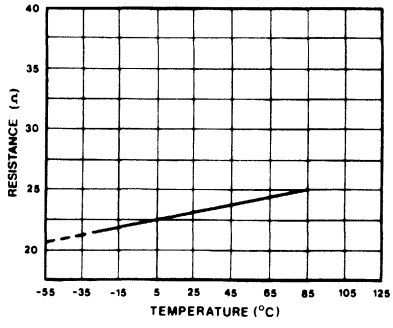



*Fig.13 Network resistance as a function of temperature*

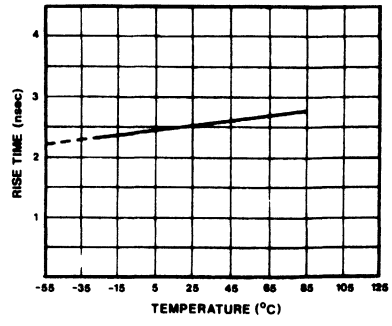



*Fig.14 MSB output edge speeds as a function of temperature*

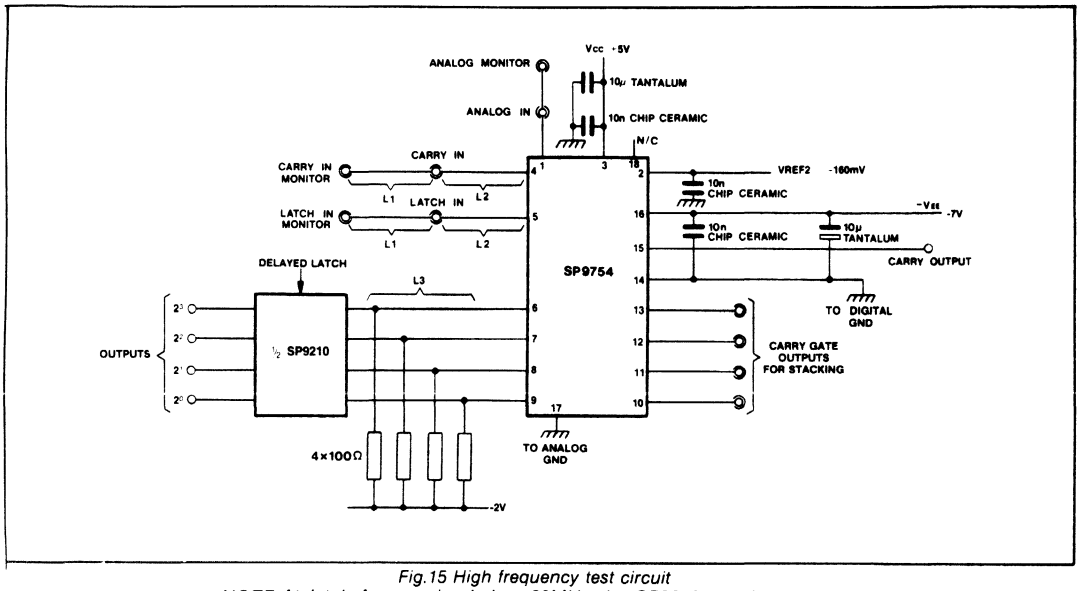



*Fig.15 High frequency test circuit*
*NOTE At latch frequencies below 60MHz the SP9210 can be ommitted.*

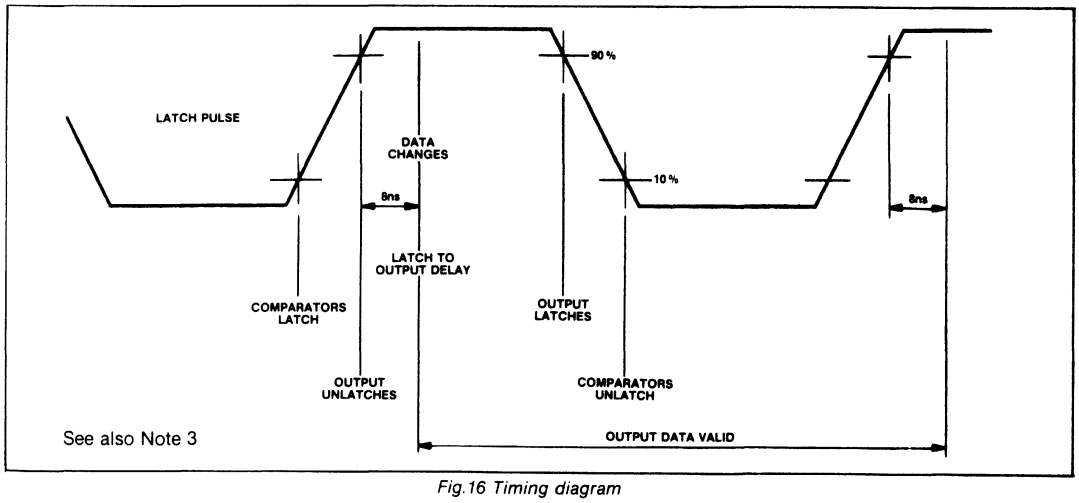



*Fig.16 Timing diagram*

## OPERATING NOTES

1. Carry output (pin 15) is high when the analog input exceeds the top reference voltage (pin 17).

Then the carry gate outputs (pins 10 to 13) go low regardless of carry input (pin 4). When the analog input is between $V_{REF}$ and $V_{REF2}$ and the carry output is low, the carry gate output will be high if the carry input is also high. Similarly if the carry input is low then the carry gate outputs will be low.

2. When used in an ambient temperature in excess of 75° C the SP9754 must be provided with an external electrically isolated heatsink or forced air cooling. This will ensure that the junction temperature does not exceed 175° C.
3. At operating clock frequencies above 60MHz clock edges should have rise and fall no faster than 4nsec.

## APPLICATION NOTES

1. The device is ideally suited to subranging systems as it maintains good accuracy at low reference voltages. This enables the second rank to be driven at higher speed from the subtracting Op-Amp.
2. For applications that require low bit error rates at high frequency, the clock signal should be adjusted for 60% ECL low, 40% ECL high mark to space ratio.

# SP98608

## 8-BIT LATCHED 450MHz MULTIPLYING D-A CONVERTER

The SP98608 is an ECL 10K compatible 8-bit latched DAC. The 2.2nsec settling time allows a 450 megasample per second conversion rate. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP98608 design includes a high performance band-gap voltage reference and reference amplifier.

Both current and voltage multiplying modes are available. The input latch can be switched into transparent mode for applications that require low through delay.

### FEATURES

- Latched Inputs
- 2.2ns Settling Time ½ LSB Typically
- 8 Bits ±½ LSB Integral and Differential Linearity
- Operating Temperature Range -40°C to +85°C
- ECL 10K Standard Inputs
- Complementary Current Outputs, 40mA Full Scale
- Reference Temperature Coefficient Typically < 40ppm/°C
- Single -5.2V Supply

### ORDERING INFORMATION

**SP98608DG** (Industrial - Ceramic DIL package)
**SP98608BB DG** (Plessey High Reliability Specification)
**SP98608LC** (Industrial - Ceramic LCC package)
(Under development)

### APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems
- ADC Evaluation

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | -5.7V |
| Digital input voltage | 0 to -4.5V |
| Minimum $R_{SET}$ (from 0V) | 175Ω |
| Maximum $R_{SET}$ | 2.5kΩ |
| Output reference supply ($V_L$) | 0 to +3V |
| Reference input | ±2V |
| Storage temperature range | -55°C to 150°C |
| Operating junction temperature | <175°C |
| Lead temperature (soldering 60 sec) | 300°C |

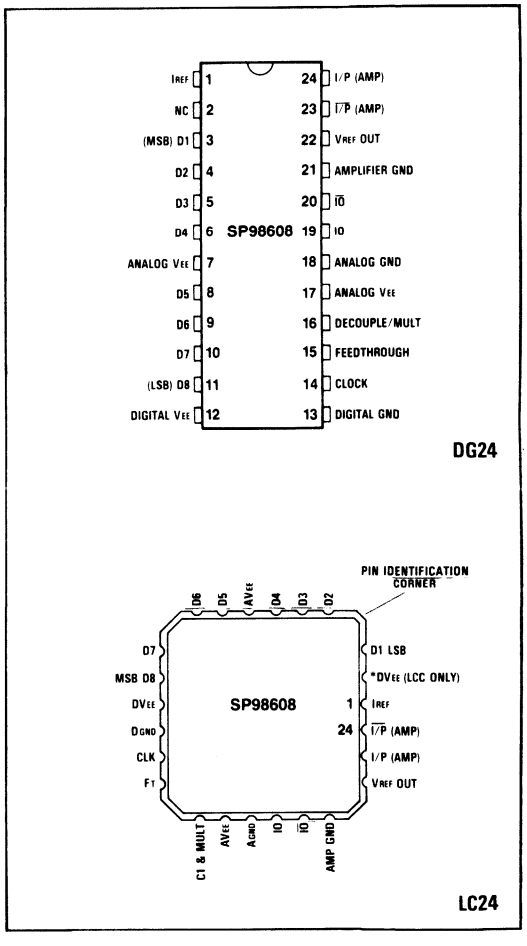



*Fig.1 Pin connections - top view*

### THERMAL CHARACTERISTICS

$\theta J_C$ = 28°C/W
$\theta J_A$ = 90°C/W

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25°C; $V_{EE}$ = -5.2V ± 5%; $R_{SET}$ = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

| Characteristic | Value | | | Unit | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Supply current $I_{EE}$ | | 135 | 154 | mA | All inputs at -1.8V |
| Logic inputs: | | | | | |
| $V_{IH}$ | -0.96 | | -0.81 | V | Standard ECL |
| $V_{IL}$ | -1.85 | | -1.65 | V | 10K compatible |
| $I_{IN(HI)}$ | | 115 | 200 | μA | All inputs HI |
| Reference voltage $V_{REF}$ | | -1.280 | | V | |
| Reference voltage temp. coeff. | -80 | 0 | 80 | ppm/°C | -30°C to +85°C |
| Output current - full scale | 2 | | 44 | mA | $R_{SET}$ 1.3kΩ to 85Ω |
| Output current - full scale | 38 | 42 | | mA | $R_{SET}$ = 130Ω |
| Output compliance | -1.2 | | +1.0 | V | $T_{amb}$ = 25°C Note 3 |
| | -1.0 | | +1.0 | V | $T_{amb}$ = 85°C Note 3 |
| Bit size (LSB) | 158 | 166 | 175 | μA | Current output, $R_{SET}$ = 130Ω |
| Resolution | 8 | | | Bits | |
| | 0.391 | | | % | |
| Integral non-linearity | | | 0.5 | LSB | End point integral |
| Differential non-linearity | | | 0.5 | LSB | |
| **Output dynamic parameters (see Note 1)** | | | | | |
| Rise time $t_r$ | | 600 | | ps | 10 to 90% |
| Glitch energy (latched) | | 20 | | psV | Mid-point |
| Glitch energy (transparent) | | 140 | | psV | transition |
| Noise output | | -90 | -83 | dBm | See Note 2 |
| Power supply rejection ratio (output WRT supply) | 45 | 80 | | dB | ±0.3V at 20kHz |
| **Multiplying mode - voltage** | | | | | |
| Multiplying input voltage range | -2 | | 0 | V | |
| Reference input resistance | | 10 | | kΩ | |
| Multiplying input bandwidth | | 30 | | MHz | -3dB |
| Transfer function non-linearity | | 0.2 | 1.0 | %FS | DC |
| **Multiplying mode - current** | | | | | |
| Multiplying input current range | 1 | | 15 | mA | |
| Set current input resistance | | 400 | | Ohms | |
| Multiplying input bandwidth | | 300 | | MHz | -3dB |
| Transfer function non-linearity | | 1.0 | 3.0 | %FS | DC |

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.
4. Analog and digital grounds should be connected together at the device pins.

| Dynamic characteristic (Note 1) | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Update rate | $F_{CLK}$ | | 450 | | MHz | |
| Latch setup time | $t_s$ | | 0.9 | | ns | |
| Latch hold time | $t_h$ | 0 | | | ns | |
| Settling time full scale | $t_{st}$ | | 2 | | ns | ½ LSB |
| Internal clock delay | $t_c$ | | 500 | | ps | |
| Initial time to 10 % | $t_i$ | | 50 | | ps | |

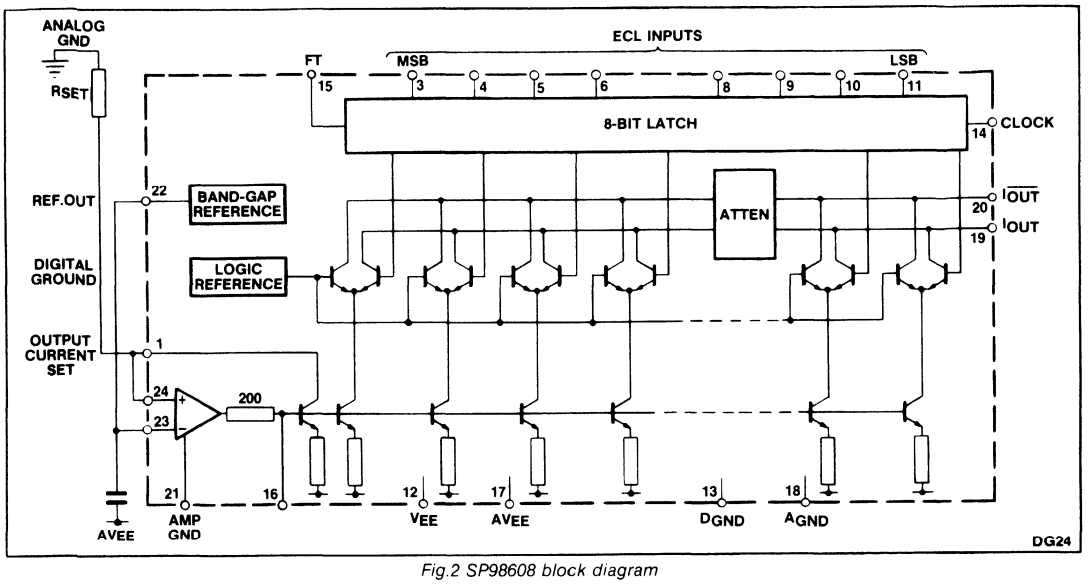



*Fig.2 SP98608 block diagram*

## OPERATING NOTES

The pinout of the device is shown in Fig.1. External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 40mA, corresponding with a 1 volt drop across a 25Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, $I_{OUT}$, is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary $I_{OUT}$ is also provided. If single output operation is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, $R_{SET}$, is typically 130Ω, giving a full-scale output current of 42mA, and should have a temperature coefficient similar to that of the output load resistor.

### Reference

The reference supply is internally compensated; however, to reduce the possibility of instability in some circuits, it has been bonded out to pin 16, it can therefore be decoupled to $AV_{EE}$ if required.

### Clock

The clock input is ECL 10K compatible. Data at the device inputs are acquired by the input latch on the rising edge of the clock.

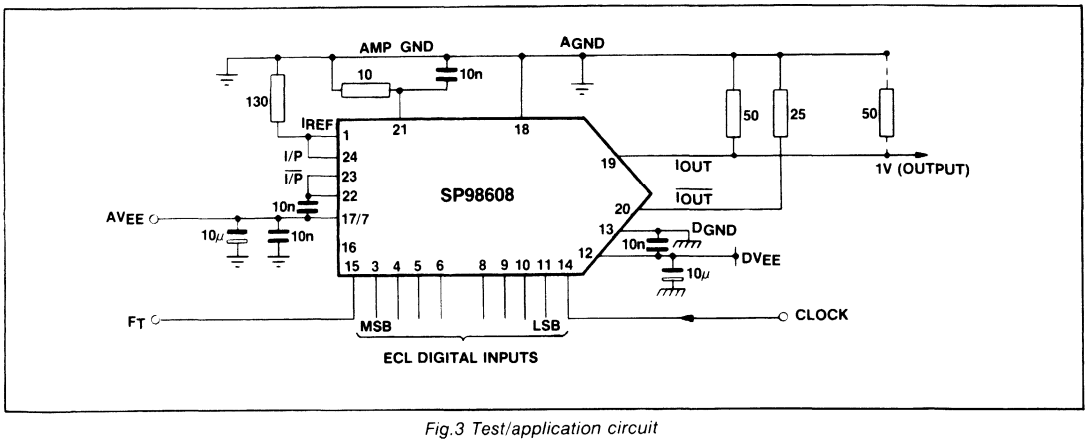



*Fig.3 Test/application circuit*

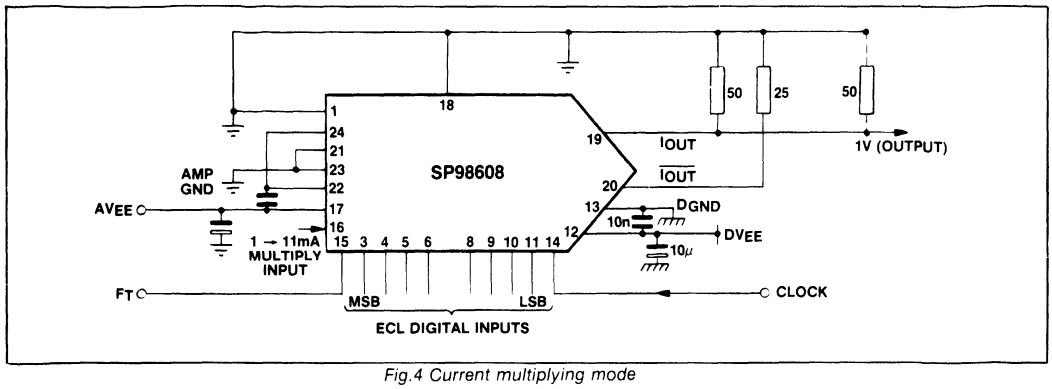



*Fig.4 Current multiplying mode*

### FT (Feedthrough)

The FT input allows both transparent or latched data inputs. When open circuit this pin will self bias to -2V and the data will be retained by the input latch for one clock cycle.

When the FT input is connected to 0V the input latch will be transparent. In this mode, it is essential that the input data has low time skew (<100ps) to avoid output glitches.

### Multiplying Mode

Multiplying operation of the DAC is available in two modes: either a voltage applied in place of the internal reference, or a current supplied via the current set pin.

**Voltage Multiplying.** The transfer function is approximately: $I_{OUT}$ (Full Scale) = 4 x $V_{IN}/R_{SET}$. While this mode offers the best linearity of operation, the frequency response limitations mean that the maximum usable bandwidth is limited to approximately 50kHz.

**Current Multiplying.** A circuit for using the DAC in current multiplying mode is shown in Fig.4. The transfer function is approximately: $I_{OUT}$ (Full Scale) = 4 x $I_{IN}$. In this mode the current setting loop amplifier is not used.

The operational bandwidth of the current input to -3dB is at least 320MHz.

A 1V output is obtained into 25Ω when a current of aproximately 11mA is fed into pin 1 and the input code is selected for full output current.

### Output Compliance

Using the SP9778 with a load resistor not referred to ground, allows a larger output swing than the conventional connection of Fig.3. Connecting analog ground and the current setting resistor $R_{SET}$ to the load return supply ensures that the scale factor of the output is independent of the load reference.

Extending the compliance beyond +1V may cause slight degradation of linearity. +3V should be considered an absolute maximum.

## TIMING

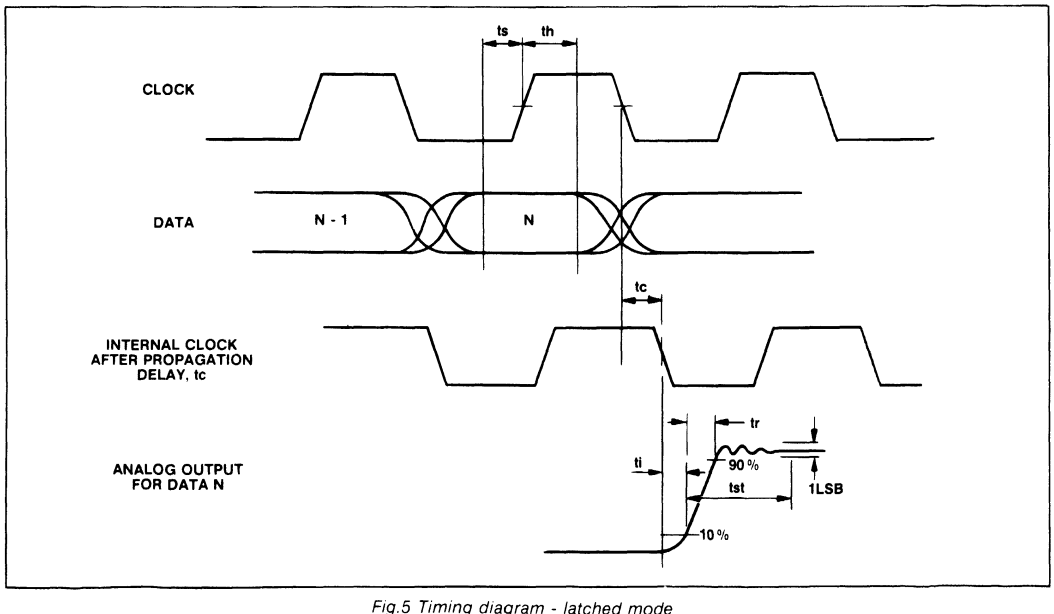



*Fig.5 Timing diagram - latched mode*

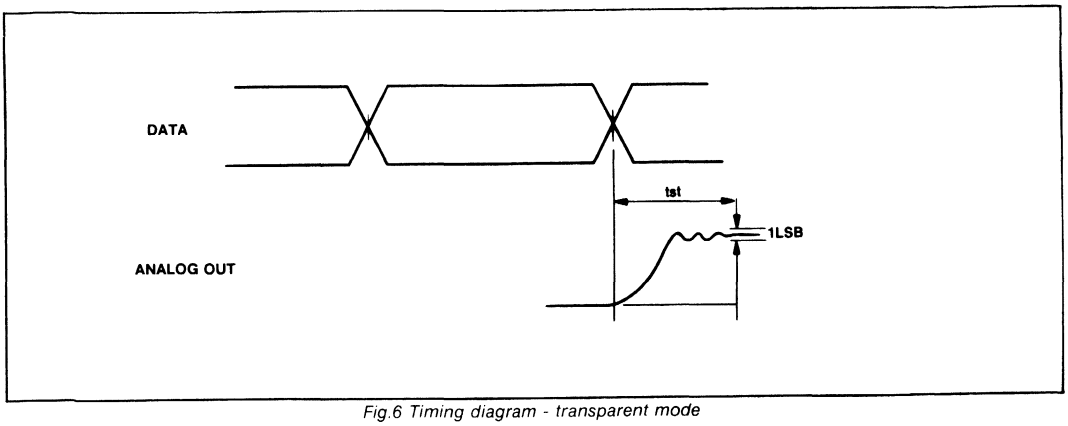



*Fig.6 Timing diagram - transparent mode*

# MV95408

## 8-BIT 50MHz DIGITAL TO ANALOG CONVERTER

The Plessey CMOS MV95408 has been designed for use in both video graphics and general high speed DAC applications.

Very low external component count is achieved as the device contains both an on chip reference amplifier and reference voltage source.

The device also contains an input register and registered video controls (Blank, Ref. White, Over Bright and Sync.). These control inputs and associated internal circuitry allow the MV95408 to be used in video graphics systems.

A control on/off input also allows the video pedestals to be overridden for conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard (RS343) video levels.

Pullup resistors have been added to tie all unused inputs into their inactive states.

### ORDERING INFORMATION

**MV95408 DP** (Industrial - Plastic DIL package)

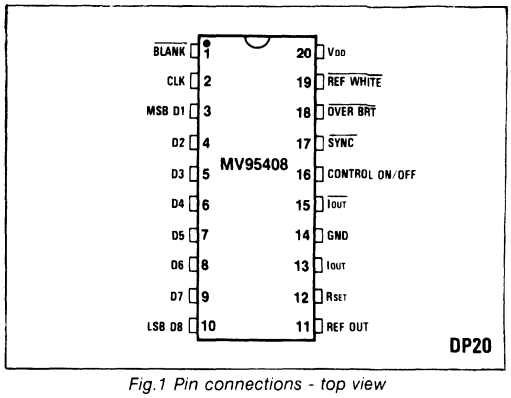



*Fig.1 Pin connections - top view*

### FEATURES

- Low Power
- RS 343 Compatible Levels
- Differential Linearity < ±½ LSB
- 20ns Settling to ±½ LSB
- On Chip Reference Voltage Source
- Graphics Ready
- Registered CMOS Inputs
- Guaranteed Monotonic
- Drives 75 Ohm Loads Directly
- Single 5V Power Supply
- 0°C to +70°C Temperature Range
- < 6ns Output Rise Time (10% to 90%)

### APPLICATIONS

- Data Conversion (General)
- Commercial TV
- Computer Graphics
- Instrumentation
- Test Equipment
- Waveform Synthesis

### RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| $R_{Load}$ (both outputs) | 75Ω |
| $V_{DD}$ | 5.0V ± 0.5V |
| $R_{SET}$ (graphics applications) | 1.8k |
| $R_{SET}$ (other DAC applications) | 1.2k |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | +7V |
| Storage temperature | -55°C to 125°C |
| Chip temperature | <150°C |

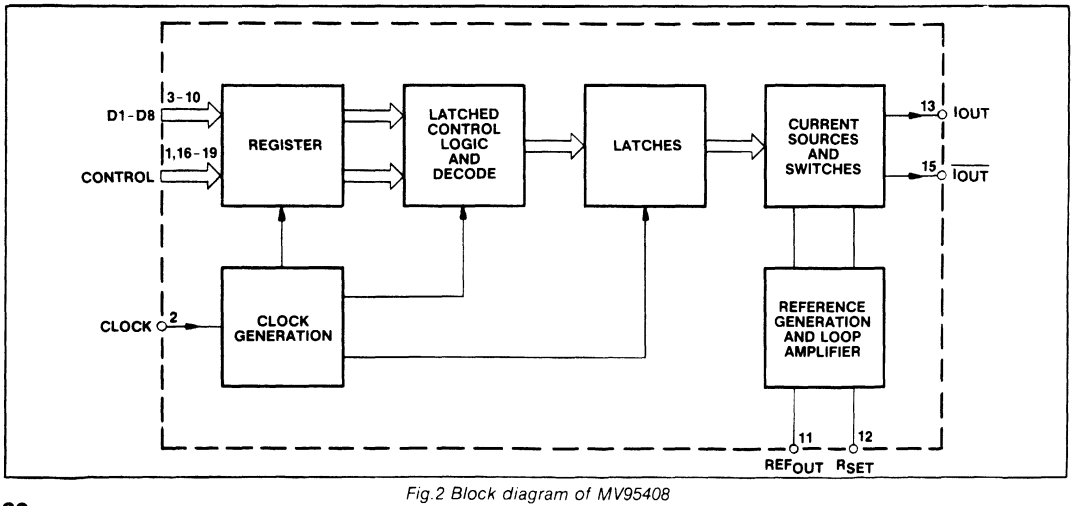



*Fig.2 Block diagram of MV95408*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 0°C to 70°C, $V_{DD}$ = +5V ± 0.5V

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply current | $I_{DD}$ | | 58 | 70 | mA | |
| Resolution | | 8 | | | Bits | |
| Differential linearity | | | | ±½ | LSB | $R_{SET}$ = 1.8k |
| Integral linearity | | | | ±½ | LSB | $R_{SET}$ = 1.8k |
| Internal reference voltage | $V_{ref}$ | | 1.0 | | V | Pin 11 |
| Update rate | $f_C$ | 50 | 75 | | MHz | |
| Maximum output current | $I_{out}$ | 16 | | | mA | |
| Clock minimum high | $t_H$ | 6 | | | ns | |
| Clock minimum low | $t_L$ | 6 | | | ns | |
| Input voltage high | $V_{INH}$ | 3 | | | V | |
| Input voltage low | $V_{INL}$ | | | 1.2 | V | |
| Data input current | | | | 20 | μA | $V_{IN}$ = 5.0V (At $f_{max}$) |
| Output rise time | $t_r$ | | | 5.5 | ns | 10% to 90% |
| Settling time | $t_{st}$ | | | 20 | ns | To ±½ LSB (75Ω load) |
| Clock to output delay | $t_i$ | | 6 | | ns | Output at 10% full scale |
| Glitch energy | | | <100 | | ps V | |

## THERMAL CHARACTERISTICS

| | |
|---|---|
| Chip to case $\theta_{JC}$ | 30°C/W |
| Chip to ambient $\theta_{JA}$ | 86°C/W |

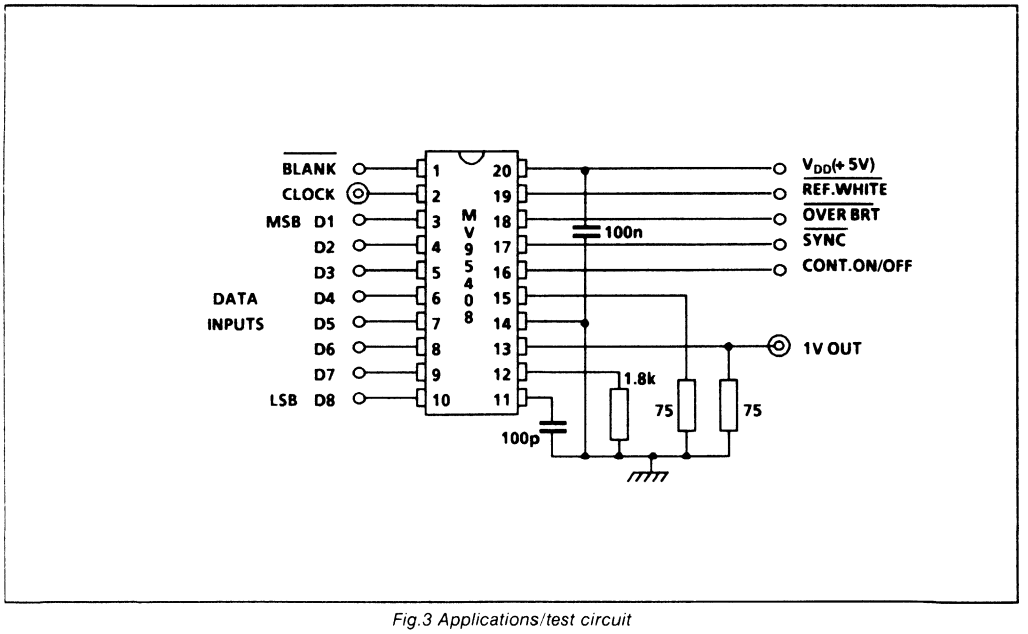



*Fig.3 Applications/test circuit*

## OPERATING NOTES

For optimum performance the device should be used in a low profile socket located over a solid ground plane. It is also important that the decoupling capacitor on pin 20 ($V_{DD}$) is located close to the device pin. For good stability the capacitance on pin 12 ($R_{SET}$) should be kept to a minimum (<10pF).

The outputs from this D to A converter are open drain, current sources and hence require pulldown load resistors. The value of the load resistors will therefore determine the peak to peak output voltage from the DAC. This should not exceed 1.2V.

With all the data inputs high and a load of 75Ω on each output, a full scale output of 1V will be seen, (Fig.3). Fine adjustment of the output voltage can be achieved by varying the value of $R_{SET}$. Increasing $R_{SET}$ will decrease the output amplitude.

For optimum slew rate and settling time, the unused output should be connected to ground via the same resistance as on the used output. This will balance the currents within the output stage of the DAC and hence provide cleaner switching.

Table 1 shows the output currents from the MV95408 with combinations of input data and control settings.

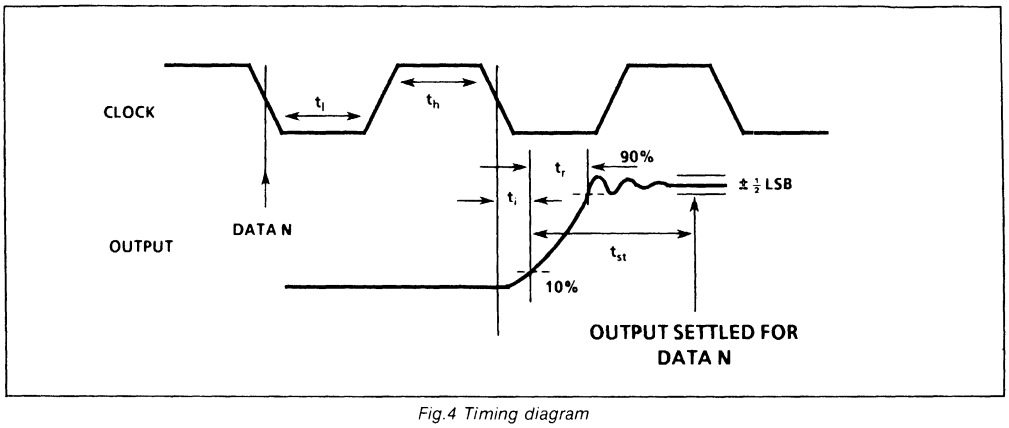



*Fig.4 Timing diagram*

### Over Bright (Pin 18)

This control input has been introduced specially for graphics applications. It can be used to illuminate areas of graphics displays for borders, headings or cursors etc. When held low this input will cause a 10% of blank to full white level increase in the output current. Unlike the other control inputs the over bright input does not override the data. See Table 1.

### Control On/Off (Pin 16)

This feature allows the MV95408 to be used in conventional DAC applications. When held low this pin will remove the sync pedestal and disable the Over Bright input. This allows the full 1V output range of the DAC to be used, 0 to 13mA into 75Ω. To gain this extra active output range, it is necessary to decrease the value of $R_{SET}$ to 1.2kΩ.

With the control on/off pin low and all the data inputs high, the output current can be calculated from:

$$I_{out} = \frac{16 \times V_{ref}}{R_{SET}}$$

$V_{ref}$ = 1.0V typ.

With the control on/off input open circuit the device will be configured for video graphics. In this mode and with all the data inputs high, the output current can be calculated from:

$$I_{out} = \frac{16 \times V_{ref}}{R_{SET}} + 4.533\text{mA}$$

$V_{ref}$ = 1.0V typ.

| Description | Control On/Off | Sync Bar | Blank Bar | Ref. White Bar | 10 % Over.BRT Bar | Input Data | $I_{OUT}$ (mA) $R_{SET}$ = 1.8k |
|---|---|---|---|---|---|---|---|
| Ref. White +10 % | 1 | 1 | 1 | 0 | 0 | X | 14.285 |
| Ref. White | 1 | 1 | 1 | 0 | 1 | X | 13.333 |
| Full White | 1 | 1 | 1 | 1 | 1 | FF | 13.333 |
| Over Bright | 1 | 1 | 1 | 1 | 0 | Data | $I_{CODE}$ +0.952 |
| Full Black | 1 | 1 | 1 | 1 | 1 | 00 | 4.533 |
| Blank | 1 | 1 | 0 | X | X | X | 3.183 |
| Data-Sync | 1 | 0 | 1 | 1 | 1 | Data | $I_{CODE}$ -3.813 |
| Sync | 1 | 0 | 0 | X | X | X | 0.000 |
| Control On/Off | 0 | X | 1 | 1 | X | Data | $I_{CODE}$ (0 to 13mA) $R_{SET}$ = 1.2k |

*Table 1 Control inputs*

X = Don't Care '1' = +5V, '0' = 0V, FF = All '1's

# SP97618

## 8-BIT HIGH SPEED GRAPHICS DAC

The SP97618 is a 250 MegaSample Per Second (MSPS), 8-bit digital-to-analog converter, capable of directly driving a 75Ω load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Four special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

### FEATURES

- Pin Replacement for TDC1018 - But Faster
- 250 MSPS Update Rate (Typ)
  200 MSPS Update Rate (Guaranteed)
- 8-Bit Resolution and Accuracy
- 1/2 LSB Linearity
- Power Supply Noise Rejection Typically > 80dB
- Registered Data and Video Controls
- Differential Current Outputs
- Video Controls: SYNC, BLANK, BRight, Force High
- Inherently Low Glitch Energy
- ECL Compatible
- Multiplying Mode Capability
- Power Dissipation 800mW
- Available in 24 Lead DIP Package
- Single -5.2V Power Supply
- On Board Reference BUFFER
- Operating Temperature Range:
  Commercial Plastic -40°C to +85°C

### ORDERING INFORMATION

**SP97618 DP** (Commercial Plastic Package)

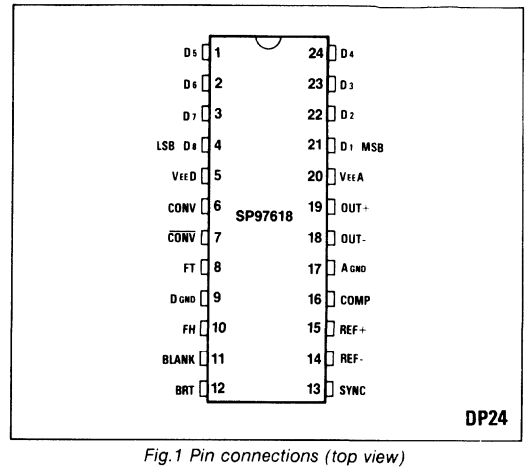



*Fig.1 Pin connections (top view)*

### APPLICATIONS

- RGB Graphics (1K x 1K pixels)
- High Resolution Video
- Raster Graphic Displays
- Digital Waveform Synthesisers
- Automated Test Equipment
- Digital Transmitters/Modulators

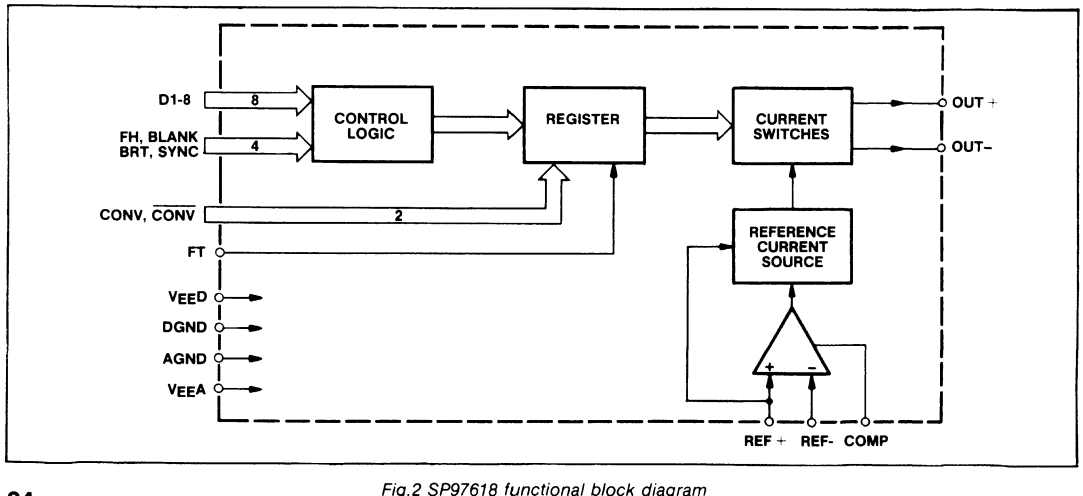



*Fig.2 SP97618 functional block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 0°C to +70°C

**DC Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Digital supply voltage | $V_{EED}$ | -4.9 | -5.2 | -5.5 | V | Measured to $D_{GND}$ |
| Analog supply voltage | $V_{EEA}$ | -4.9 | -5.2 | -5.5 | V | Measured to $A_{GND}$ |
| Supply current | $I_{EEA}$ + $I_{EED}$ | | | 140 | mA | $V_{EEA}$ = $V_{EED}$ = Max |
| Analog ground voltage | $V_{AGND}$ | -0.1 | 0.0 | 0.1 | V | Measured to $D_{GND}$ |
| Supply voltage differential | $V_{EEA}$ - $V_{EED}$ | -0.1 | 0.0 | +0.1 | V | |
| CONV input voltage, common mode range | $V_{ICM}$ | -0.5 | | -2.5 | V | |
| CONV input voltage differential | $V_{IDF}$ | 0.4 | | 1.2 | V | |
| Min. CONV pulse width, LOW | $t_{PWL}$ | | 2 | 2.5 | ns | |
| Min. CONV pulse width, HIGH | $t_{PWH}$ | | 2 | 2.5 | ns | |
| Min. Set up time, data and controls | $t_S$ | | 2 | 4 | ns | |
| Hold time, data and controls | $t_H$ | 0 | | | ns | |
| Input voltage, logic LOW | $V_{IL}$ | -1.5 | | | V | |
| Input voltage, logic HIGH | $V_{IH}$ | | | -1.0 | V | |
| Reference current | $I_{REF}$ | | | | mA | |
| Video standard levels | | 1.059 | 1.115 | 1.171 | | |
| 8-bit linearity | | 1.0 | | 1.3 | mA | |
| Compensation capacitor | $C_C$ | | 5 | | nF | |

**System Performance Characteristics**

| Characteristic | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Linearity error integral, terminal based | ELI | | | ±0.2 | % | $V_{EEA}$,$V_{EED}$ = Nom<br>$I_{REF}$ = Nom |
| Linearity error differential | ELD | | | ±0.2 | % | $V_{EEA}$, $V_{EED}$ = Nom<br>$I_{REF}$ = Nom |
| Output offset current | $I_{OF}$ | | 0.7 | 10 | μA | $V_{EEA}$, $V_{EED}$ = Max |
| Absolute gain error | $E_G$ | | ±0.5 | ± 5 | % | $V_{EEA}$, $V_{EED}$ = Min<br>$I_{REF}$ = Nom |
| Gain error tempco | $TC_G$ | | | ±0.024 | %/°C | $V_{EEA}$, $V_{EED}$ = Min<br>$I_{REF}$ = Nom |
| Power supply rejection ratio (Note (1)) | PSRR | | 90 | 45 | dB | $V_{EEA}$, $V_{EED}$ = Nom<br>$I_{REF}$ = Nom |
| Power supply rejection ratio (Note (2)) | PSRR | | 90 | 55 | dB | $V_{EEA}$, $V_{EED}$ = Nom<br>$I_{REF}$ = Nom |
| Power supply sensitivity | PSS | | | 120 | μA/V | $V_{EEA}$, $V_{EED}$ = Nom<br>$I_{REF}$ = Nom |
| Peak glitch energy (Area) (Note (3)) | $G_E$ | | 14 | 30 | pV-sec | FT = 1 |
| Feedthrough clock (Note (4)) | $FT_C$ | | -70 | -50 | dB | Data = Constant |
| Feedthrough data (Note (4)) | $FT_D$ | | -60 | -50 | dB | Clock = Constant |

NOTES
1. 20kHz ± 0.3V ripple on $V_{EEA}$, $V_{EED}$. dB's relative to full Gray Scale.
2. 60Hz, ± 0.3V ripple on $V_{EEA}$, $V_{EED}$. dB's relative to full Gray Scale.
3. 37.5ohm load. Average glitch energy approaches zero.
4. dB relative to full Gray Scale, 250MHz bandwidth limit.

**AC Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum update rate | $F_S$ | 200 | 250 | | MSPS | $V_{EEA}$, $V_{EED}$ = Min |
| Clock to output delay clocked mode | $t_{DSC}$ | | | 8 | ns | $V_{EEA}$, $V_{EED}$ = Min, FT = 0 |
| Data to output delay, transparent mode | $t_{DST}$ | | | 13 | ns | $V_{EEA}$, $V_{EED}$ = Min, FT = 1 |
| Current settling time clocked mode | $t_{SI}$ | | | | | $V_{EEA}$, $V_{EED}$ = Min, FT = 0 |
| 0.2 % | | | | 10 | ns | |
| 0.8 % | | | | 8 | ns | |
| 3.2 % | | | | 5 | ns | |
| Rise time, current | $t_{RI}$ | | | 1.1 | ns | 10 % to 90 % of Gray Scale |

## ABSOLUTE MAXIMUM RATINGS

**Supply Voltage**

| | |
|---|---|
| $V_{EED}$ (measured to $D_{GND}$) | 7V |
| $V_{EEA}$ (measured to $A_{GND}$) | 7V |
| $A_{GND}$ (measured to $D_{GND}$) | ±0.5V |

**Input**

| | |
|---|---|
| CONV, Data and Controls (measured to $D_{GND}$) | $V_{EED}$ to 0.5V |
| Reference input, applied voltage (measured to $A_{GND}$) | |
| REF + | $V_{EEA}$ to 0.5V |
| REF- | $V_{EEA}$ to 0.5V |
| Reference input, applied current, externally forced. | |
| REF + | 6.0mA |
| REF- | 0.5mA |

**Output**

| | |
|---|---|
| Analog output, applied voltage (measured to $A_{GND}$) | |
| OUT + | -2V to +2V |
| OUT- | -2V to +2V |
| Analog output, applied current externally forced. | |
| OUT + | 50mA |
| OUT- | 50mA |

## THERMAL CHARACTERISTICS

| | |
|---|---|
| $\theta_{JA}$ | 65 deg C/W (typ) |
| $\theta_{JC}$ | 15 deg C/W (typ) |
| $T_{amb}$ | -40° C to +85° C |
| Maximum storage temperature | -55° C to +150° C |
| Lead temperature (soldering 60 sec) | 300° C |

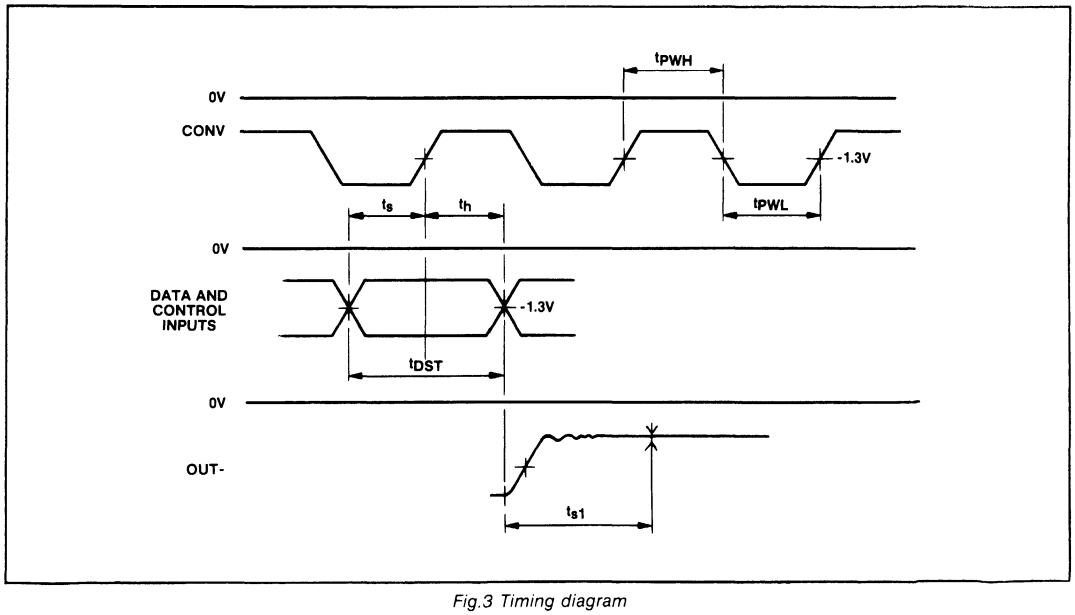



*Fig.3 Timing diagram*

## DEVICE PIN FUNCTIONAL DESCRIPTION

| Pin No. | Name | Description |
|---|---|---|
| 21 - 24, 1 - 4 | $D_1$ - $D_8$ | To allow the internal register to aquire the input data correctly the eight digital data inputs, $D_1$ - $D_8$, must be valid one data set-up time before each rising edge of the clock, and remain valid for one data hold time after this rising edge. $D_1$ - $D_8$ are overridden by FH, BLANK, or SYNC = 1. |
| 5 | $V_{EE}D$ | Digital supply voltage, -5.2V typ. ± 0.25V. |
| 6, 7 | CONV, $\overline{CONV}$ | Differential clock inputs which should have $V_{IH}$ and $V_{IL}$ levels compatible with standard ECL logic. |
| 8 | FT | Feedthrough (asynchronous control). When FT = 1, the input register is transparent. |
| 9 | $D_{GND}$ | Digital ground. |
| 10 | FH | Force High control. FH = 1 forces the output current to the equivalent of all data values $D_1$ - $D_8$ high. 10% enhancement of this value is available, via the BRT control. In the hierarchy of the controls, FH overrides only the data. |
| 11 | BLANK | Blank level control. When high, BLANK forces the output to -20.826mA (if $I_{REF}$ = 1.185mA), which is slightly below the normal low level signal generated by data = 0. BLANK takes precedence over all controls except SYNC and disables BRT. |
| 12 | BRT | Brightness enhancement control. When high, BRT increases the signal present by 10 % of the full scale current. This control is disabled when SYNC or BLANK is asserted. |
| 13 | SYNC | SYNC level control. When high, SYNC forces the output of the chip to a full negative output (standard -28.57mA for an $I_{REF}$ input of 1.185mA). SYNC = 1 takes precedence over all other controls and disables BRT. |
| 15, 14 | REF +, REF- | Connections for a differential reference current source. |
| 16 | COMP | Connection for compensation capacitor for internal reference buffer. |
| 17 | $A_{GND}$ | Analog ground. |
| 19, 18 | OUT +, OUT- | Current outputs, which comprise a differential pair designed to drive 37.5Ω loads directly. |
| 20 | $V_{EE}A$ | Analog supply voltage, -5.2V typ. ± 0.25V. |

| SYNC | BLANK | FORCE HIGH | BRIGHT | DATA INPUT | OUT- (mA) NOTE (1) | OUT- (V) NOTE (2) | OUT- (IRE) NOTE (3) | DESCRIPTION NOTE (4) |
|---|---|---|---|---|---|---|---|---|
| 1 | X | X | X | X | 28.57 | -1.071 | -40 | SYNC LEVEL |
| 0 | 1 | X | X | X | 20.83 | -0.781 | 0 | BLANK LEVEL |
| 0 | 0 | 1 | 1 | X | 0.00 | 0.00 | 110 | ENHANCED HIGH LEVEL |
| 0 | 0 | 1 | 0 | X | 1.95 | -0.073 | 100 | NORMAL HIGH LEVEL |
| 0 | 0 | 0 | 0 | 000 . . | 19.40 | -0.728 | 7.5 | NORMAL LOW LEVEL |
| 0 | 0 | 0 | 0 | 111 . . | 1.95 | -0.073 | 100 | NORMAL HIGH LEVEL |
| 0 | 0 | 0 | 1 | 000 . . | 17.44 | -0.654 | 17.5 | ENHANCED LOW LEVEL |
| 0 | 0 | 0 | 1 | 111 . . | 0.00 | 0.00 | 110 | ENHANCED HIGH LEVEL |

NOTES
1. OUT+ is complementary to OUT-. Current is specified as conventional current when flowing into the device.
2. The voltage produced when driving a standard load configuration (37.5ohms).
3. 140 IRE Units = 1.00V.
4. RS-343-A tolerance on all control values is assumed.

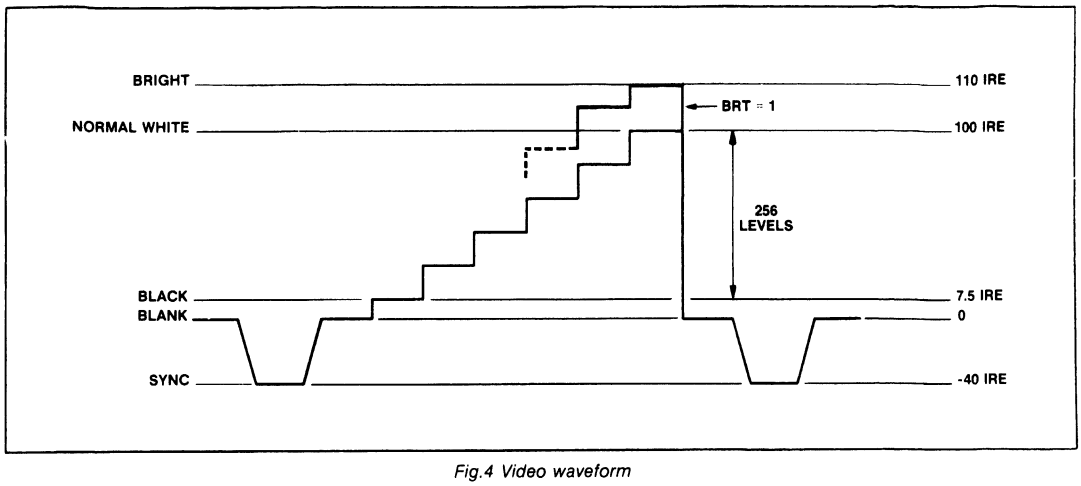



*Fig.4 Video waveform*

## APPLICATIONS

### Board Construction

As the Plessey SP97618 contains a mixture of high speed digital and analog circuitry, care must be taken with ground plane and component placement.

Supply decoupling should be placed close to the device with good high frequency, low loss capacitors. Pins 16 and 17 should be decoupled directly to VEEA (pin 20).

The settling time of the output is aided by matching the loads on the OUT + and OUT- outputs. A 37Ω resistor from pin 19 to ground is shown in the applications diagram.

### FT Input

The feedthrough input, when high, will cause the internal register to become transparent. When using the D to A converter in the transparent mode, it is essential that time skew on the input data is minimised, because this skew will be converted directly to output glitch energy.

### Video Controls

Internal pulldown resistors allow these inputs to be left open circuit when not in use. The pulldown resistors are approximately 40kΩ connected to VEED.

The bright input causes the video information that is above 7.5 IRE to be placed on a pedestal that is 10 IRE units high.

Sync, Blank and Force High cause DC currents at the outputs as specified.

### Convert Signal

The input data and controls are acquired into the register on the rising edge of the CONV (convert) command. The device is designed to accept differential ECL levels from devices such as the Plessey SP1658 voltage controlled multivibrator. Single ended CONV signals can be used if the unused CONV inupt is biased at -1.3V and decoupled close to the device pin. Care should be taken with the termination of lines driving the CONV signal. For long lines or voltage levels that are not ECL, a low cost high speed comparator can be used such as the Plessey SP9680.

### Data Inputs

As the SP97618 contains an input register, (FT = 0) no external latching is required. Single in-line resistors of values 270Ω and 150Ω can be used in the Thevenin configuration (see applications circuit, Fig.5) for the termination of 100Ω twisted pair data input lines.

If long lines are used and the device is in the transparent mode (FT = 1) then two line receivers such as the Plessey SP1692 can be used before the data inputs. Twos complement data can be converted by simply configuring the SP1692 to invert the MSB.

### Multiplying Mode

The output amplitude can be modulated by varying the voltage fed to REF +. This technique is only practical at low modulating frequencies. The multiplying bandwidth is affected by amplitude and the compensation capacitor on pin 16. The circuit will remain stable with this capacitor reduced to 2nF.

### Output Load

To maintain the fast settling time of this device, it is recommended that both outputs are terminated with equal resistance. This is regardless of whether single or differential output drive is required (see Fig.5).

### Output Compliance

The output voltage of the circuit can be DC offset more positive by connecting the OUT + and OUT- loads to a positive voltage (<1.5V).

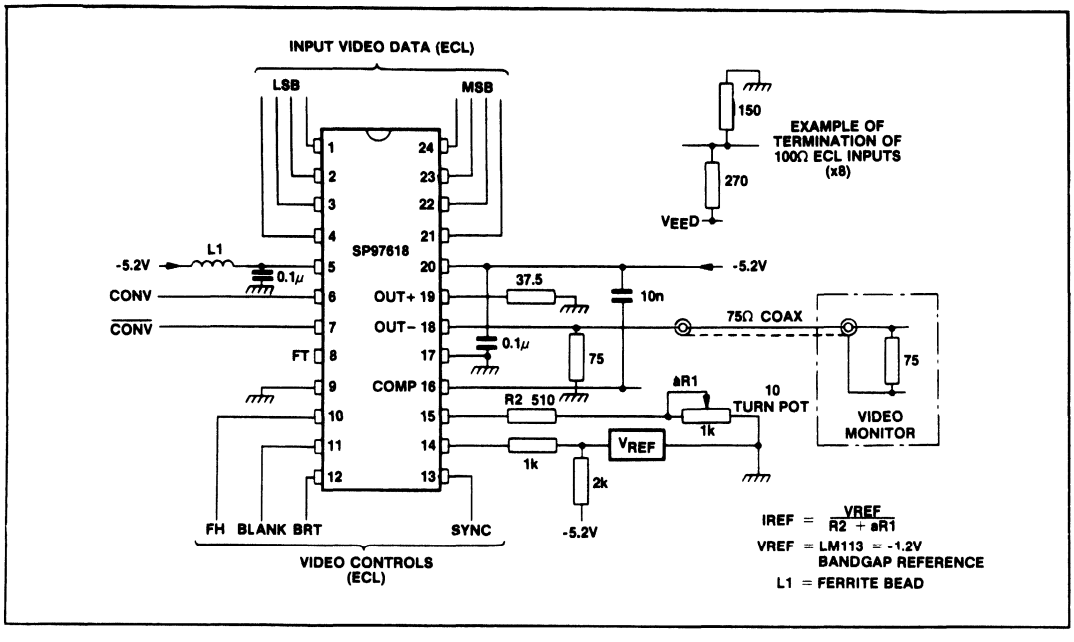



*Fig.5 Application diagram SP97618*

# SP9768

## 8-BIT HIGH SPEED MULTIPLYING D-A CONVERTER

The SP9768 is an ECL 10K compatible 8-bit DAC. The 5nsec settling time allows a 150 megasample per second conversion time. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP9768 design includes a high performance voltage reference and reference amplifier.

Both current and voltage multiplying modes are available.

### FEATURES

- 5ns Settling Time 1 LSB Typically
- 8 Bits ±½ LSB Integral and Differential Linearity
- Current Output
- Operating Temperature Range -30°C to +85°C
- ECL 10K Standard Inputs
- Complementary Outputs, 20mA Full Scale
- Reference Temperature Coefficient Typically 40ppm/°C

### ORDERING INFORMATION

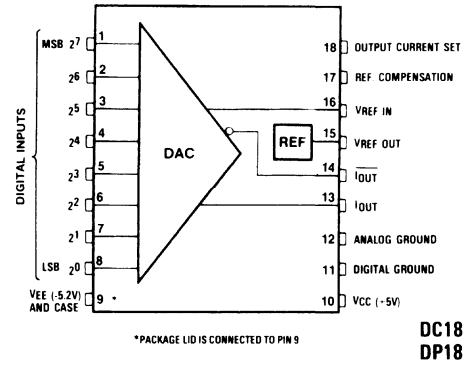
**SP9768DP** (Industrial - Plastic DIL package)
**SP9768DC** (Industrial - Sidebrazed DILMON package)
**SP9768BB DC** (Plessey High Reliability Ceramic DIL package)
**SP9768LC** (Industrial - LCC package)

### APPLICATIONS

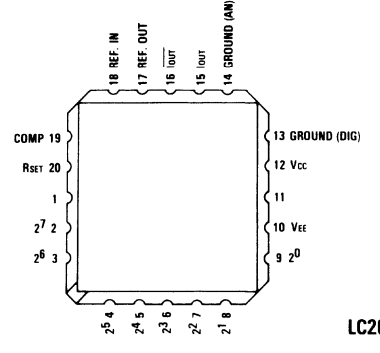
- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems
- ADC Evaluation

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Positive supply voltage | +5.5V |
| Negative supply voltage | -5.7V |
| Digital input voltage | 0 to -4.5V |
| Minimum $R_{SET}$ (from 0V) | 175Ω |
| Maximum $R_{SET}$ | 2.5kΩ |
| Output reference supply ($V_L$) | 0 to +3V |
| Reference input | ±2V |
| Storage temperature range | -65°C to +150°C |
| Operating junction temperature | <175°C |
| Lead temperature (soldering 60 sec) | 300°C |




DC18
DP18




LC20

**NOT TO SCALE**

*Fig.1 Pin connections - top view*

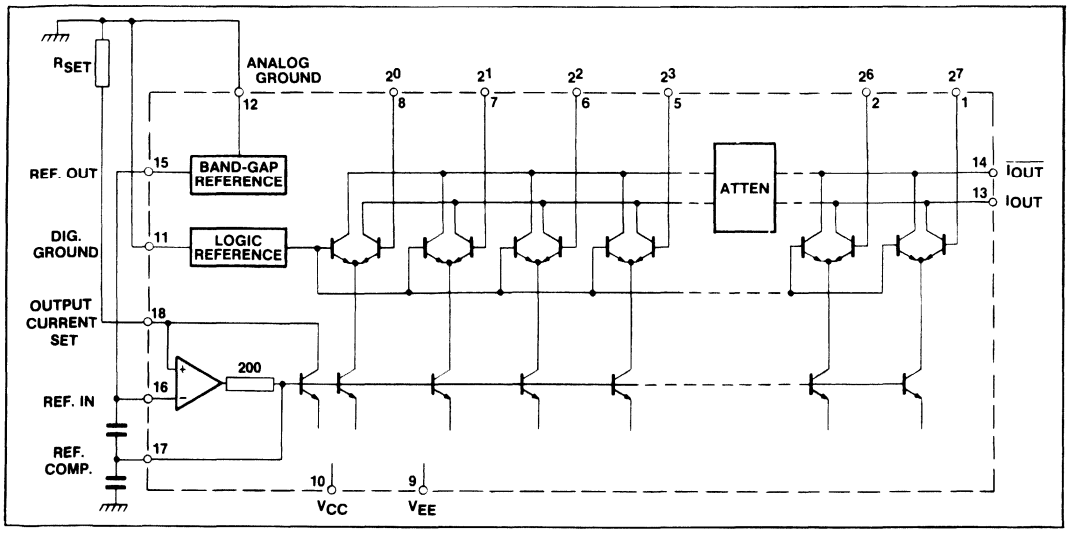



*Fig.2 SP9768 block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25°C; $V_{CC}$ = +5.00V ± 5%; $V_{EE}$ = -5.2V ± 5%; $R_{SET}$ = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

| Characteristic | Value | | | Unit | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Supply current $I_{CC}$ | 7.0 | 12.0 | 20.0 | mA | All inputs at |
| Supply current $I_{EE}$ | 55.0 | 66.0 | 80.0 | mA | -1.8V |
| Logic inputs: | | | | | |
| $V_{IH}$ | -0.96 | | -0.81 | V | Standard ECL |
| $V_{IL}$ | -1.85 | | -1.65 | V | 10K compatible |
| $I_{IN(HI)}$ | | 115 | 200 | μA | All inputs HI |
| Reference voltage $V_{REF}$ | -1.250 | -1.280 | -1.300 | V | |
| Reference voltage temp. coeff. | | 40 | 80 | ppm/°C | -30°C to +85°C |
| Output current - full scale | 2 | | 30 | mA | $R_{SET}$ 2.5kΩ - 175Ω |
| Output current - full scale | 20.2 | 21.3 | 22.4 | mA | $R_{SET}$ = 240Ω |
| Output compliance | -1.0 | | +1.0 | V | $T_{amb}$ = 25°C See |
| | -0.7 | | +1.0 | V | $T_{amb}$ = 85°C Note 4 |
| Bit size (LSB) | 78.9 | 83.2 | 87.5 | μA | Current output |
| Resolution | 8 | | | Bits | |
| | 0.391 | | | % | |
| Integral non-linearity | | | 0.5 | LSB | |
| Differential non-linearity | | | 0.5 | LSB | |
| **Output dynamic parameters (see Note 1)** | | | | | |
| Rise time | | 1.2 | 2.0 | ns | 10 to 90% |
| Settling time - full scale | | 5 | 10 | ns | To 1 LSB |
| Glitch energy | | 90 | 150 | psV | Mid-point |
| Glitch duration | | | 4 | ns | transition |
| Noise output | | -90 | -83 | dBm | See Note 2 |
| **Multiplying mode - voltage (see Fig.5)** (See Note 1) | | | | | |
| Multiplying input voltage range | -2 | | 0 | V | |
| Reference input resistance | | 10 | | kΩ | |
| Multiplying input bandwidth | | 200 | | kHz | -3dB see Note 3 |
| Transfer function non-linearity | | 0.2 | 1.0 | %FS | DC |

| Characteristic | Value | | | Unit | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Multiplying mode - current (see Fig.6)** (See Note 1) | | | | | |
| Multiplying input current range | 0.5 | | 8.0 | mA | |
| Set current input resistance | | 400 | | Ohms | |
| Multiplying input bandwidth | | 20 | | MHz | -3dB |
| Transfer function non-linearity | | 1.0 | 3.0 | %FS | DC |

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. Voltage-mode multiplying bandwidth is limited by the reference compensation capacitor on the loop amplifier output (pin 17). For the minimum recommended value of 3.9nF, the -3dB point is typically 200kHz. However, the loop amplifier output slew rate is asymmetrical at high frequencies; the maximum frequency at which no significant distortion is introduced is typically 35kHz.
4. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.
5. Analog and digital grounds should be connected together at the device pins (pin 11 and pin 12).

## THERMAL CHARACTERISTICS

DC18 $\theta_{JA}$ = 85°C/W $\theta_{JC}$ = 16°C/W
LC20 $\theta_{JA}$ = 73°C/W $\theta_{JC}$ = 22°C/W
DP18 $\theta_{JA}$ = 85°C/W $\theta_{JC}$ = 30°C/W

## APPLICATION

The pinout of the device is shown in Fig.1 External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 20mA, corresponding with a 1 volt drop across a 50Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, $I_{OUT}$, is approximately given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary $I_{OUT}$ is also provided. If single output operation only is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, $R_{SET}$, is typically 240Ω, giving a full-scale output current of 21mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally -1.280 volts and is of a modified bandgap type. Samples show average temperature coefficients of 50ppm/° C over the range -55° C to +125° C. This precision voltage reference can be used as an independent part.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 15 should be decoupled as shown in Fig.4. The current loop technique has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 17 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

Fig.3 shows a suggested circuit for a conventional D to A using the on-chip voltage reference.

## RECOMMENDATION

For low output noise it is best to use a chip capacitor on pin 17 to the 0V (GND) plane. The use of split analog and digital ground planes for this device is not recommended. Eurocard construction is not recommended. Ringing or time skew on digital inputs should be avoided.

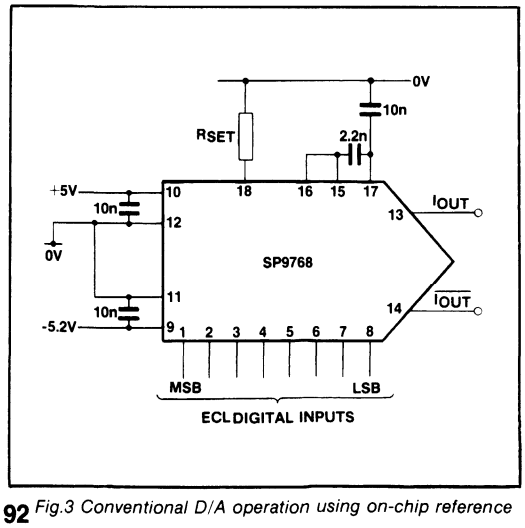



Fig.3 Conventional D/A operation using on-chip reference

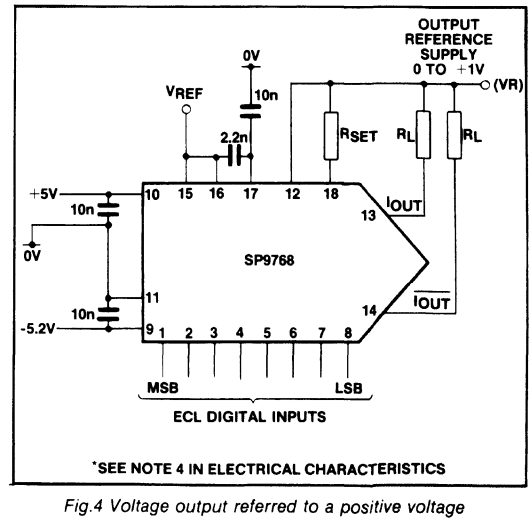



Fig.4 Voltage output referred to a positive voltage

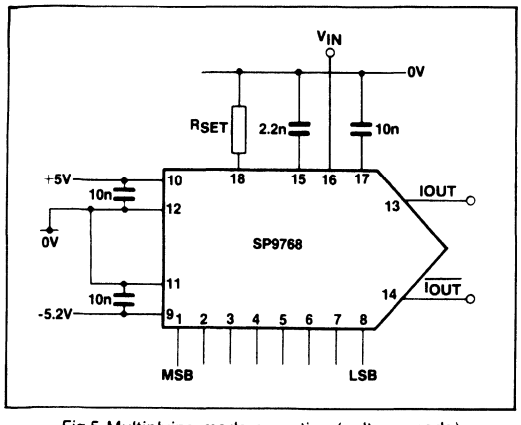



*Fig.5 Multiplying mode operation (voltage mode)*

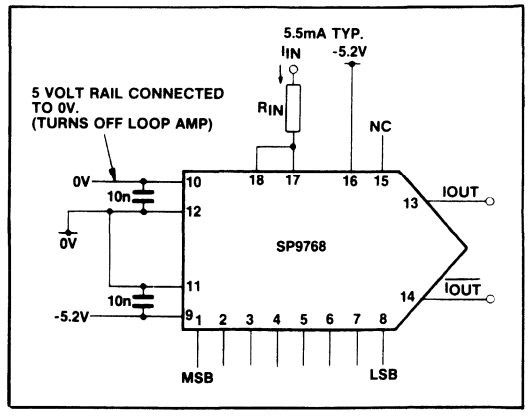



*Fig.6 Multiplying mode operation (current mode)*

## OPERATING NOTES

### Output Compliance

Fig.4 shows the method of using the SP9768 with a load resistor not referred to ground, allowing a larger output swing than the conventional connection of Fig.3. Connecting pin 12 and the current setting resistor $R_{SET}$ to the load reference supply ensures that the scale factor of the output is independent of the load reference.

As pointed out in Note 4 of the Electrical Characteristics, extending the compliance beyond +1V may cause sight degradation of linearity.

### Multiplying Mode

Multiplying operation of the DAC is available in two modes: either a voltage applied in place of the internal reference, or a current supplied via the current set pin.

**Voltage** A circuit for using the DAC in voltage multiplying mode is shown in Fig.5. The transfer function is approximately: $I_{OUT}$ (Full Scale) = 4 x $V_{IN}/R_{SET}$. While this mode offers the best linearity of operation, the frequency response limitations outlined in Note 3 mean that the maximum useable bandwidth is limited to approximately 35kHz.

**Current** A circuit for using the DAC in current multiplying mode is shown in Fig.6. The transfer function is approximately: $I_{OUT}$ (Full Scale) = 4 x $I_{IN}$. In this mode the current setting loop amplifier is not used, and any possibility of instability or interference can be averted by turning off the amplifier by connecting $V_{CC}$ to 0V as shown.

The operational bandwidth of the current input to -3dB is at least 20MHz.

A 1V output is obtained into 50 ohm when a current of approximately 5.5mA is fed into pin 17/18 and the input code is selected for full output current.

# SP9770B & C

## 10-BIT HIGH SPEED MULTIPLYING D-A CONVERTER

The SP9770 is an ECL 10K compatible 10-bit DAC. The 12nsec settling time allows a 75 megasample per second conversion time. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP9770 design includes a high performance voltage reference and reference amplifier.

### FEATURES

- Operating Temperature Range -30°C to +85°C
- 12ns Settling Time 1 LSB Typically
- **SP9770B** 10 Bits ±½ LSB Integral and ±½ LSB Differential Linearity
- **SP9770C** 10 Bits ±½ LSB Integral and ±1 LSB Differential Linearity
- Current Output
- ECL 10K Standard Inputs
- Complementary Outputs, 20mA Full Scale
- Reference Temperature Coefficient Typically 40ppm/°C

### ORDERING INFORMATION

**SP9770B DC** (Industrial - Sidebrazed DILMON package)
**SP9770C DC** (Industrial - Sidebrazed DILMON package)
**SP9770BB DC** (Plessey High Reliability Ceramic DIL package)

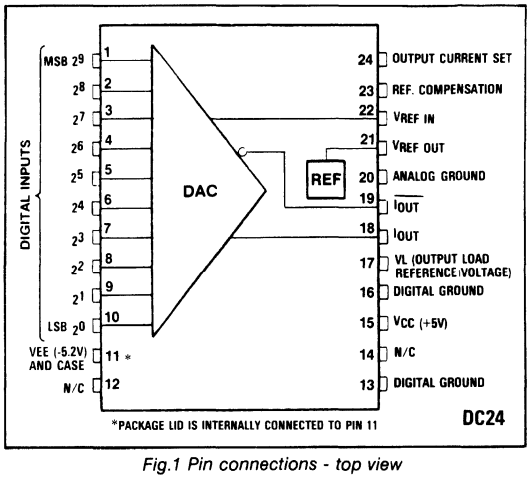



*Fig.1 Pin connections - top view*

### APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems

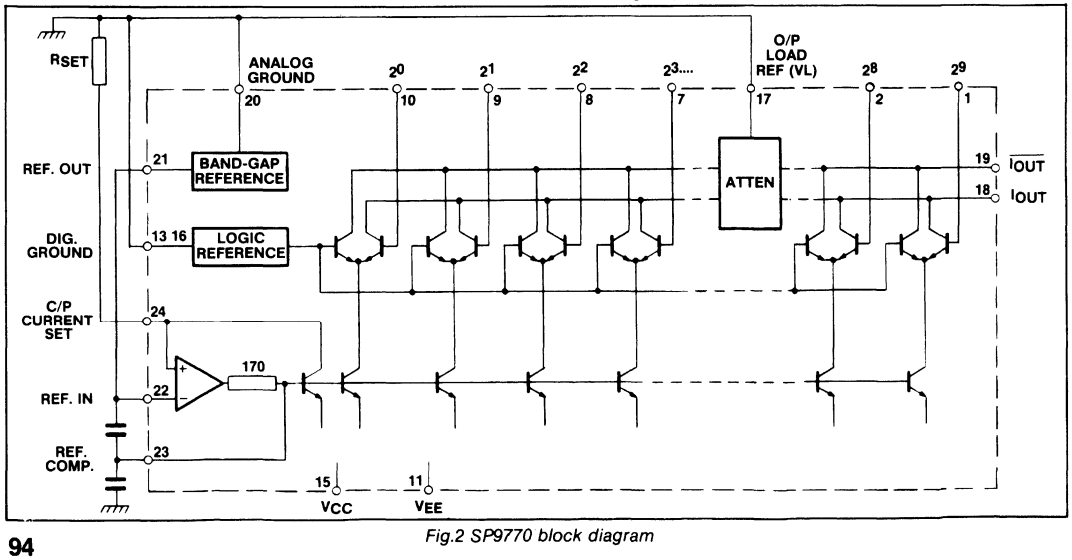



*Fig.2 SP9770 block diagram*

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| Positive supply voltage | +5.5V | Output reference supply ($V_L$) | 0 to +3V |
| Negative supply voltage | -5.7V | Reference input | ±2V |
| Digital input voltage | 0 to -4.5V | Storage temperature range | -65°C to +150°C |
| Minimum $R_{SET}$ (from 0V) | 175Ω | Junction operating temperature | <175°C |
| Maximum $R_{SET}$ | 2.5kΩ | Lead temperature (soldering 60 sec) | 300°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25°C; $V_{CC}$ = +5.00V ± 5%; $V_{EE}$ = -5.2V ± 5%; $R_{SET}$ = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

| Characteristic | Value | | | Unit | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Supply current $I_{CC}$ | 7.0 | 12.0 | 17.0 | mA | All inputs at |
| Supply current $I_{EE}$ | 45.0 | 56.0 | 70.0 | mA | -1.8V |
| Logic inputs: | | | | | |
| $V_{IH}$ | -0.96 | | -0.81 | V | Standard ECL |
| $V_{IL}$ | -1.85 | | -1.65 | V | 10K compatible |
| $I_{IN(HI)}$ | | 115 | 200 | μA | All inputs HI |
| Reference voltage $V_{REF}$ | -1.250 | -1.280 | -1.300 | V | |
| Reference voltage temp. coeff. | | 40 | 80 | ppm/°C | -30°C to +85°C |
| Output current - full scale | 2 | | 30 | mA | $R_{SET}$ 2.5kΩ - 175Ω |
| Output current - full scale | 20.2 | 21.3 | 22.4 | mA | $R_{SET}$ = 240Ω |
| Output compliance | -1.0 | | +1.0 | V | $T_{amb}$ =25°C See |
| | -0.7 | | +1.0 | V | $T_{amb}$ =85°C Note 4 |
| Bit size (LSB) | 19.7 | 20.8 | 21.9 | μA | Current output |
| Resolution | 10 | | | Bits | |
| | 0.098 | | | % | |
| Differential non-linearity | | | 0.5 | LSB | |
| Integral non-linearity | | | 0.5 | LSB | SP9770B |
| | | | 1.0 | LSB | SP9770C |
| **Output dynamic parameters (see Note 1)** | | | | | |
| Rise time | | 2.0 | 3.0 | ns | 10 to 90% |
| Settling time - full scale | | 12 | 20 | ns | To 1 LSB |
| Glitch energy | | 90 | 150 | psV | Mid-point |
| Glitch duration | | | 4 | ns | transition |
| Noise output | | -90 | -83 | dBm | See Note 2 |
| **Multiplying mode - voltage (see Fig.5)** | | | | | |
| Multiplying input voltage range | -2 | | 0 | V | |
| Reference input resistance | | 10 | | kΩ | |
| Multiplying input bandwidth | | 200 | | kHz | -3dB see Note 3 |
| Transfer function non-linearity | | 0.2 | 1.0 | %FS | DC |

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. Voltage-mode multiplying bandwidth is limited by the reference compensation capacitor on the loop amplifier output (pin 23). For the minimum recommended value of 3.9nF, the -3dB point is typically 200kHz. However, the loop amplifier output slew rate is asymmetrical at high frequencies; the maximum frequency at which no significant distortion is introduced is typically 35kHz.
4. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.

Thermal characteristics $\theta_{JA}$ = 65°C/W
$\theta_{JC}$ = 15°C/W

## APPLICATION

The pinout of the device is shown in Fig.1. External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 20mA, corresponding with a 1 volt drop across a 50Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, $I_{OUT}$, is given by

$$I_{OUT} \triangleq 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary $I_{OUT}$ is also provided. If single output operation only is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, $R_{SET}$, is typically 240Ω, giving a full-scale output current of 21mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally -1.280 volts and is of a modified bandgap type. Samples show average temperature coefficients of 50ppm/° C over the range -55° C to +125° C. This precision voltage reference can be used as an independent part.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 21 should be decoupled as shown in Fig.4. The current loop technique has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 23 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

Fig.3 shows a suggested circuit for a conventional D to A using the on-chip voltage reference.

## RECOMMENDATIONS

For low output noise it is best to use a chip capacitor on pin 23 to the 0V (GND) plane. The use of split analog and digital ground planes for this device is not recommended.

For low glitch output it is essential that the input time skew and ringing is minimised. The Plessey SP9210 is a suitable high speed latch for this purpose.

Eurocard construction is not recommended.

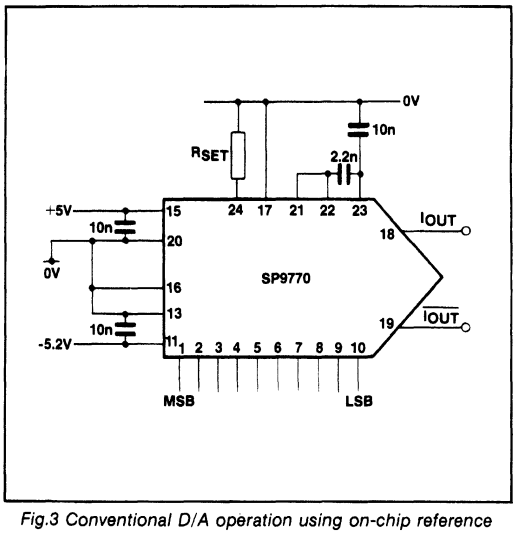



*Fig.3 Conventional D/A operation using on-chip reference*

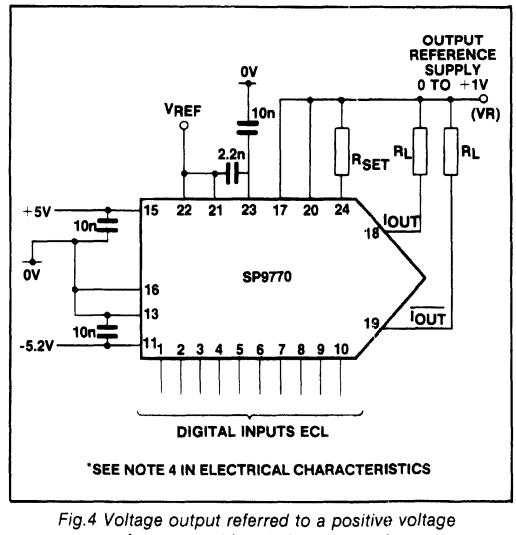



*Fig.4 Voltage output referred to a positive voltage for outputs biased above ground*

## OPERATING NOTES

### Output Compliance

Fig.4 shows the method of using the SP9770 with a load resistor not referred to ground, allowing a larger output swing than the conventional connection of Fig.3. Connecting pins 17 and 20, and the current setting resistor $R_{SET}$ to the load reference supply ensures that the scale factor of the output is independent of the load reference.

As pointed out in Note 4 of the Electrical Characteristics, extending the compliance beyond +1V may cause slight degradation of linearity.

**Voltage multiplying.** A circuit for using the DAC in voltage multiplying mode is shown in Fig.5. The transfer function is approximately: $I_{OUT}$ (Full Scale) = 4 x $V_{IN}/R_{SET}$. While this mode offers the best linearity of operation, the frequency response limitations outlined in Note 3 mean that the maximum useable bandwidth is limited to approximately 35kHz.

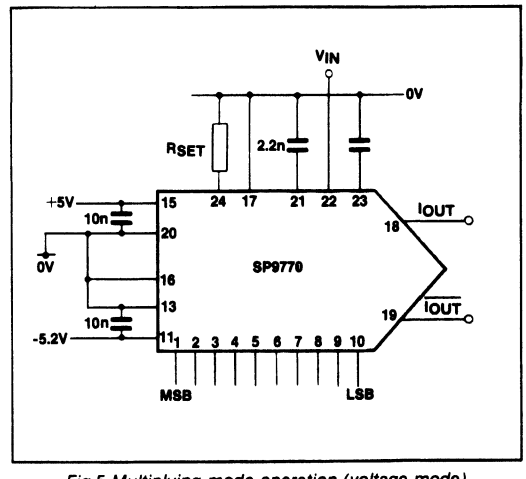



*Fig.5 Multiplying mode operation (voltage mode)*

# SP93808

## SUB-NANOSECOND OCTAL COMPARATOR

The Plessey SP93808 contains eight independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The device also contains circuitry that enables the input hysteresis to be adjusted between 0mV and 10mV by a single external resistor.

Each channel includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. The SP93808 can also be used as two matched quad devices, due to comparators 1 to 4 being clocked separately from comparators 5 to 8.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

### ORDERING INFORMATION

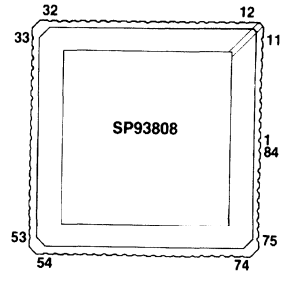
**SP93808B LC** (Industrial - Ceramic LCC package)

### FEATURES

- -40°C to +85°C Temperature Range
- Typical Delay < 1ns
- Adjustable Hysteresis, 0 to 10mV
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 8 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching < 100ps
- High Input Impedance

### APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers




| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | O/P $V_{CC2}$ | 22 | G4 | 43 | I/P $V_{CC1}$ | 64 | +I/P4 |
| 2 | GB | 23 | $\overline{NC}$ | 44 | $V_{MM}$ | 65 | NC |
| 3 | $\overline{NC}$ | 24 | $\overline{Q4}$ | 45 | RES | 66 | -I/P5 |
| 4 | $\overline{Q8}$ | 25 | Q4 | 46 | NC | 67 | +I/P5 |
| 5 | Q8 | 26 | NC | 47 | $\overline{CLK1}$ | 68 | NC |
| 6 | NC | 27 | G3 | 48 | $\overline{CLK1}$ | 69 | -I/P6 |
| 7 | G7 | 28 | $\overline{NC}$ | 49 | NC | 70 | +I/P6 |
| 8 | $\overline{NC}$ | 29 | $\overline{Q3}$ | 50 | $V_{EE1}$ | 71 | NC |
| 9 | $\overline{Q7}$ | 30 | Q3 | 51 | $V_{EE1}$ | 72 | -I/P7 |
| 10 | Q7 | 31 | NC | 52 | HYS | 73 | +I/P7 |
| 11 | NC | 32 | G2 | 53 | NC | 74 | NC |
| 12 | G6 | 33 | $\overline{NC}$ | 54 | -I/P1 | 75 | -I/P8 |
| 13 | $\overline{NC}$ | 34 | $\overline{Q2}$ | 55 | +I/P1 | 76 | +I/P8 |
| 14 | $\overline{Q6}$ | 35 | Q2 | 56 | NC | 77 | NC |
| 15 | Q6 | 36 | NC | 57 | -I/P2 | 78 | $V_{EE2}$ |
| 16 | NC | 37 | G1 | 58 | +I/P2 | 79 | $V_{EE2}$ |
| 17 | G5 | 38 | $\overline{NC}$ | 59 | NC | 80 | $\overline{CLK2}$ |
| 18 | $\overline{NC}$ | 39 | $\overline{Q1}$ | 60 | -I/P3 | 81 | CLK2 |
| 19 | $\overline{Q5}$ | 40 | Q1 | 61 | +I/P3 | 82 | $V_{MM}$ |
| 20 | Q5 | 41 | O/P $V_{CC1}$ | 62 | NC | 83 | I/P $V_{CC2}$ |
| 21 | NC | 42 | O/P $V_{CC1}$ | 63 | -I/P4 | 84 | O/P $V_{CC2}$ |

*Fig.1 Pin connections - top view*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ - $V_{MM}$ | +6V |
| Supply voltage $V_{MM}$ - $V_{EE}$ | -6V |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |
| Output current | ≤30mA |
| Maximum input voltage | |
| Common mode positive | ≤$V_{CC}$ |
| Common mode negative | ≥$V_{EE}$ |
| Differential input voltage | ≤±3.8V |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = -40°C to +85°C, I/P and O/P $V_{CC}$ = +5V ± 0.25V,
$V_{EE}$ = -5.2V ± 0.25V, $V_{MM}$ = 0V (see Fig.4), Load = 50Ω to $V_{CC}$-2V

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 65.5 | 84 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5.2V No load |
| Negative supply current | $I_{EE}$ | | 33.0 | 42 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5.2V No load |
| Positive supply voltage | $V_{CC}$ | I/P MAX +1.55 | 5.0 | I/P MIN +7.3 | V | |
| Negative supply voltage | $V_{EE}$ | -5.5 | -5.2 | -4.9 | V | |
| Input offset voltage | $V_{OS}$ | -3.5 | | +3.5 | mV | |
| Input bias current | $I_B$ | | 5.25 | 9 | μA | |
| Input offset current | $I_{OS}$ | | 0.95 | 1.2 | μA | |
| Input capacitance | $C_I$ | 1.5 | (Note 1) | pF | | |
| Input impedance | $R_I$ | | 250 | | kΩ | Measured at DC |
| Differential input range | $V_{DIF}$ | | | ±3.8 | V | |
| Common mode input range | CMIR | -2.1 | | +2.6 | V | |
| Output voltage high | $V_{OH}$ | $V_{CC}$-1.050 | | $V_{CC}$-0.81 | V | +25°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-1.140 | | $V_{CC}$-0.91 | V | -40°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-0.965 | | $V_{CC}$-0.704 | V | +85°C, $V_{IN}$ > 60mV |
| Output voltage low | $V_{OL}$ | $V_{CC}$-1.712 | | $V_{CC}$-1.544 | V | +25°C, $V_{IN}$ <- 60mV |
| | | $V_{CC}$-1.792 | | $V_{CC}$-1.650 | V | -40°C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.638 | | $V_{CC}$-1.465 | V | +85°C, $V_{IN}$ < -60mV |
| Gain (transparent mode) | | | 26 | | dB | Differential |
| Common mode rejection | CMRR | 50 | 50 | | dB | +25°C, with respect to I/P |
| Supply voltage rejection | PSRR | | 70 | | dB | +25°C, with respect to I/P offset |
| Clock input: | | | | | | |
| Common mode range | CMRC | $V_{MM}$+2V | | $V_{CC}$-1.35V | V | |
| Differential swing | DS | 400 | | 1600 | mV | |

NOTES 1. Guaranteed but not tested.

**Dynamic Characteristics (Note 1)** See dynamic test circuit Fig.9.

| Characteristic | Symbol | Value | | | Units | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Latch setup time | $t_S$ | | 150 | | ps | 10mV overdrive |
| Hold time | $t_H$ | | 600 | | ps | 10mV overdrive |
| Input to Q delay | $t_{PD}$ | | 950 | | ps | 10mV overdrive |
| Latch to Q delay | $t_{LQ}$ | | 1850 | | ps | 10mV overdrive |
| Glitch capture regeneration | $t_{RD}$ | | 900 | | ps | 20mV overdrive at Qn |
| Propagation delay matching | $t_{PDM}$ | -100 | | +100 | ps | Within each device |
| Min. compare pulse width | $t_{PW}$ | | 950 | | ps | 10mV overdrive |
| Min. reset pulse width | $t_{RM}$ | | 800 | | ps | |
| Max. flip flop reset time | $t_{RR}$ | | 800 | | ps | |
| Min. hold time of Qn after reset | $t_{GH}$ | | 800 | | ps | |
| Delay between Gn and Qn | $t_{DQ}$ | | 900 | | ps | |
| Propagation delay Gn to reset | $t_{GR}$ | | 800 | | ps | |

NOTES 1 Guaranteed but not tested.

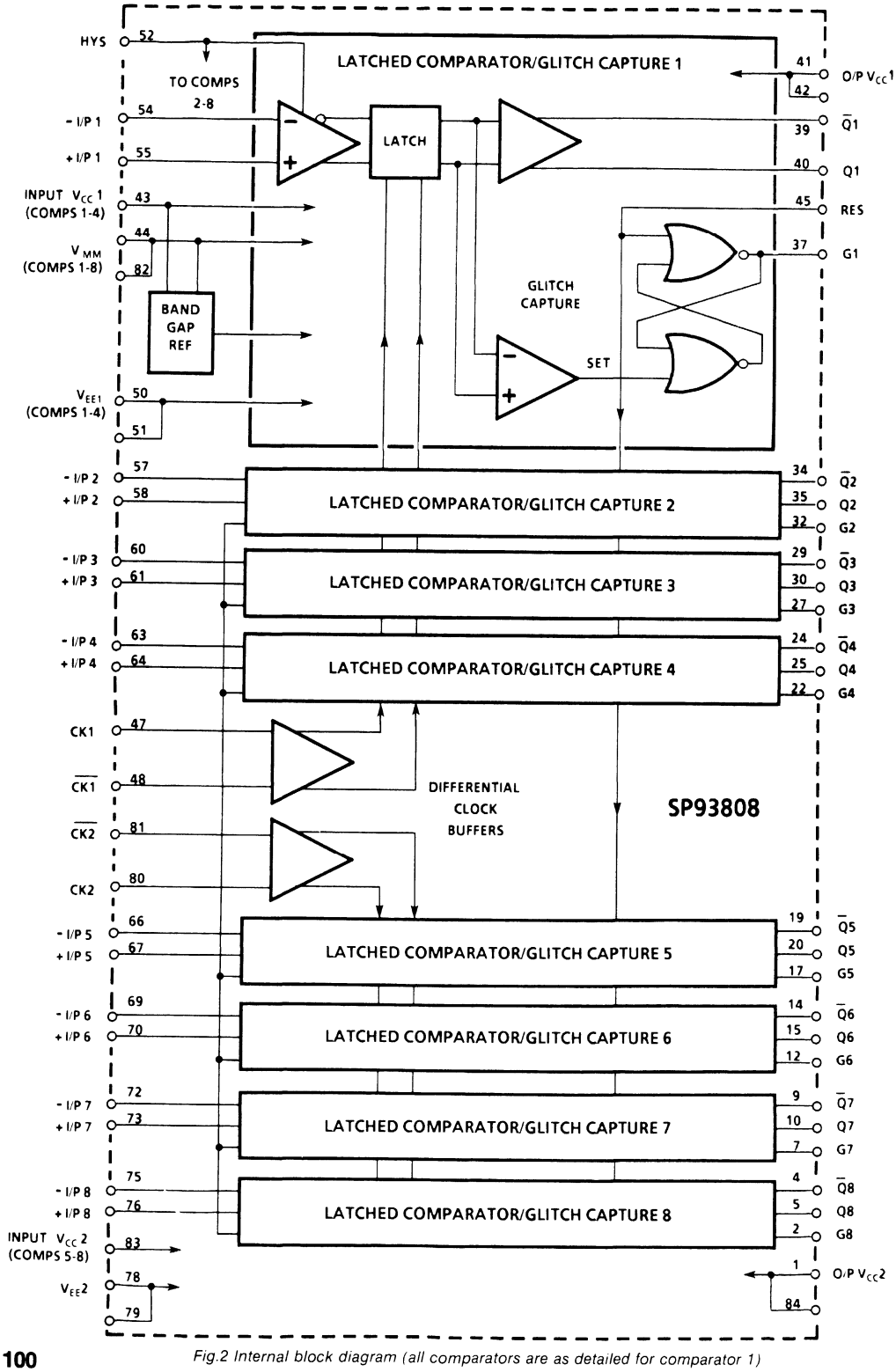



*Fig.2 Internal block diagram (all comparators are as detailed for comparator 1)*

## PIN FUNCTIONS

| Name | Pin | Description |
|---|---|---|
| I/P $V_{CC}1$ | 43 | Positive supply connection for comparators 1 to 4, and the bandgap reference. |
| O/P $V_{CC}1$ | 41 & 42 | Positive supply connection for the outputs Qn and Gn of comparators 1 to 4 (emitter follower outputs, see Fig.5). |
| I/P $V_{CC}2$ | 83 | Positive supply connection for comparators 5 to 8. |
| O/P $V_{CC}2$ | 1 & 84 | Positive supply connection for the outputs Qn, Qn and Gn of comparators 5 to 8 (emitter follower outputs, see Fig.5). |
| -I/Pn<br>+I/Pn | 54/55, 57/58, 60/61, 63/64, 66/67, 69/70, 72/73, 75/76 | Inverting and non-inverting inputs to comparators 1 to 8, respectively. |
| Qn/$\overline{Qn}$ | 40/39, 35/34, 30/29, 25/24, 20/19, 15/14, 10/9, 5/4 | Q and $\overline{Q}$ outputs of comparators 1 to 8, respectively. |
| Gn | 37,32,27,22, 17,12,7,2 | Outputs of glitch capture circuits 1 to 8, respectively. |
| RES | 45 | Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'. |
| CLK1, $\overline{CLK1}$ | 47,48 | Clock input pins for comparators 1 to 4. ECL active low signal which latches the outputs of comparators 1 to 4. |
| CLK2, $\overline{CLK2}$ | 80,81 | Clock input pins for comparators 5 to 8. ECL active low signal which latches the outputs of comparators 5 to 8. |
| $V_{EE}1$ | 50 & 51 | Negative supply voltage for comparators 1 to 4. |
| $V_{EE}2$ | 78 & 79 | Negative supply voltage for comparators 5 to 8. |
| HYS | 52 | Hysteresis control pin. A pull-up resistor ($R_H$) is required to set the input hysteresis window for all comparators. |
| $V_{MM}$ | 44,82 | Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref. |

## OPERATING NOTES

### Transparent Mode

The SP93808 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 26dB. In this mode, for example, a 10mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93808 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

### Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

### Supply Connections

The SP93808 operates from supply voltages of 0V, -5.2V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from $V_{CC}$, then to interface with other ECL circuits directly, supplies of 0V, -5.2V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage ($V_{MM}$), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

Note that the O/P $V_{CC}$ pins are connected to the collectors of the output emitter followers; load return currents should therefore be directed towards these device pins.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5.2V supply is not available.

The SP93808 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5.2V rails.

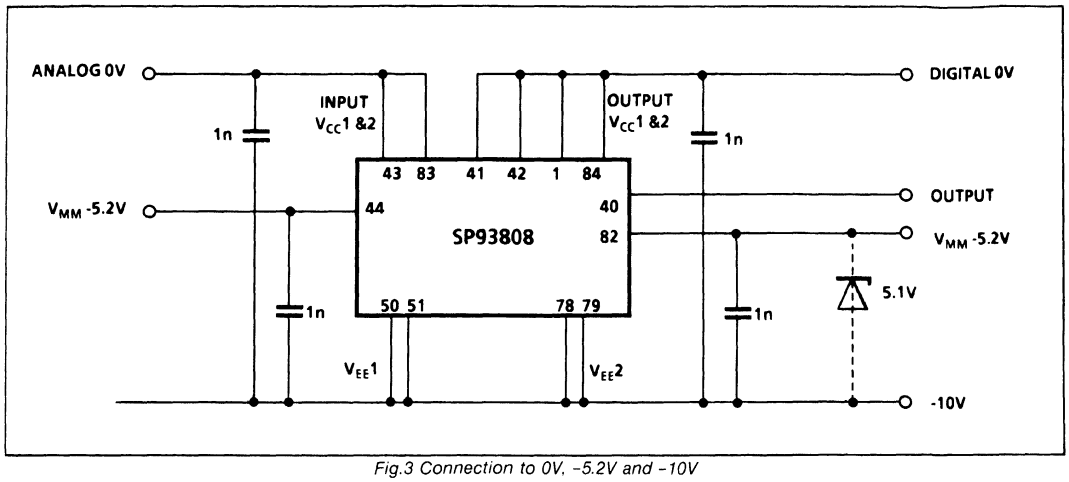



*Fig.3 Connection to 0V, -5.2V and -10V*

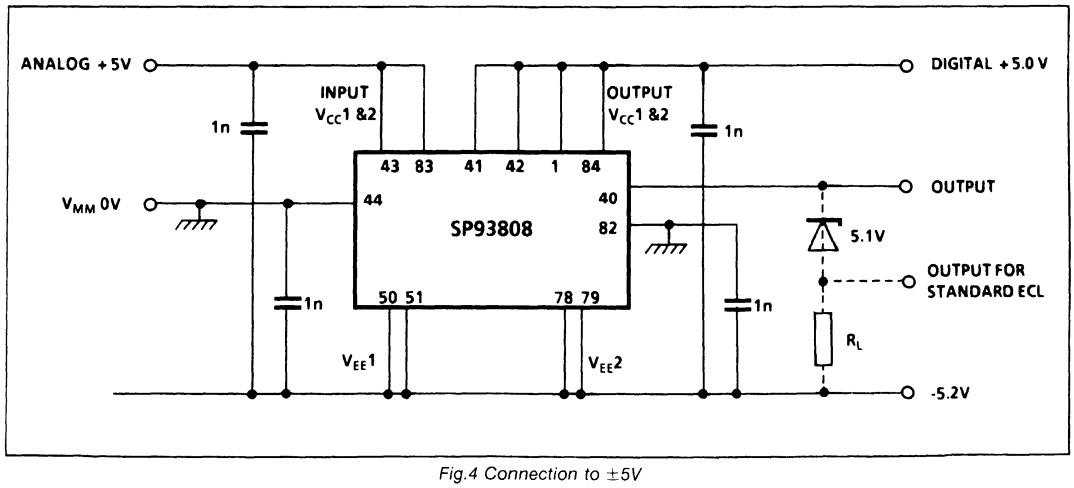



*Fig.4 Connection to ±5V*

## External Components

The Qn, $\overline{Qn}$ and Gn outputs are open emitters and therefore required external pulldown resistors ($R_L$). These resistors may be in the range of 50-250Ω connected to $V_{CC}$-2V ($V_T$) or 250-2000Ω connected to $V_{MM}$.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and $V_{EE}$ is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

## Hysteresis Control

The SP93808 incorporates adjustable hysteresis. The input window is simply controlled by the current flowing into the HYS input (pin 52). The following expression can be used to determine the value of this resistor for a defined amount of symmetrical hysteresis at the input ($V_{HYS}$). See Fig.6.

$$R_H = \frac{|V_{CC} - V_{EE}| - 0.8 - 75V_{HYS}}{0.64V_{HYS}} \Omega$$

where: $V_{CC}$ = +Supply voltage (V)
$V_{EE}$ = -Supply voltage (V)
$V_{HYS}$ = Required peak-to-peak hysteresis window at the input (V)

Note that for zero hysteresis the HYS pin should be connected to $V_{EE}1$; $R_H$ minimum is 500Ω.

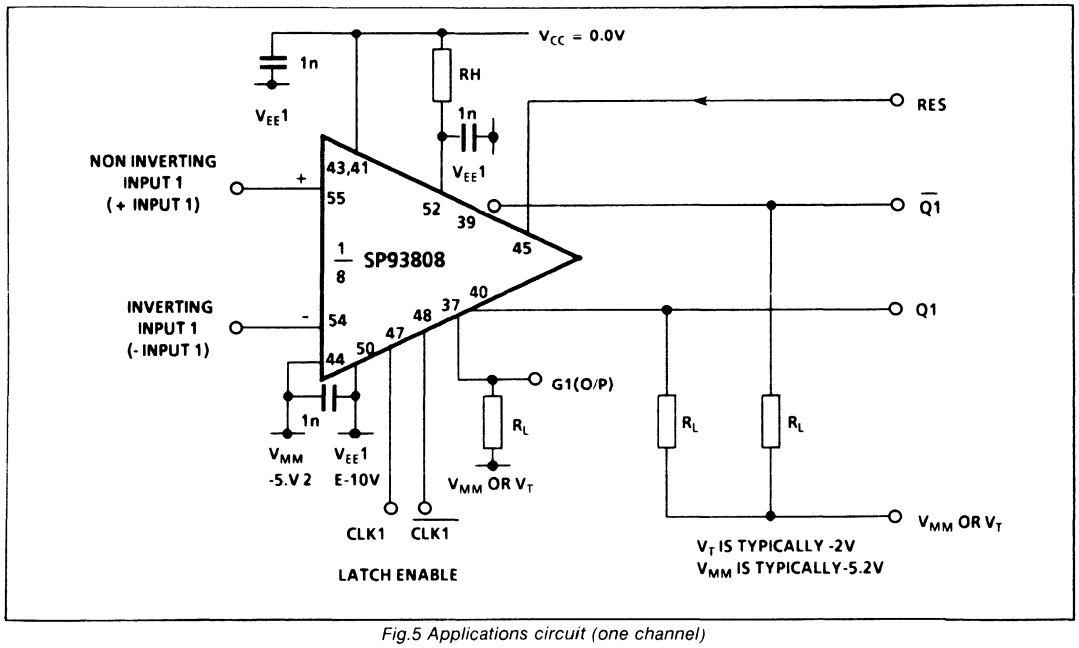



*Fig.5 Applications circuit (one channel)*

## Clock Inputs

The SP93808 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as a dual quad comparator as comparators 1 to 4 can be clocked separately from comparators 5 to 8.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device $V_{CC}$ connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

CLK1 (pin 47) comparators 1 to 4 latch when low.
$\overline{CLK1}$ (pin 48) inverse clock for comparators 1 to 4.
CLK2 (pin 81) comparators 5 to 8 latch when low.
$\overline{CLK2}$ (pin 80) inverse clock for comparators 5 to 8.

The clock inputs should have fast rise times and low jitter. The Plessey SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator.

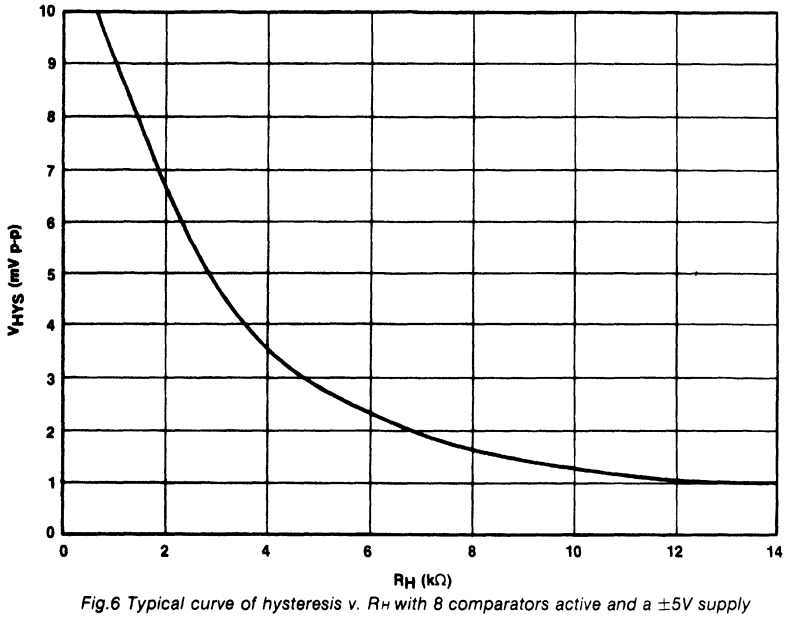



*Fig.6 Typical curve of hysteresis v. $R_H$ with 8 comparators active and a ±5V supply*

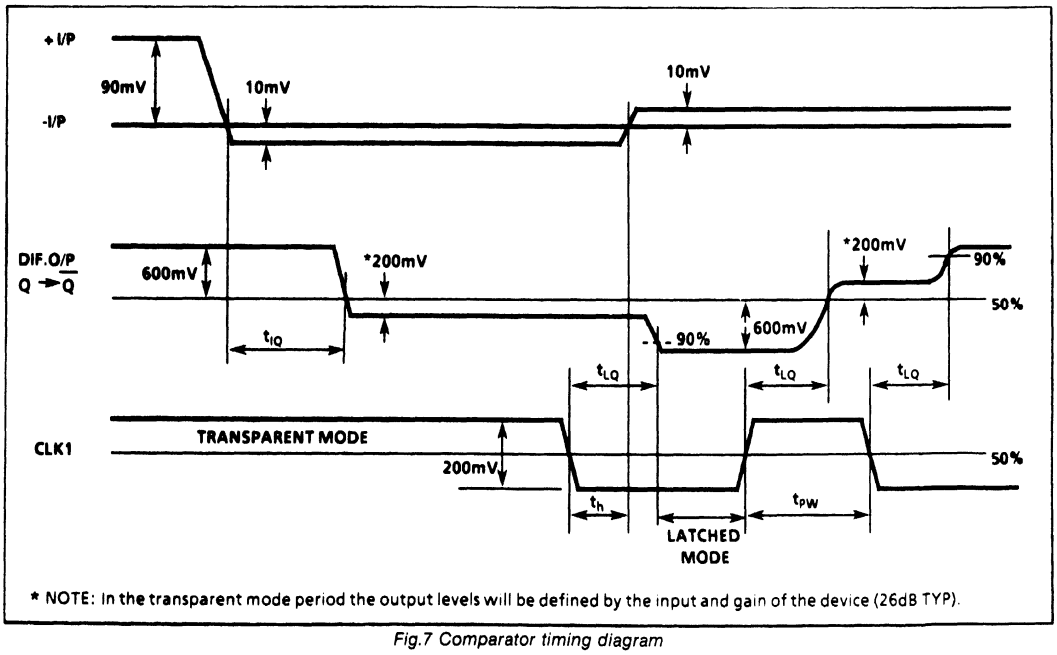



*Fig.7 Comparator timing diagram*

| I/P | CLK | Qn + 1 |
|---|---|---|
| X | 0 | Qn |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

X = Don't Care

*Table 1 Truth table for comparator*

### Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' ($V_{CC}$-0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn outpt will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

| RES | SET(1) (n + 1) | Gn + 1 |
|---|---|---|
| 1 | X | 0 |
| 0 | ⌐ | ⌐ |
| 0 | ¬ | 1 |
| 0 | 1 | 1 |
| 0 | 0 | Gn(2) |
| ¬ | 1 | ⌐ |
| ¬ | 0 | 0 |

X = Don't Care

*Table 2 Truth table for glitch capture circuit*

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.9.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

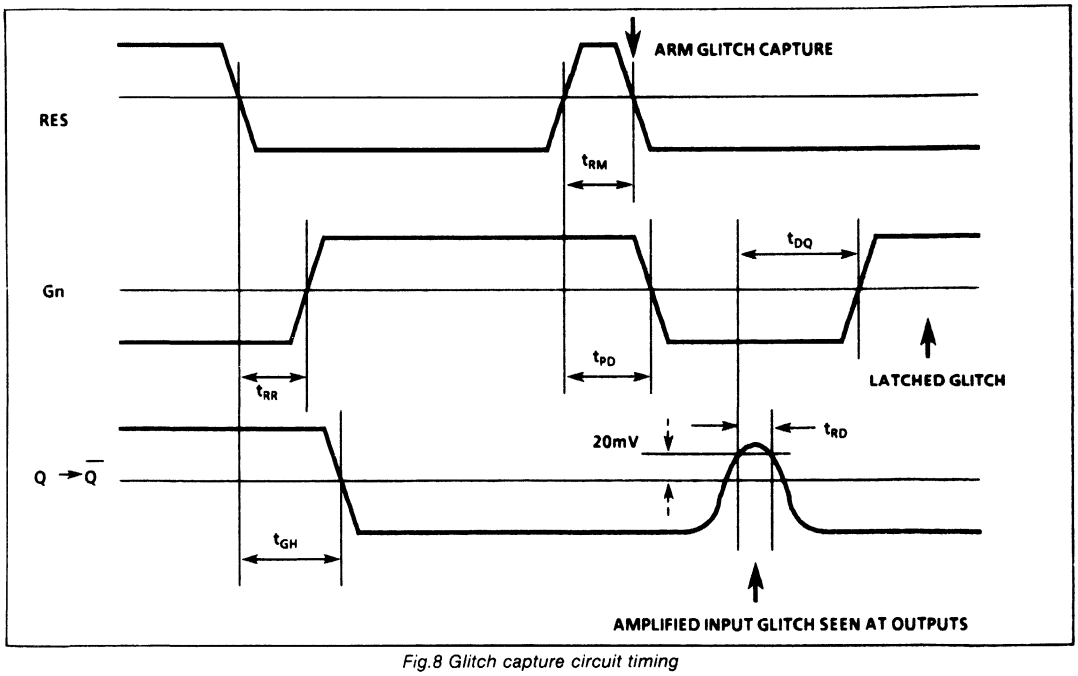
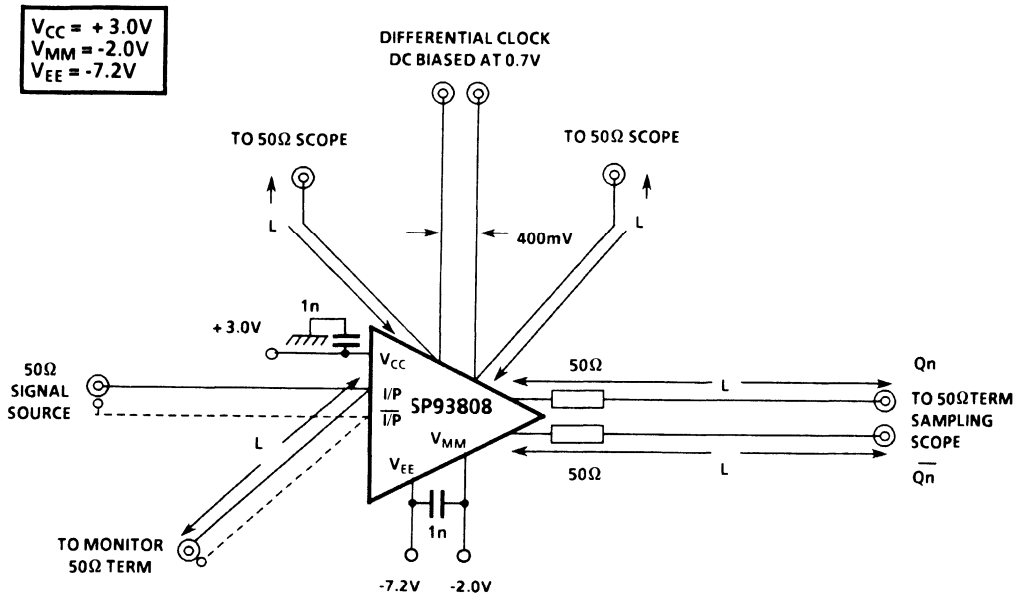



*Fig.8 Glitch capture circuit timing*




NOTES:-

The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) A Plessey SP92701 can be used with supplies of + 3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

*Fig.9 Comparator dynamic test circuit (one channel)*

# SP93804

## SUB-NANOSECOND QUAD COMPARATOR/GLITCH DETECTOR

The Plessey SP93804 contains four independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The device also contains circuitry that enables the input hysteresis to be adjusted between 0mV and 10mV by a single external resistor.

Each channel includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. The SP93804 can also be used as two matched dual devices, due to comparators 1 and 2 being clocked separately from comparators 5 and 4.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

### ORDERING INFORMATION

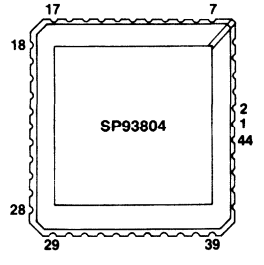
**SP93804B LC** (Industrial - Ceramic LCC package)

### FEATURES

- -40°C to +85°C Temperature Range
- Typical Delay < 1ns
- Adjustable Hysteresis, 0 to 10mV
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 4 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching <100ps
- High Input Impedance

### APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers




LC44

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | I/P Vcc2 | 12 | NC | 23 | VMM | 34 | NC |
| 2 | O/P Vcc2 | 13 | G2 | 24 | RES | 35 | -I/P3 |
| 3 | G4 | 14 | NC | 25 | CLK1 | 36 | +I/P3 |
| 4 | NC | 15 | Q2 | 26 | $\overline{CLK1}$ | 37 | NC |
| 5 | $\overline{Q4}$ | 16 | $\overline{Q2}$ | 27 | VEE1 | 38 | -I/P4 |
| 6 | $\overline{Q4}$ | 17 | NC | 28 | HYS | 39 | +I/P4 |
| 7 | NC | 18 | G1 | 29 | -I/P1 | 40 | NC |
| 8 | G3 | 19 | Q1 | 30 | +I/P1 | 41 | VEE2 |
| 9 | NC | 20 | $\overline{Q1}$ | 31 | NC | 42 | CLK2 |
| 10 | Q3 | 21 | O/P Vcc1 | 32 | -I/P2 | 43 | $\overline{CLK2}$ |
| 11 | $\overline{Q3}$ | 22 | I/P Vcc1 | 33 | +I/P2 | 44 | VMM |

*Fig.1 Pin connections - top view*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage Vcc - VMM | +6V |
| Supply voltage VMM - VEE | -6V |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |
| Output current | ≤30mA |
| Maximum input voltage | |
| Common mode positive | ≤Vcc |
| Common mode negative | ≥VEE |
| Differential input voltage | ≤±3.8V |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = -40°C to +85°C, I/P and O/P $V_{CC}$ = +5V ± 0.25V,
$V_{EE}$ = -5.2V ± 0.25V, $V_{MM}$ = 0V (see Fig.4), Load = 50Ω to $V_{CC}$-2V

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 38.5 | 50 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5.2V No load |
| Negative supply current | $I_{EE}$ | | 16.0 | 21 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5.2V No load |
| Positive supply voltage | $V_{CC}$ | I/P MAX +1.55 | 5.0 | I/P MIN +7.3 | V | |
| Negative supply voltage | $V_{EE}$ | -5.5 | -5.2 | -4.9 | V | |
| Input offset voltage | $V_{OS}$ | -3.5 | | +3.5 | mV | |
| Input bias current | $I_B$ | | 5.25 | 9 | μA | |
| Input offset current | $I_{OS}$ | | 0.95 | 1.2 | μA | |
| Input capacitance | $C_I$ | | 1.5 (Note 1) | | pF | |
| Input impedance | $R_I$ | | 250 | | kΩ | Measured at DC |
| Differential input range | $V_{DIF}$ | | | ±3.8 | V | |
| Common mode input range | CMIR | -2.1 | | +2.6 | V | |
| Output voltage high | $V_{OH}$ | $V_{CC}$-1.050 | | $V_{CC}$-0.81 | V | +25°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-1.140 | | $V_{CC}$-0.91 | V | -40°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-0.965 | | $V_{CC}$-0.704 | V | +85°C, $V_{IN}$ > 60mV |
| Output voltage low | $V_{OL}$ | $V_{CC}$-1.712 | | $V_{CC}$-1.544 | V | +25°C, $V_{IN}$ <- 60mV |
| | | $V_{CC}$-1.792 | | $V_{CC}$-1.650 | V | -40°C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.638 | | $V_{CC}$-1.465 | V | +85°C, $V_{IN}$ < -60mV |
| Gain (transparent mode) | | | 26 | | dB | Differential |
| Common mode rejection | CMRR | | 50 | | dB | +25°C, with respect to I/P |
| Supply voltage rejection | PSRR | | 70 | | dB | +25°C, with respect to I/P offset |
| Clock input: | | | | | | |
| Common mode range | CMRC | $V_{MM}$+2V | | $V_{CC}$-1.35V | V | |
| Differential swing | DS | 400 | | 1600 | mV | |

NOTES 1. Guaranteed but not tested.

**Dynamic Characteristics (Note 1)**

See dynamic test circuit Fig.9.

| Characteristic | Symbol | Value | | | Units | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Latch setup time | $t_S$ | | 150 | | ps | 10mV overdrive |
| Hold time | $t_H$ | | 600 | | ps | 10mV overdrive |
| Input to Q delay | $t_{PD}$ | | 950 | | ps | 10mV overdrive |
| Latch to Q delay | $t_{LQ}$ | | 1850 | | ps | 10mV overdrive |
| Glitch capture regeneration | $t_{RD}$ | | 900 | | ps | 20mV overdrive at Qn |
| Propagation delay matching | $t_{PDM}$ | -100 | | +100 | ps | Within each device |
| Min. compare pulse width | $t_{PW}$ | | 950 | | ps | 10mV overdrive |
| Min. reset pulse width | $t_{RM}$ | | 800 | | ps | |
| Max. flip flop reset time | $t_{RR}$ | | 800 | | ps | |
| Min. hold time of Qn after reset | $t_{GH}$ | | 800 | | ps | |
| Delay between Gn and Qn | $t_{DQ}$ | | 900 | | ps | |
| Propagation delay Gn to reset | $t_{GR}$ | | 800 | | ps | |

NOTES 1 Guaranteed but not tested.

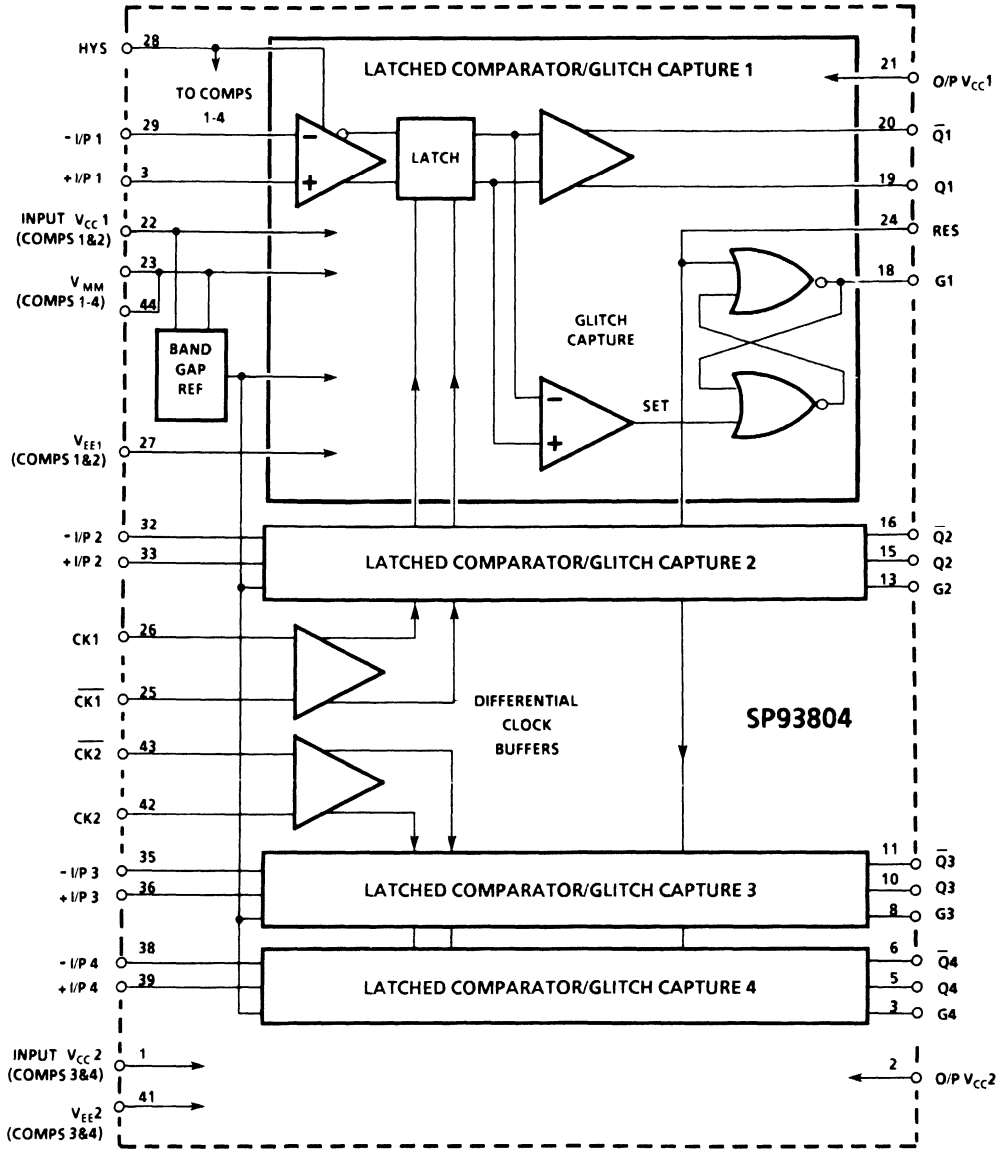



*Fig.2 Internal block diagram (all comparators are as detailed for comparator 1)*

## PIN FUNCTIONS

| Name | Pin | Description |
|---|---|---|
| I/P $V_{CC}1$ | 22 | Positive supply connection for comparators 1 and 2, and the bandgap reference. |
| O/P $V_{CC}1$ | 21 | Positive supply connection for the outputs Qn and Gn of comparators 1 and 2 (emitter follower outputs, see Fig.5). |
| I/P $V_{CC}2$ | 1 | Positive supply connection for comparators 3 and 4. |
| O/P $V_{CC}2$ | 2 | Positive supply connection for the outputs Qn, Qn and Gn of comparators 3 and 8 (emitter follower outputs, see Fig.5). |
| -I/Pn<br>+I/Pn | 29/20, 32/33,<br>35/36, 38/39 | Inverting and non-inverting inputs to comparators 1 to 4, respectively. |
| Qn/$\overline{Qn}$ | 19/20, 15/16,<br>10/11, 5/6, | Q and $\overline{Q}$ outputs of comparators 1 to 4, respectively. |
| Gn | 18,13,8,3 | Outputs of glitch capture circuits 1 to 4, respectively. |
| RES | 24 | Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'. |
| CLK1, $\overline{CLK1}$ | 25,26 | Clock input pins for comparators 1 and 2. ECL active low signal which latches the outputs of comparators 1 and 2. |
| CLK2, $\overline{CLK2}$ | 42,43 | Clock input pins for comparators 3 and 4. ECL active low signal which latches the outputs of comparators 3 and 4. |
| $V_{EE}1$ | 27 | Negative supply voltage for comparators 1 and 2. |
| $V_{EE}2$ | 41 | Negative supply voltage for comparators 3 and 4. |
| HYS | 28 | Hysteresis control pin. A pull-up resistor ($R_H$) is required to set the input hysteresis window for all comparators. |
| $V_{MM}$ | 23,44 | Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref. |

## OPERATING NOTES

### Transparent Mode

The SP93804 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 26dB. In this mode, for example, a 10mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93804 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

### Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

### Supply Connections

The SP93804 operates from supply voltages of 0V, -5.2V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from $V_{CC}$, then to interface with other ECL circuits directly, supplies of 0V, -5.2V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage ($V_{MM}$), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

Note that the O/P $V_{CC}$ pins are connected to the collectors of the output emitter followers; load return currents should therefore be directed towards these device pins.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5.2V supply is not available.

The SP93804 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5.2V rails.

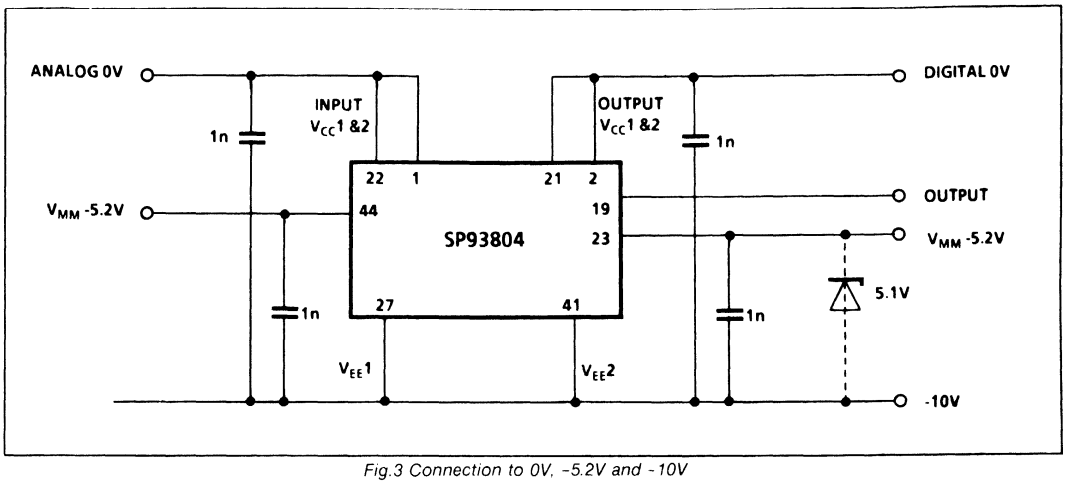



*Fig.3 Connection to 0V, -5.2V and -10V*

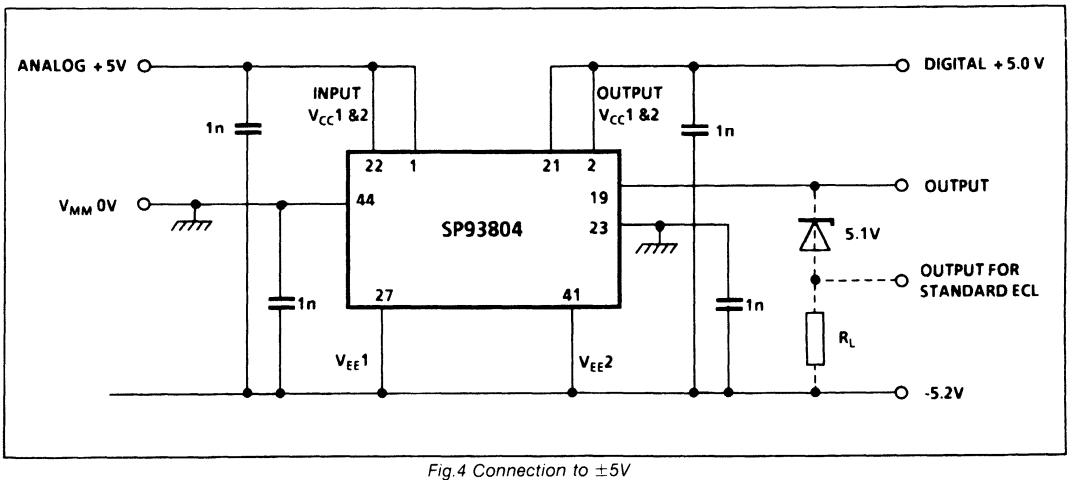



*Fig.4 Connection to ±5V*

## External Components

The Qn, $\overline{Q}$n and Gn outputs are open emitters and therefore required external pulldown resistors ($R_L$). These resistors may be in the range of 50-250Ω connected to $V_{CC}$-2V ($V_T$) or 250-2000Ω connected to $V_{MM}$.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and $V_{EE}$ is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

## Hysteresis Control

The SP93804 incorporates adjustable hysteresis. The input window is simply controlled by the current flowing into the HYS input (pin 28). The following expression can be used to determine the value of this resistor for a defined amount of symmetrical hysteresis at the input ($V_{HYS}$). See Fig.6.

$$R_H = \frac{|V_{CC} - V_{EE}| - 0.8 - 75V_{HYS}}{0.32V_{HYS}} \ \Omega$$

where: $V_{CC}$ = +Supply voltage (V)
$V_{EE}$ = -Supply voltage (V)
$V_{HYS}$ = Required peak-to-peak hysteresis window at the input (V)

Note that for zero hysteresis the HYS pin should be connected to $V_{EE}1$; $R_H$ minimum is 200Ω.

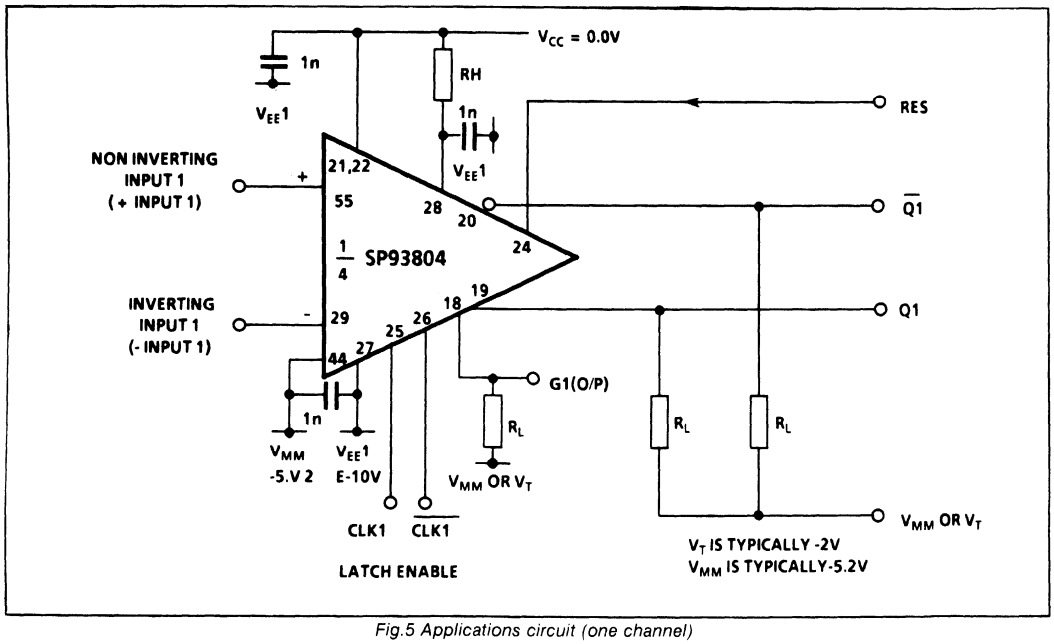



*Fig.5 Applications circuit (one channel)*

## Clock Inputs

The SP93804 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as two dual comparators as comparators 1 and 2 can be clocked separately from comparators 3 and 4.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device $V_{CC}$ connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

$\overline{CLK1}$ (pin 25) comparators 1 and 2 latch when low.
$\overline{CLK1}$ (pin 26) inverse clock for comparators 1 and 2.
$\overline{CLK2}$ (pin 42) comparators 3 and 4 latch when low.
$\overline{CLK2}$ (pin 43) inverse clock for comparators 3 and 4.

The clock inputs should have fast rise times and low jitter. The Plessey SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator.

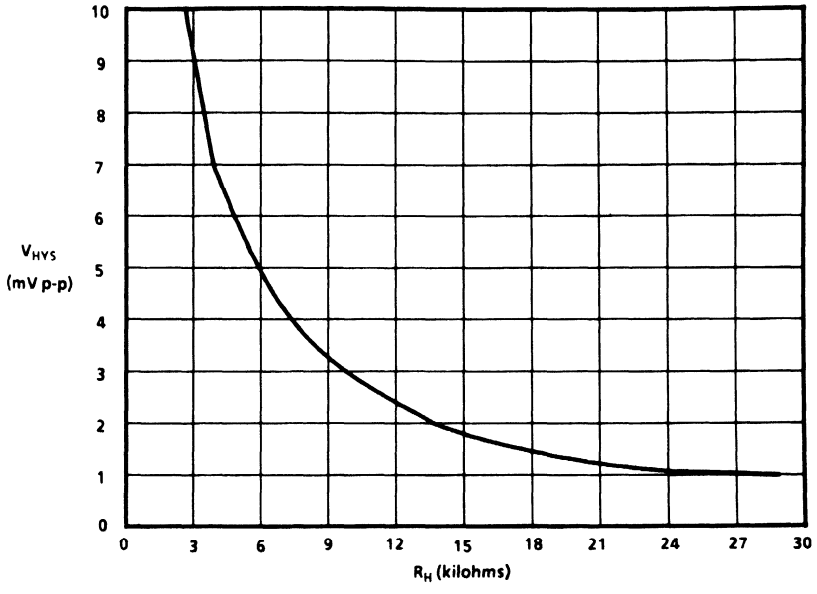
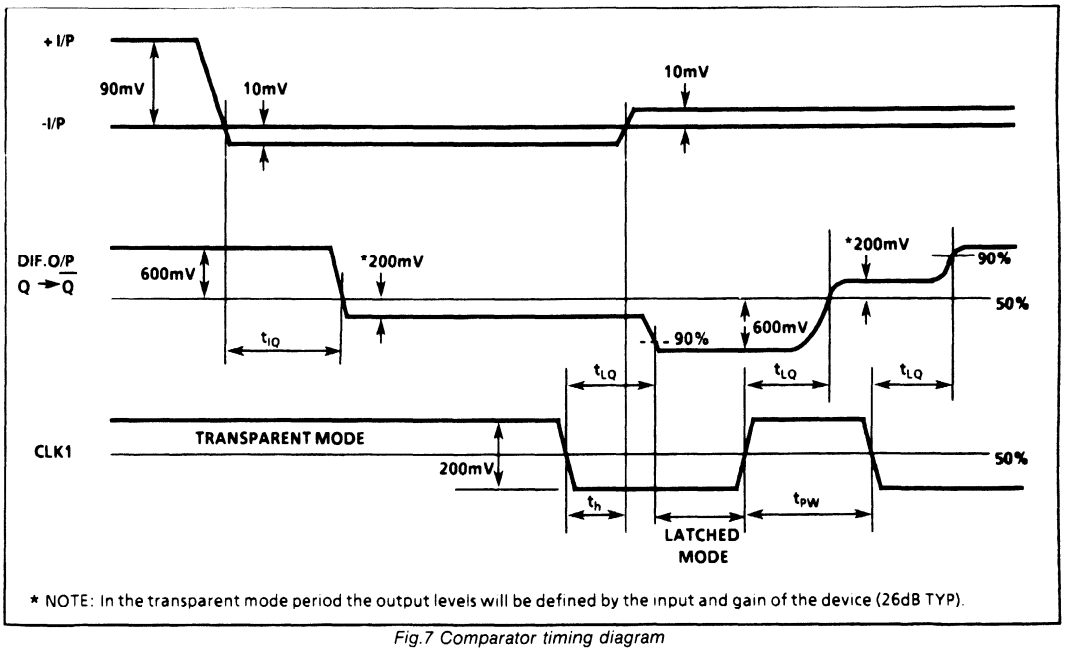



*Fig.6 Typical curve of hysteresis v. $R_H$ with all comparators active and a 10V supply*




* NOTE: In the transparent mode period the output levels will be defined by the input and gain of the device (26dB TYP).

*Fig.7 Comparator timing diagram*

| I/P | CLK | Qn + 1 |
|---|---|---|
| X | 0 | Qn |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

X = Don't Care

*Table 1 Truth table for comparator*

## Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' ($V_{CC}$-0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn outpt will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

| RES | SET(1) (n + 1) | Gn + 1 |
|---|---|---|
| 1 | X | 0 |
| 0 | ↗ | ↗ |
| 0 | ↘ | 1 |
| 0 | 1 | 1 |
| 0 | 0 | Gn(2) |
| ↘ | 1 | ↗ |
| ↘ | 0 | 0 |

X = Don't Care

*Table 2 Truth table for glitch capture circuit*

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.9.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

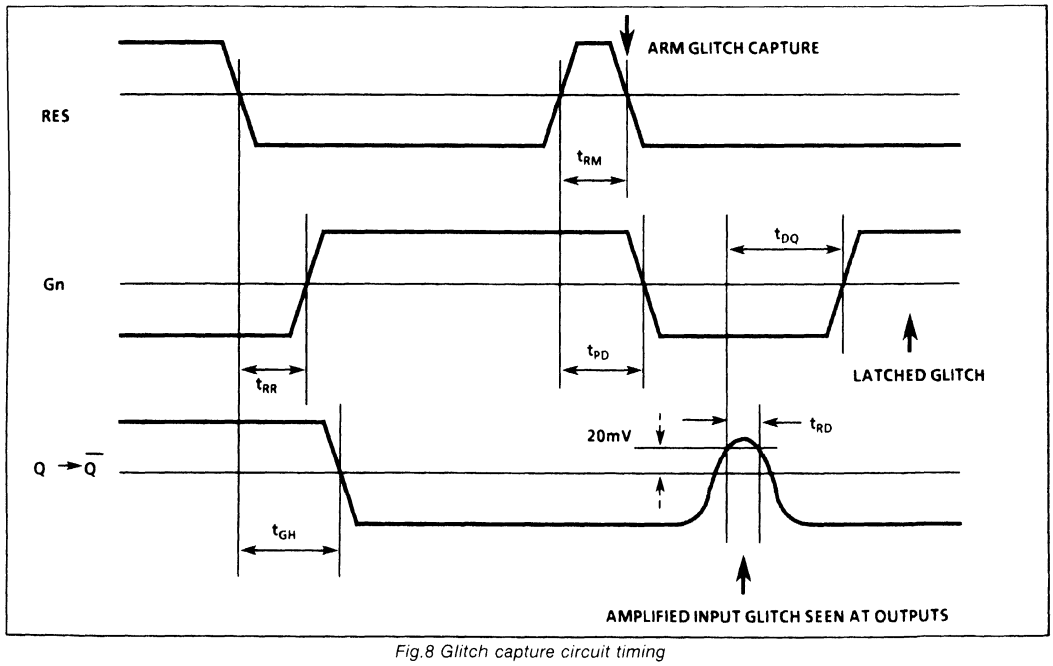
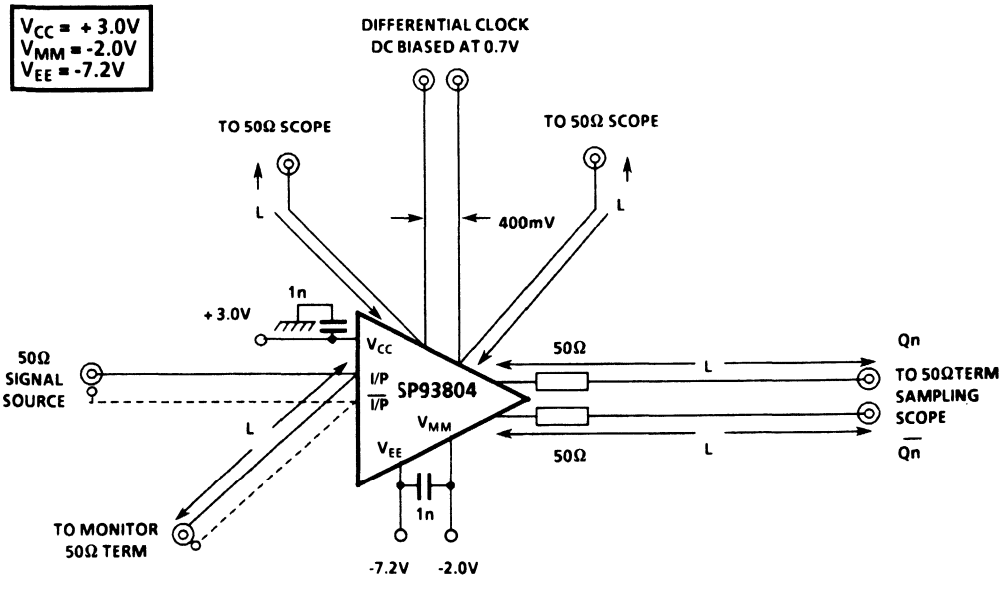



*Fig.8 Glitch capture circuit timing*




NOTES:-

The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) A Plessey SP92701 can be used with supplies of +3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

*Fig.9 Comparator dynamic test circuit (one channel)*

# SP93802

## SUB-NANOSECOND DUAL COMPARATOR

The Plessey SP93802 contains two independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The device also contains circuitry that enables the input hysteresis to be adjusted between 0mV and 10mV by a single external resistor.

Each comparator includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. As each comparator is separately clocked, the device can be used as a matched pair.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

### FEATURES

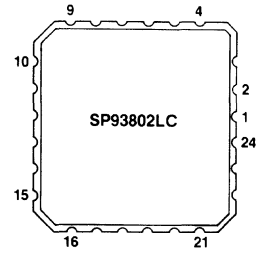
- -40°C to +85°C Temperature Range
- Typical Delay < 1ns
- Adjustable Hysteresis, 0 to 10mV
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 2 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching <100ps
- High Input Impedance

### APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers

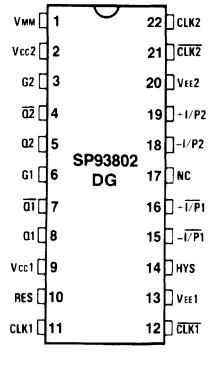
### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ - $V_{MM}$ | +6V |
| Supply voltage $V_{MM}$ - $V_{EE}$ | -6V |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |
| Output current | ≤30mA |
| Maximum input voltage | |
| Common mode positive | ≤$V_{CC}$ |
| Common mode negative | ≥$V_{EE}$ |
| Differential input voltage | ≤±3.8V |




LC24

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | $V_{MM}$ | 7 | $\overline{G1}$ | 13 | $\overline{CLK1}$ | 19 | NC |
| 2 | $V_{CC}2$ | 8 | $\overline{Q1}$ | 14 | $V_{EE}1$ | 20 | -I/P2 |
| 3 | NC | 9 | Q1 | 15 | HYS | 21 | +I/P2 |
| 4 | $\overline{G2}$ | 10 | $V_{CC}1$ | 16 | NC | 22 | $V_{EE}2$ |
| 5 | $\overline{Q2}$ | 11 | RES | 17 | -I/P1 | 23 | $\overline{CLK2}$ |
| 6 | Q2 | 12 | CLK1 | 18 | +I/P1 | 24 | CLK2 |




DG22

*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**SP93802B LC** (Industrial - Ceramic LCC package)
**SP93802B DG** (Industrial - Ceramc DIL package)

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = -40°C to +85°C, I/P and O/P $V_{CC}$ = +5V ± 0.25V,
$V_{EE}$ = -5.2V ± 0.25V, $V_{MM}$ = 0V (see Fig.4), Load = 50Ω to $V_{CC}$-2V

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 38.5 | 50 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5.2V No load |
| Negative supply current | $I_{EE}$ | | 16.0 | 21 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5.2V No load |
| Positive supply voltage | $V_{CC}$ | I/P MAX +1.55 | 5.0 | I/P MIN +7.3 | V | |
| Negative supply voltage | $V_{EE}$ | -5.5 | -5.2 | -4.9 | V | |
| Input offset voltage | $V_{OS}$ | -3.5 | | +3.5 | mV | |
| Input bias current | $I_B$ | | 5.25 | 9 | μA | |
| Input offset current | $I_{OS}$ | | 0.95 | 1.2 | μA | |
| Input capacitance | $C_I$ | 1.5 | (Note 1) | pF | | LC package |
| Input impedance | $R_I$ | | 250 | | kΩ | Measured at DC |
| Differential input range | $V_{DIF}$ | | | ±3.8 | V | |
| Common mode input range | CMIR | -2.1 | | +2.6 | V | |
| Output voltage high | $V_{OH}$ | $V_{CC}$-1.050 | | $V_{CC}$-0.81 | V | +25°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-1.140 | | $V_{CC}$-0.91 | V | -40°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-0.965 | | $V_{CC}$-0.704 | V | +85°C, $V_{IN}$ > 60mV |
| Output voltage low | $V_{OL}$ | $V_{CC}$-1.712 | | $V_{CC}$-1.544 | V | +25°C, $V_{IN}$ <- 60mV |
| | | $V_{CC}$-1.792 | | $V_{CC}$-1.650 | V | -40°C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.638 | | $V_{CC}$-1.465 | V | +85°C, $V_{IN}$ < -60mV |
| Gain (transparent mode) | | | 26 | | dB | Differential |
| Common mode rejection | CMRR | | 50 | | dB | +25°C, with respect to I/P |
| Supply voltage rejection | PSRR | | 70 | | dB | +25°C, with respect to I/P offset |
| Clock input: | | | | | | |
| Common mode range | CMRC | $V_{MM}$+2V | | $V_{CC}$-1.35V | V | |
| Differential swing | DS | 400 | | 1600 | mV | |

NOTES 1. Guaranteed but not tested.

**Dynamic Characteristics (Note 1)** See dynamic test circuit Fig.9.

| Characteristic | Symbol | Value | | | Units | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Latch setup time | $t_S$ | | 150 | | ps | 10mV overdrive |
| Hold time | $t_H$ | | 600 | | ps | 10mV overdrive |
| Input to Q delay | $t_{PD}$ | | 950 | | ps | 10mV overdrive |
| Latch to Q delay | $t_{LQ}$ | | 1850 | | ps | 10mV overdrive |
| Glitch capture regeneration | $t_{RD}$ | | 900 | | ps | 20mV overdrive at Qn |
| Propagation delay matching | $t_{PDM}$ | -100 | | +100 | ps | Within each device |
| Min. compare pulse width | $t_{PW}$ | | 950 | | ps | 10mV overdrive |
| Min. reset pulse width | $t_{RM}$ | | 800 | | ps | |
| Max. flip flop reset time | $t_{RR}$ | | 800 | | ps | |
| Min. hold time of Qn after reset | $t_{GH}$ | | 800 | | ps | |
| Delay between Gn and Qn | $t_{DQ}$ | | 900 | | ps | |
| Propagation delay Gn to reset | $t_{GR}$ | | 800 | | ps | |

NOTES 1 Guaranteed but not tested.

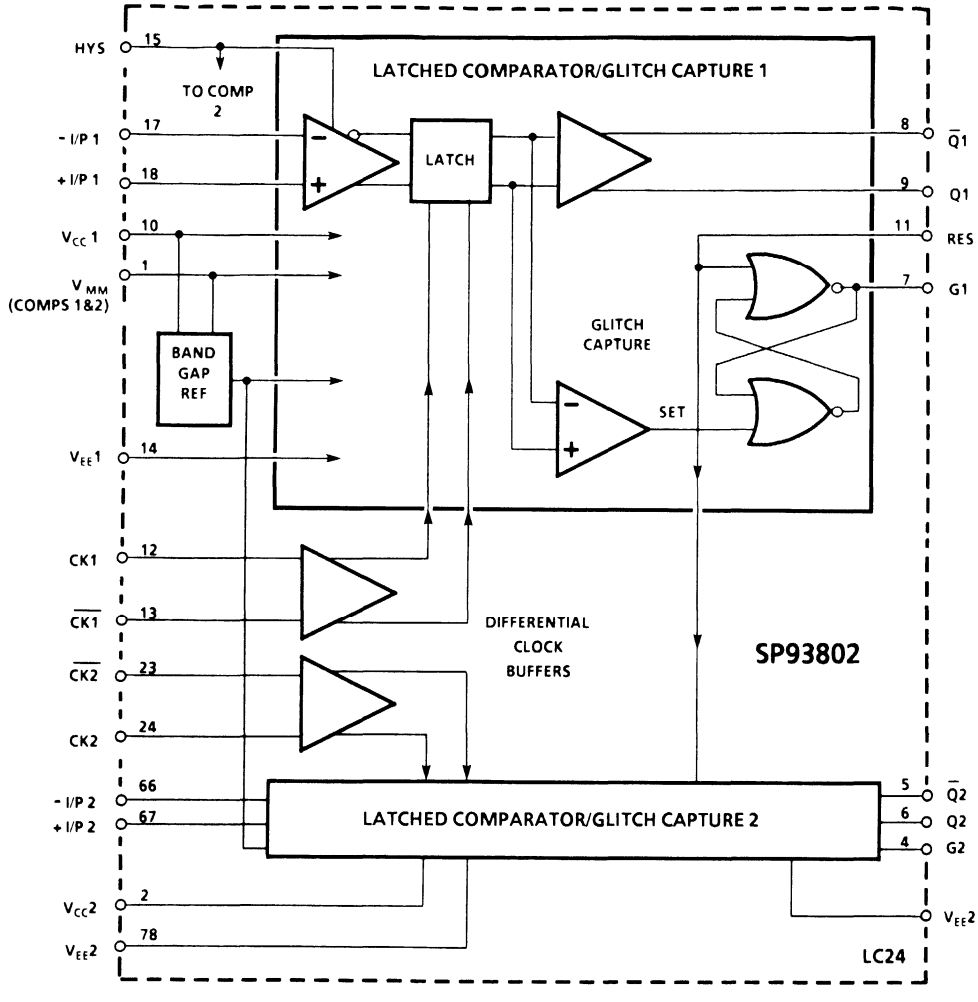



*Fig.2 Internal block diagram, with pins shown for LC24 package (comparator 2 as detailed for comparator 1)*

## PIN FUNCTIONS

| Name | Pin | Description |
|---|---|---|
| $V_{CC}1$ | 10 | Positive supply connection for comparator 1 and the bandgap reference. |
| $V_{CC}2$ | 2 | Positive supply connection for comparator 2. |
| -I/Pn | 17/18, 20/21 | Inverting and non-inverting inputs to comparators 1 and 2, respectively. |
| +I/Pn | | |
| Qn/$\overline{Qn}$ | 9/8, 6/5 | Q and $\overline{Q}$ outputs of comparators 1 and 2, respectively. |
| Gn | 7,4 | Outputs of glitch capture circuits 1 and 2, respectively. |
| RES | 11 | Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'. |
| CLK1, $\overline{CLK1}$ | 12,13 | Clock input pins for comparator 1. ECL active low signal which latches the outputs of comparator 1. |
| CLK2, $\overline{CLK2}$ | 24,23 | Clock input pins for comparator 2. ECL active low signal which latches the outputs of comparator 2. |
| $V_{EE}1$ | 14 | Negative supply voltage for comparator 1. |
| $V_{EE}2$ | 22 | Negative supply voltage for comparator 2. |
| HYS | 15 | Hysteresis control pin. A pull-up resistor ($R_H$) is required to set the input hysteresis window for all comparators. |
| $V_{MM}$ | 1 | Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref. |

## OPERATING NOTES

### Transparent Mode

The SP93802 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 26dB. In this mode, for example, a 10mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93802 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

### Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

### Supply Connections

The SP93802 operates from supply voltages of 0V, -5.2V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from $V_{CC}$, then to interface with other ECL circuits directly, supplies of 0V, -5.2V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage ($V_{MM}$), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5.2V supply is not available.

The SP93802 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5.2V rails.

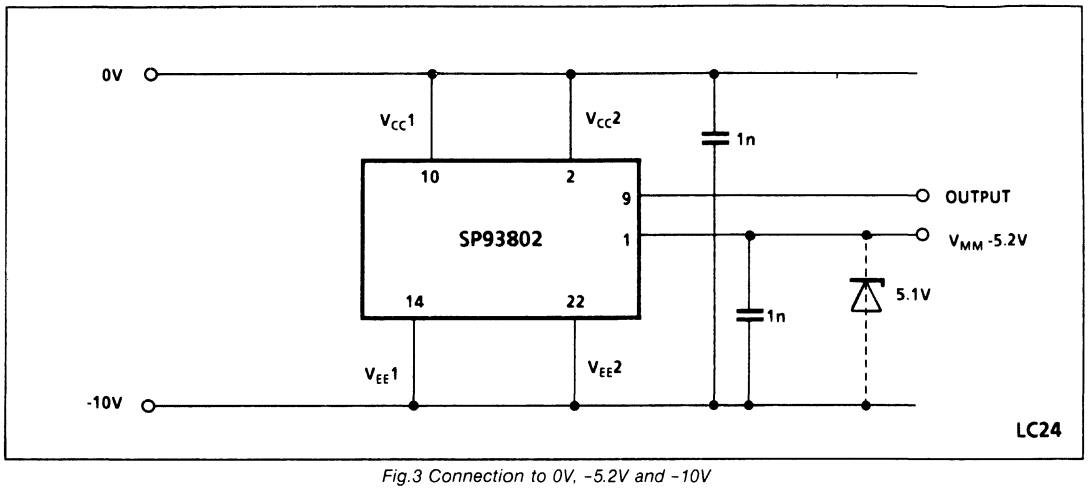



*Fig.3 Connection to 0V, -5.2V and -10V*

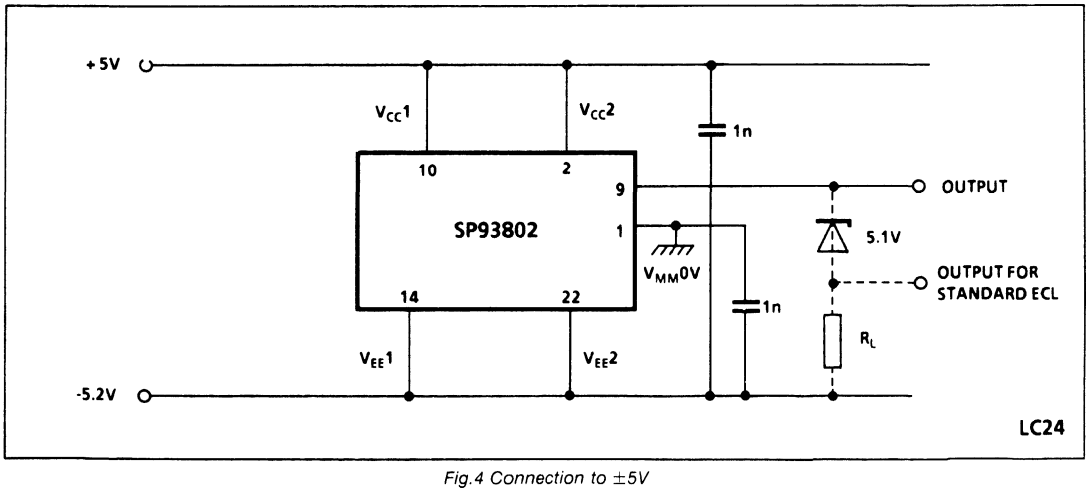



*Fig.4 Connection to ±5V*

### External Components

The Qn, Qn and Gn outputs are open emitters and therefore required external pulldown resistors ($R_L$). These resistors may be in the range of 50-250Ω connected to $V_{CC}$-2V ($V_T$) or 250-2000Ω connected to $V_{MM}$.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and $V_{EE}$ is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

### Hysteresis Control

The SP93802 incorporates adjustable hysteresis. The input window is simply controlled by the current flowing into the HYS input (pin 15). The following expression can be used to determine the value of this resistor for a defined amount of symmetrical hysteresis at the input ($V_{HYS}$). See Fig.6.

$$R_H = \frac{|V_{CC} - V_{EE}| - 0.8 - 75V_{HYS}}{0.32V_{HYS}} \Omega$$

where: $V_{CC}$ = +Supply voltage (V)
$V_{EE}$ = -Supply voltage (V)
$V_{HYS}$ = Required peak-to-peak hysteresis window at the input (V)

Note that for zero hysteresis the HYS pin should be connected to $V_{EE}1$; $R_H$ minimum is 200Ω.

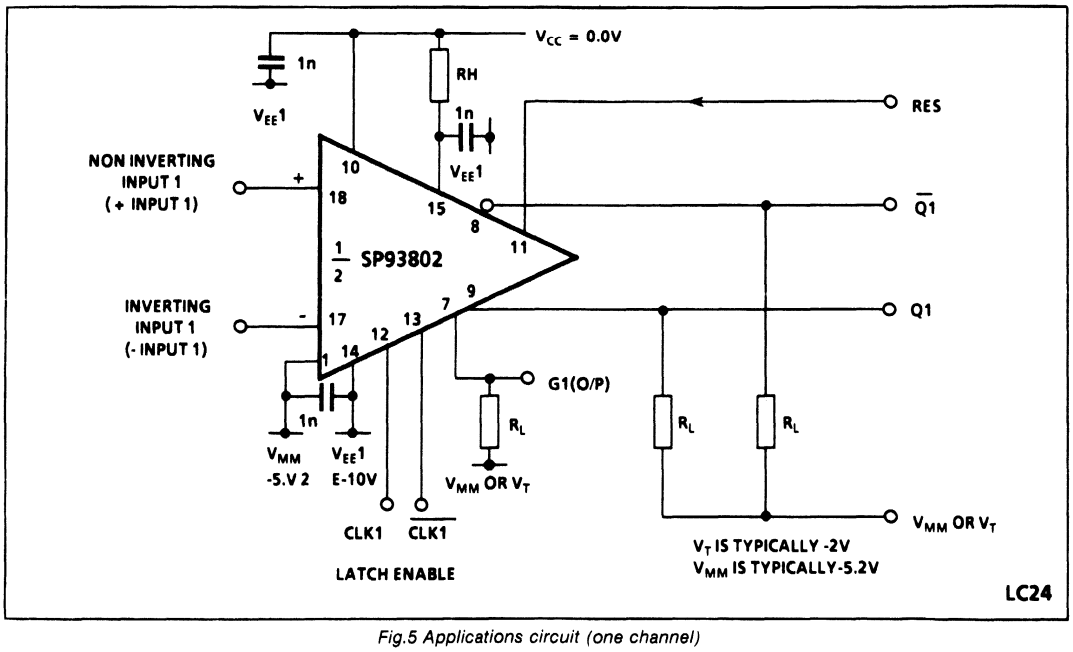



*Fig.5 Applications circuit (one channel)*

### Clock Inputs

The SP93802 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as two single comparators as both comparators can be clocked separately from comparators 3 and 4.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device Vcc connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

CLK1 (pin 12) comparator 1 latched when low.
$\overline{CLK1}$ (pin 13) inverse clock for comparator 1.
CLK2 (pin 24) comparator 2 latched when low.
$\overline{CLK2}$ (pin 23) inverse clock for comparator 2.

The clock inputs should have fast rise times and low jitter. The Plessey SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator.

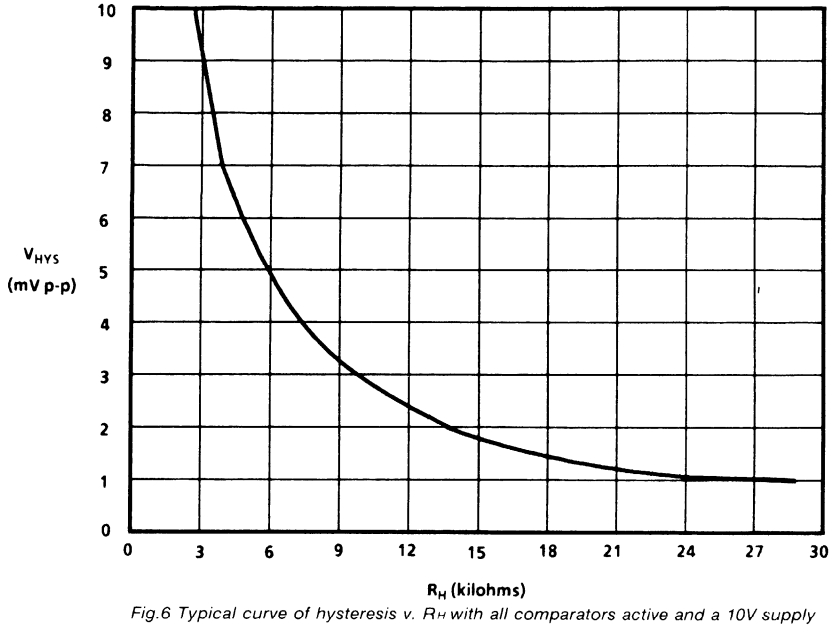



*Fig.6 Typical curve of hysteresis v. $R_H$ with all comparators active and a 10V supply*

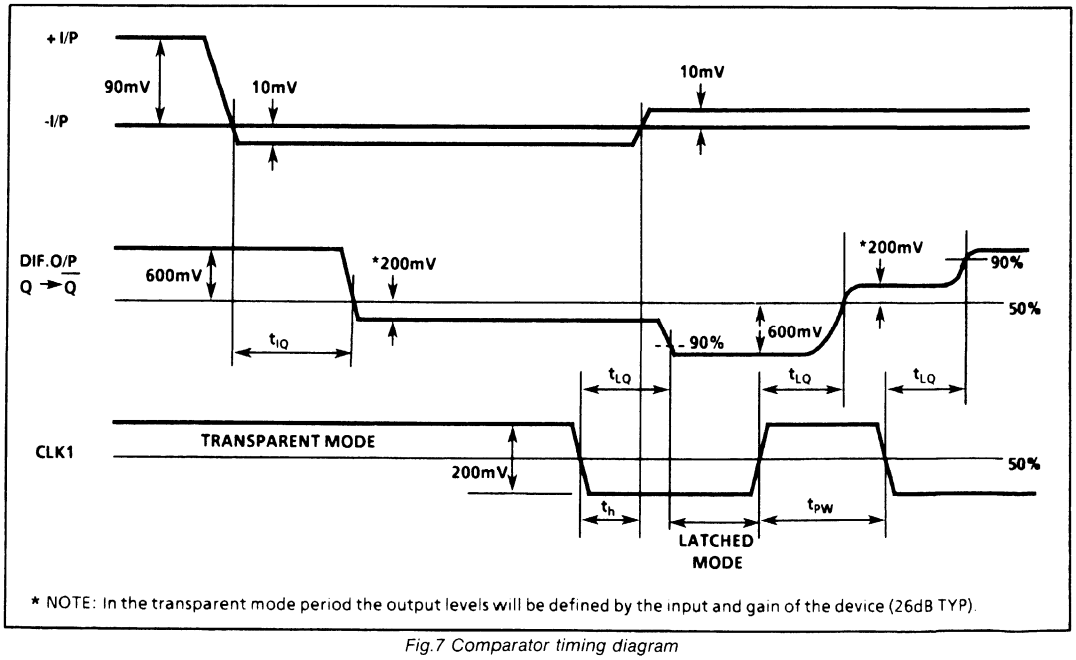



*Fig.7 Comparator timing diagram*

| I/P | CLK | Qn + 1 |
|---|---|---|
| X | 0 | Qn |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

X = Don't Care

*Table 1 Truth table for comparator*

### Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' ($V_{CC}$-0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn outpt will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

| RES | SET(1) (n + 1) | Gn + 1 |
|---|---|---|
| 1 | X | 0 |
| 0 | ↗ | ↗ |
| 0 | ↘ | 1 |
| 0 | 1 | 1 |
| 0 | 0 | Gn(2) |
| ↘ | 1 | ↗ |
| ↘ | 0 | 0 |

X = Don't Care

*Table 2 Truth table for glitch capture circuit*

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.9.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

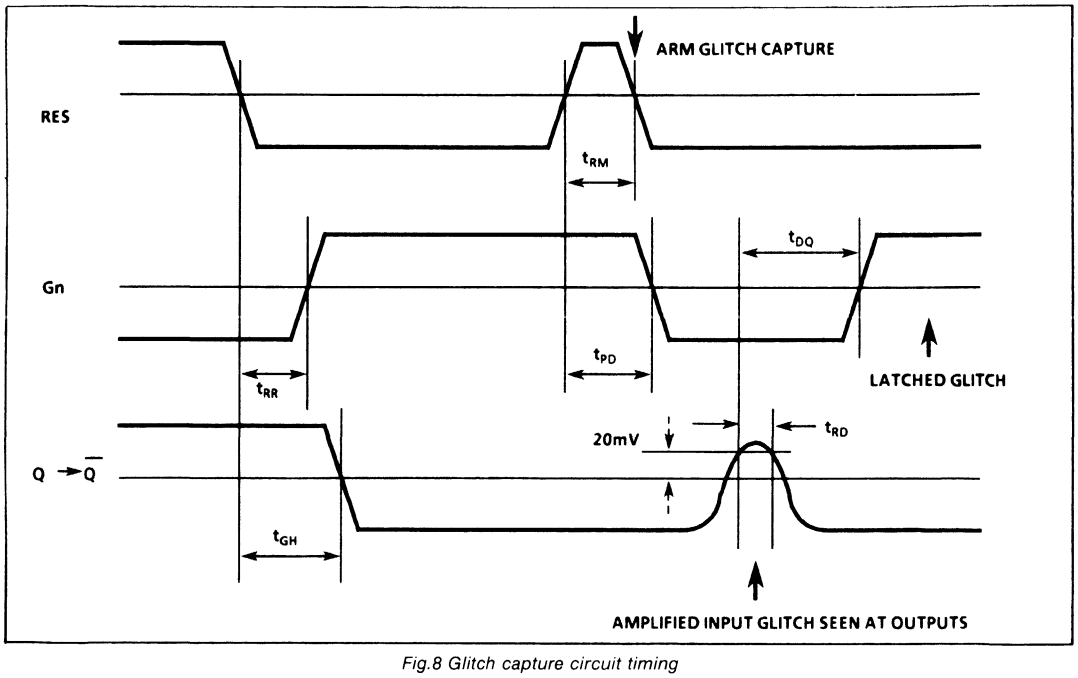
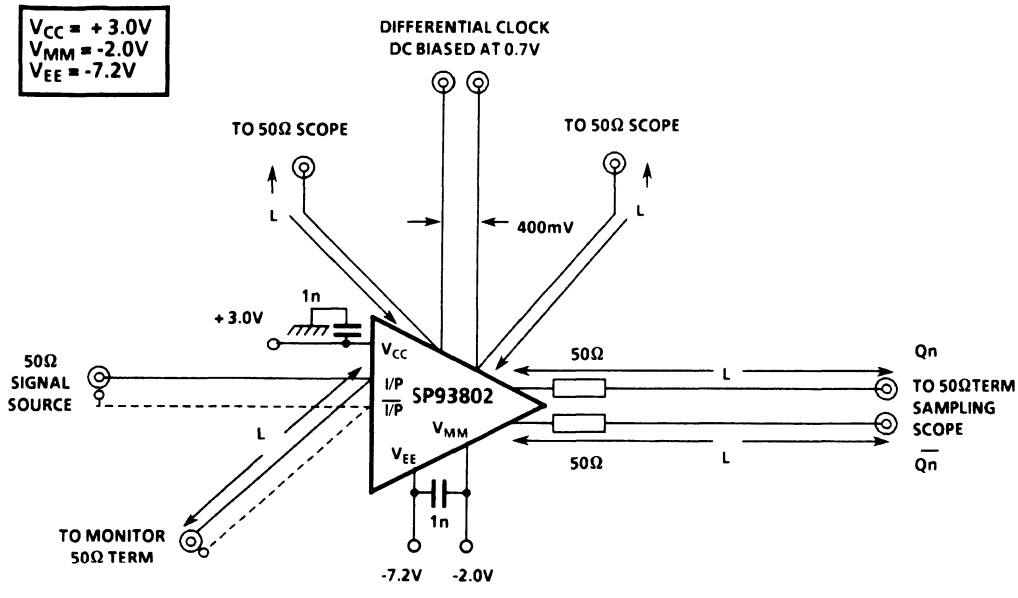



*Fig.8 Glitch capture circuit timing*




NOTES:-
The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) A Plessey SP92701 can be used with supplies of +3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

*Fig.9 Comparator dynamic test circuit (one channel)*

PLESSEY
Semiconductors

# SP9687

## ULTRA FAST COMPARATOR

The SP96857 is an ultra-fast dual comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be operate in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is high, and $\overline{LE}$ is low, the comparator function is in operation. When LE is driven low and $\overline{LE}$ high, the outputs are locked into the logical states at the time of arrival of the latch signal. If the latch function is not used, LE must be connected to ground.

The device is pin compatible with the AM687 and operates from conventional +5V and -5.2V rails.

### FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- 50 ohm Line Driving Capability
- Excellent Common Mode Rejection
- Supply Voltages +5V, -5.2V
- Operating Temperature Range:
  SP9687 — -30°C to +85°C
  SP9687AC — -55°C to +125°C
- Pin Compatible with AD9687
- Pin Compatible with AM687 — But Faster
- Comparators within each SP9687 are matched as follows:
  Input to Output Delay Matching 200ps (typ)
  Latch to Output Delay Matching 200ps (typ)

### ORDERING INFORMATION

**SP9687DG** (Industrial - Ceramic DIL package)
**SP9687BB DG** (Plessey High Reliability Ceramic DIL package)
**SP9687LC** (Industrial - LCC package)
**SP9687MP** (Industrial - Miniature Plastic package)
**SP9687AC DG** (Military - Ceramic DIL package)

NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

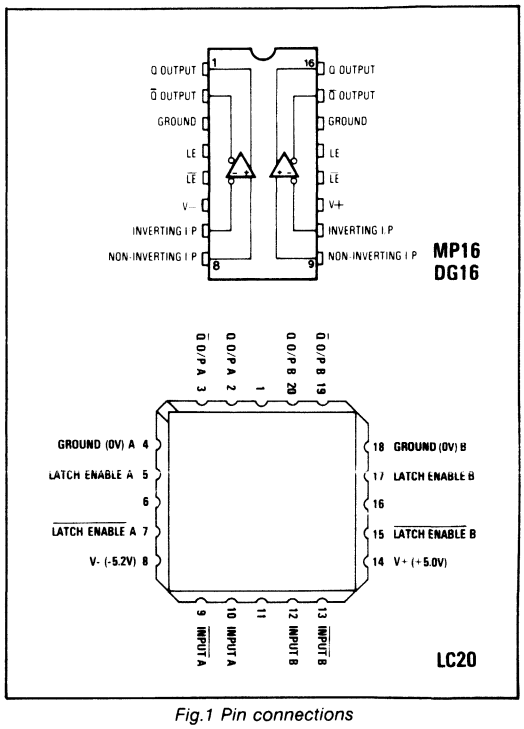
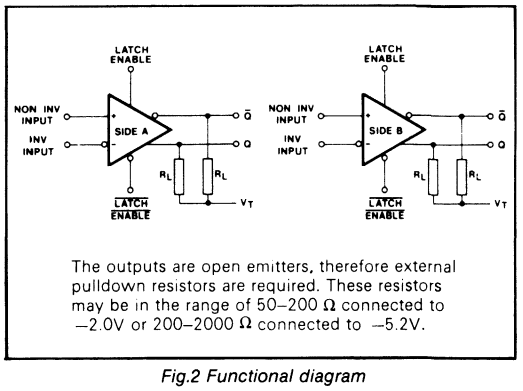



*Fig.1 Pin connections*




The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to –2.0V or 200–2000 Ω connected to –5.2V.

*Fig.2 Functional diagram*

## OPERATING NOTES

### Timing diagram

The timing diagram, Fig. 3, shows in graphic form a sequence of events in the SP9687. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time $t_{pd}$. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time $t_s$ before the latch falling edge, and must be maintained for a time $t_h$ after the latch falling edge, in order to be acquired. After $t_h$, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strob operation, and the output transitions occur after a time $t_{pd(E)}$. The LE input is omitted for clarity.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Postive supply voltage | 6V |
| Negative supply voltage | -6V |
| Output current | 30mA |
| Input voltage | ±3V |
| Differential input voltage | 3.5V |
| Differential latch voltage | 3.5V |
| Power dissipation | 590mW |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |
| Lead temperature (soldering 60 sec) | 300°C |

Thermal characteristics

| | |
|---|---|
| DG16 | $\theta_{JA}$ = 110°C/W |
| | $\theta_{JC}$ = 33°C/W |
| LC20 | $\theta_{JA}$ = 73°C/W |
| | $\theta_{JC}$ = 22°C/W |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = -30°C to +85°C: $V_{CC}$ = 5.0V ± 0.25V: $V_{EE}$ = -5.2V ± 0.25V:
$R_L$ = 50Ω: $V_T$ = -2.0V (see Fig.2)

| Characteristic | Value | | Units | Conditions |
|---|---|---|---|---|
| | Min. | Max. | | |
| Input offset voltage | -5 | +5 | mV | $R_S$ < 100Ω 25°C |
| | -7 | +7 | mV | $R_S$ < 100Ω |
| Input bias current | | 20 | μA | 25°C |
| | | 30 | μA | |
| Input offset current | | 5 | μA | 25°C |
| | | 8 | μA | |
| Input resistance | 60 | | kΩ | 25°C |
| Input capacitance | | 3 | pF | 25°C |
| Supply current $I_{EE}$ | | 68 | mA | Note 2 25°C |
| | | 75 | mA | |
| Supply current $I_{CC}$ | | 46 | mA | Note 2 25°C |
| | | 50 | mA | |
| Common mode range | -2.5 | +2.5 | V | |
| Output logic levels | | | | |
| Output high | -0.96 | -0.81 | V | 25°C |
| | -1.045 | -0.875 | V | $T_{amb}$ = Min. |
| | -0.89 | -0.70 | V | $T_{amb}$ = Max. |
| Output low | -1.85 | -1.65 | V | 25°C |
| | -1.89 | -1.65 | V | $T_{amb}$ = Min. |
| | -1.83 | -1.575 | V | $T_{amb}$ = Max. |
| Min. latch set up time | | 1 | ns | Notes 1, 3, 4 25°C |
| | | 2 | ns | |
| Input to output delay | | 3 | ns | Notes 1, 3 (Q and Q) 25°C |
| | | 4 | ns | |
| Latch to output delay | | 3 | ns | Notes 1, 3, 4 (Q and Q) 25°C |
| | | 4.5 | ns | |
| Minimum latch pulse width | | 3 | ns | Note 1 25°C |
| Minimum hold time | | 1 | ns | Note 1 25°C |

NOTES

1. Guaranteed but not tested.
2. Refers to entire package. Other data in this table applies to each half.
3. +100mV pulse with -10mV overdrive. See Figs.6 to 8.
4. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.

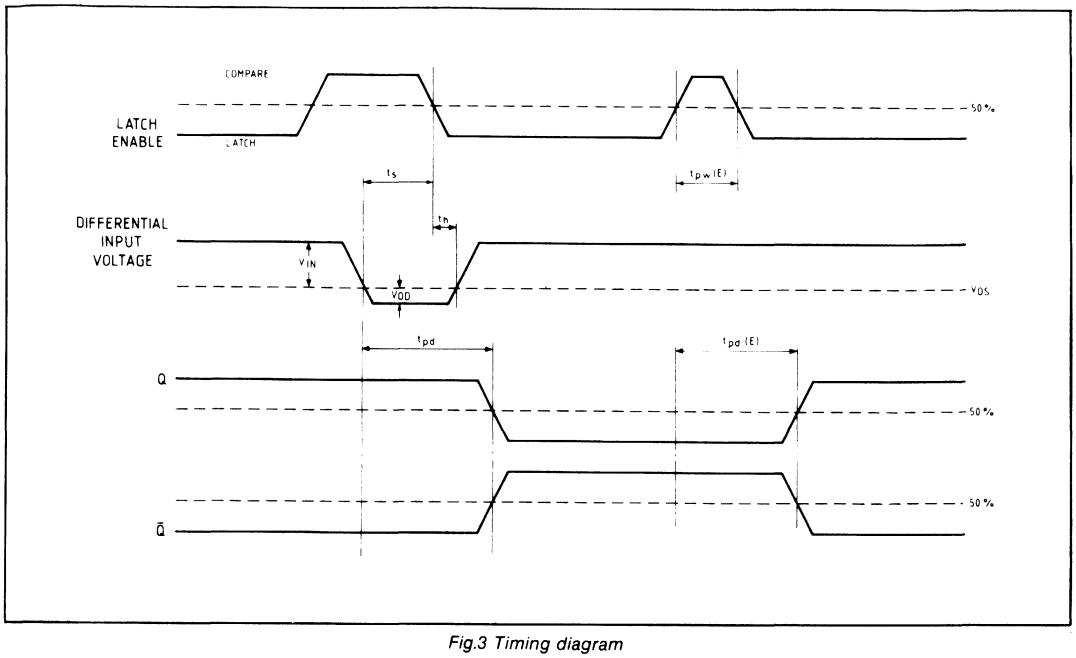



*Fig.3 Timing diagram*

## PERFORMANCE CURVES

Unless otherwise specified, standard conditions for all curves are $T_{amb}$ = 25°C, $V_{CC}$ = 5.0V, $V_{EE}$ = -5.2V

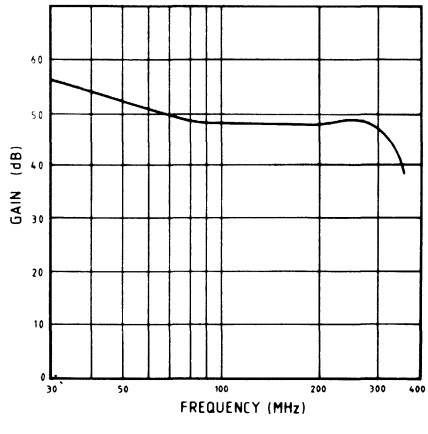



*Fig.4 Open loop gain as a function of frequency*

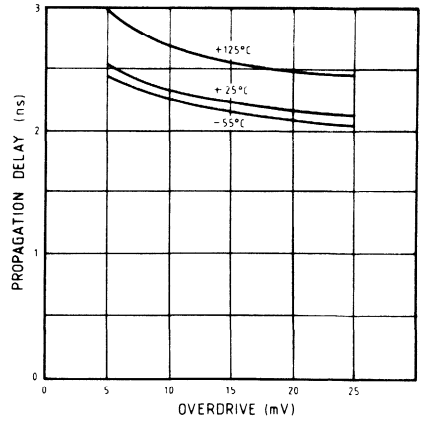



*Fig.5 Propagation delay, latch to output as a function of overdrive*

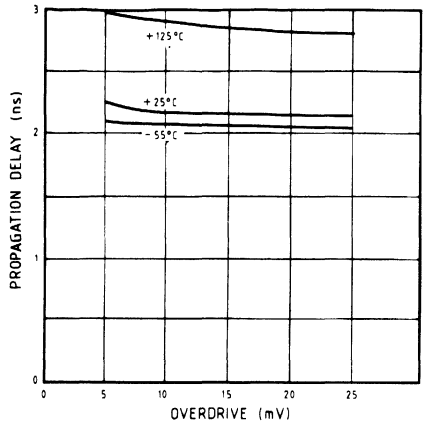



*Fig.6 Propagation delay, input to output as a function of overdrive*

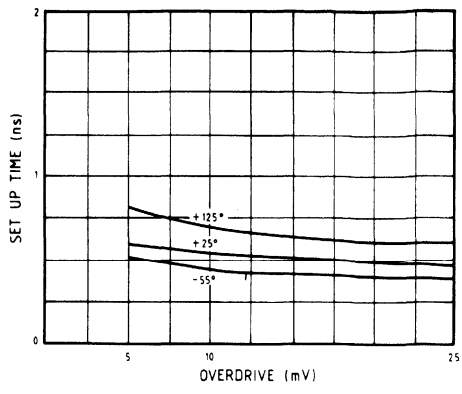



*Fig.7 Set-up time as a function of temperature*

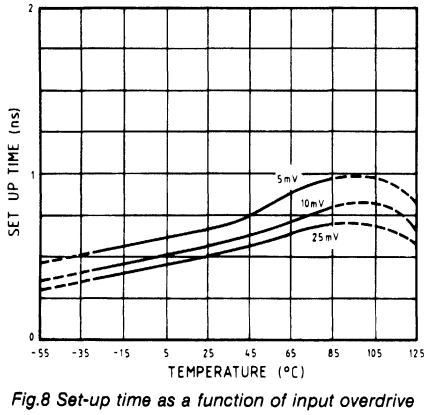



*Fig.8 Set-up time as a function of input overdrive*

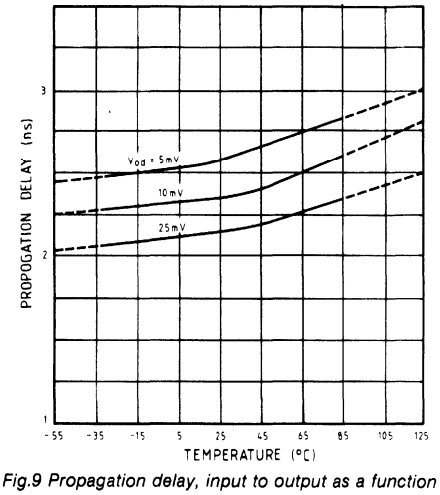



*Fig.9 Propagation delay, input to output as a function of temperature*

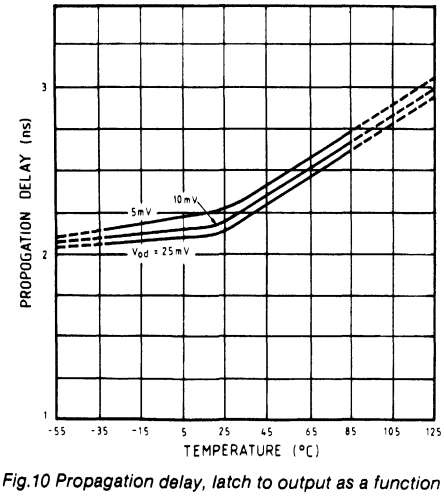



*Fig.10 Propagation delay, latch to output as a function of temperature*

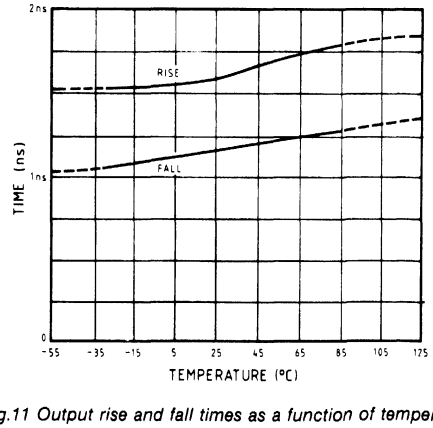



*Fig.11 Output rise and fall times as a function of temperature*

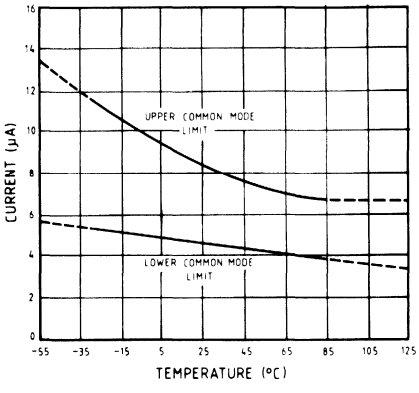



*Fig.12 Input bias currents as a function of temperature*

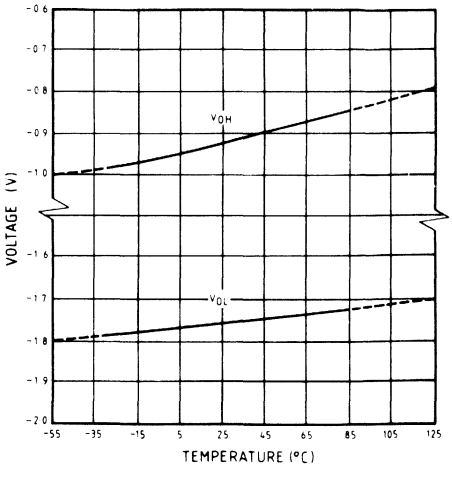



*Fig.13 Output levels as a function of temperature*

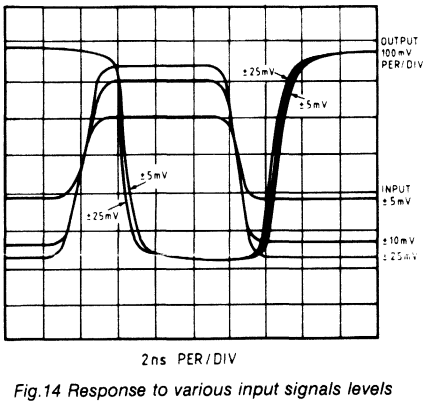



*Fig.14 Response to various input signals levels*

# SP9685

## ULTRA FAST COMPARATOR

The SP9685 is an ultra-fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and -5.2V rails. It is pin and voltage compatible with AD9685.

### FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- Supply +5V, -5.2V (±0.25V)
- 50 ohm Line Driving Capability
- Excellent Common Mode Rejection
- Operating Temperature Range :
  SP9685 — -30°C to +85°C
  SP9685AC — -55°C to +125°C
- Pin Compatible with AD9685
- Pin Compatible with AM685 — But Faster

### APPLICATIONS

- Ultra High Speed A/D Converter
- Ultra High Speed Line Receivers
- Peak Detectors
- Threshold Detectors

### ORDERING INFORMATION

**SP9685CM** (Industrial - Cylindrical Metal package)
**SP9685DG** (Industrial - Ceramic DIL package)
**SP9685LC** (Industrial - LCC package)
**SP9685BB DG** (Plessey High Reliability Ceramic DIL package)
**SP9685MP** (Industrial - Miniature Plastic package)
**SP9685AC DG** (Military - Ceramic DIL package)

NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

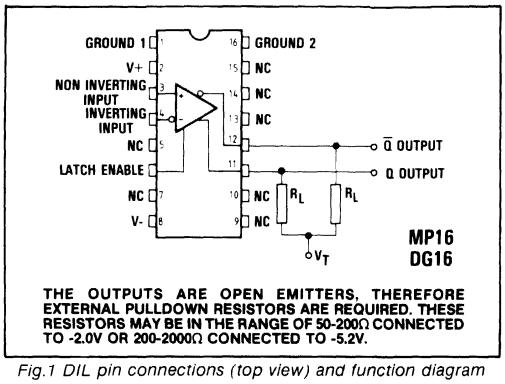



*Fig.1 DIL pin connections (top view) and function diagram*

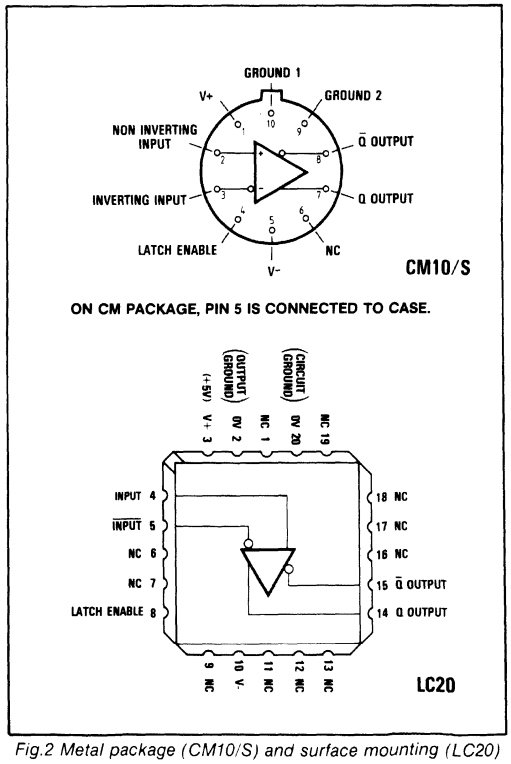



*Fig.2 Metal package (CM10/S) and surface mounting (LC20) package pin connections (top view)*

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| Postive supply voltage | 6V | Storage temperature range | -55°C to +150°C |
| Negative supply voltage | -6V | Operating junction temperature | <175°C |
| Output current | 30mA | Lead temperature (soldering 60 sec) | 300°C |
| Input voltage | ±3V | Vibration | 196m/s² |
| Differential input voltage | 3.5V | Shock | 14700m/s² peak 0.5ms duration |
| Power dissipation | 350mW | | |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$V_{CC}$ = 5.00V: $V_{EE}$ = -5.2V: $R_L$ = 50Ω: $V_T$ = 2.0V (see Fig.1)

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Input offset voltage | -5 | | +5 | mV | $R_S$ < 100Ω 25°C |
| | -7 | | +7 | mV | $R_S$ < 100Ω |
| Input bias current | | | 20 | μA | 25°C |
| | | | 30 | μA | |
| Input offset current | | | 5 | μA | 25°C |
| | | | 8 | μA | |
| Supply current $I_{EE}$ | | | 34 | mA | 25°C |
| | | | 36 | mA | |
| Supply current $I_{CC}$ | | | 23 | mA | 25°C |
| | | | 24 | mA | 25°C |
| Total power dissipation | 210 | | 350 | mW | Note 325°C |
| Common mode range | -2.5 | | +2.5 | V | |
| Output logic levels | | | | | |
| Output high | -0.96 | | -0.81 | V | 25°C |
| | -1.045 | | -0.875 | V | $T_{amb}$ = Min. |
| | -0.89 | | -0.70 | V | $T_{amb}$ = Max. |
| Output low | -1.85 | | -1.65 | V | 25°C |
| | -1.89 | | -1.65 | V | $T_{amb}$ = Min. |
| | -1.83 | | -1.575 | V | $T_{amb}$ = Max. |
| Min. latch set up time | | | 1 | ns | Notes 1, 2, 3 25°C |
| | | | 2 | ns | |
| Input to output delay | | | 3 | ns | Note 1, 3 (Q and Q) 25°C |
| | | | 4 | ns | |
| Latch to output delay | | | 3 | ns | Notes 1, 2, 3 (Q and Q) 25°C |
| | | | 4.5 | ns | |
| Minimum latch pulse width | | | 3 | ns | Note 3 25°C |
| Minimum hold time | | | 1 | ns | Note 3 25°C |
| Max. input capacitance | | 3 | | pF | Note 3 25°C |
| Input resistance | 60 | | kΩ | | Note 3 25°C |
| Common mode rejection ratio | 70 | | | dB | Note 3 25°C |
| Supply voltage rejection ratio | 50 | | | dB | Note 3 25°C |

NOTES

1. +100mV pulse with -10mV overdrive.
2. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.
3. Guaranteed but not tested.

Thermal characteristics

| | | |
|---|---|---|
| CM10 | $\theta_{JA}$ = 220°C/W | |
| | $\theta_{JC}$ = 65°C/W | |
| DG16 | $\theta_{JA}$ = 120°C/W | |
| | $\theta_{JC}$ = 40°C/W | |
| LC20 | $\theta_{JA}$ = 73°C/W | |
| | $\theta_{JC}$ = 22°C/W | |

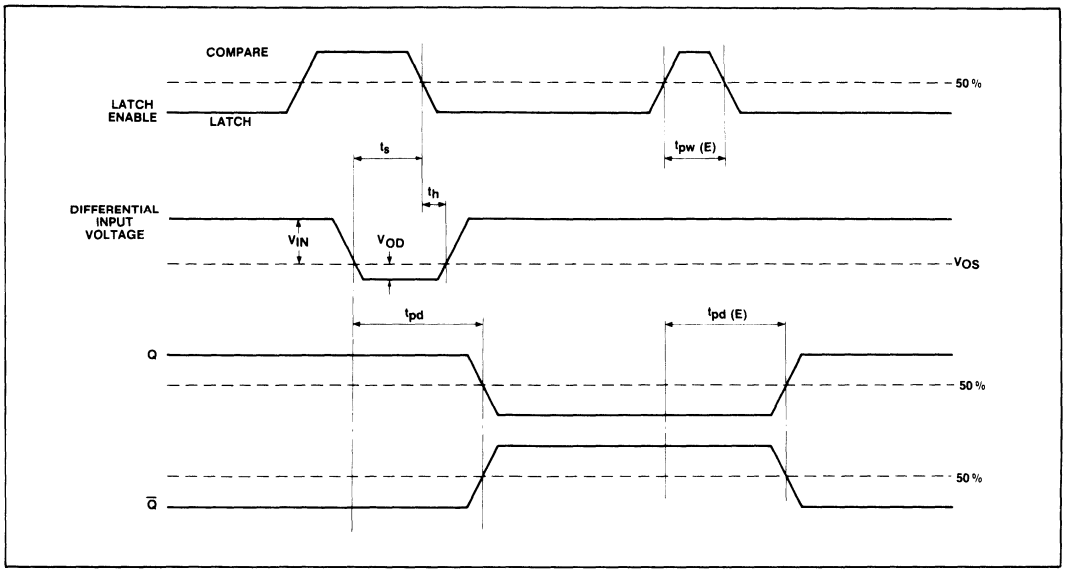



*Fig.3 Timing diagram*

## OPERATING NOTES

### Timing diagram

The timing diagram, Fig. 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time $t_{pd}$. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time $t_s$ before the latch falling edge, and must be maintained for a time $t_h$ after the latch falling edge, in order to be acquired. After $t_h$, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

### Measurement of propagation and latch delays

A simple test circuit is shown in Fig.4. The operating sequence is:

1. Power up and apply input and latch signals. Input = 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

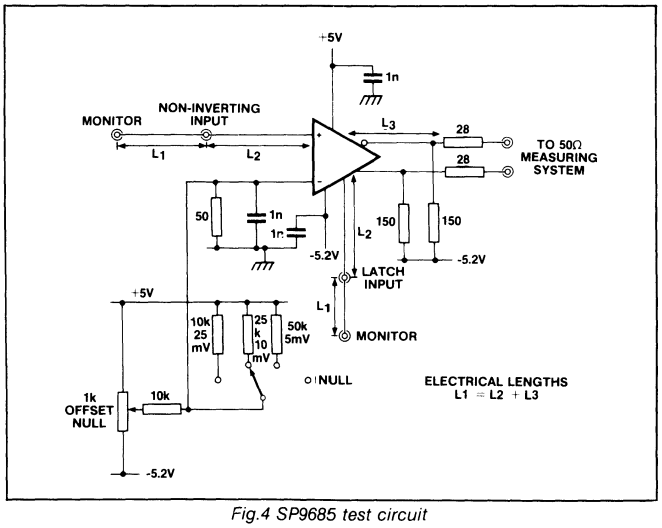



*Fig.4 SP9685 test circuit*

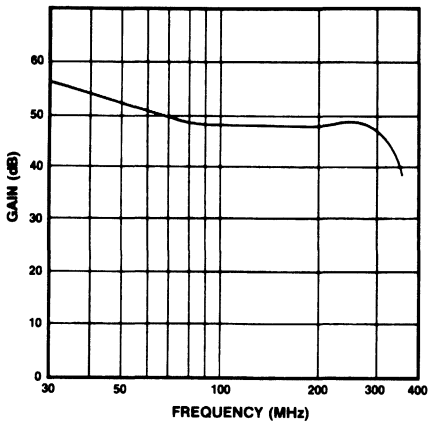



*Fig.5 Open loop gain as a function of frequency*

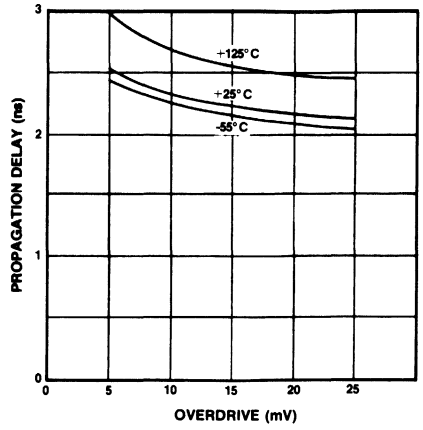



*Fig.6 Propagation delay, latch to output as a function of overdrive*

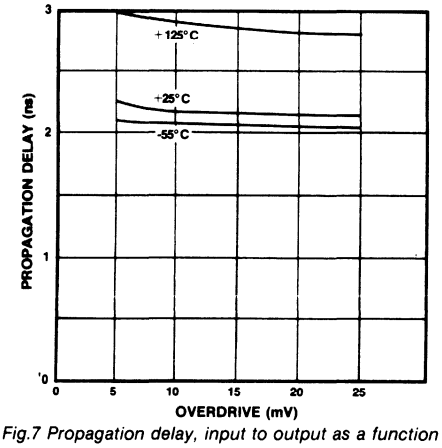



*Fig.7 Propagation delay, input to output as a function of overdrive*

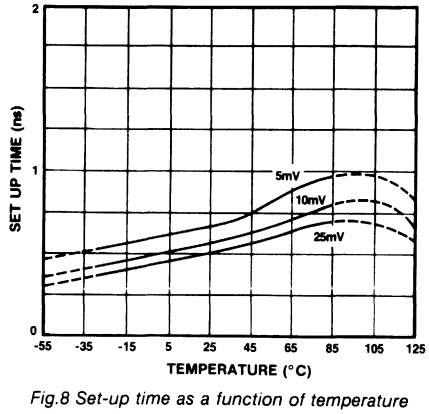



*Fig.8 Set-up time as a function of temperature*

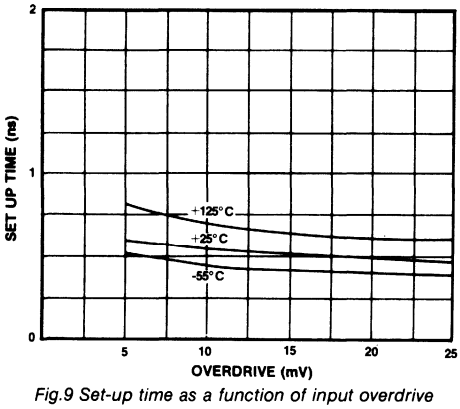



*Fig.9 Set-up time as a function of input overdrive*

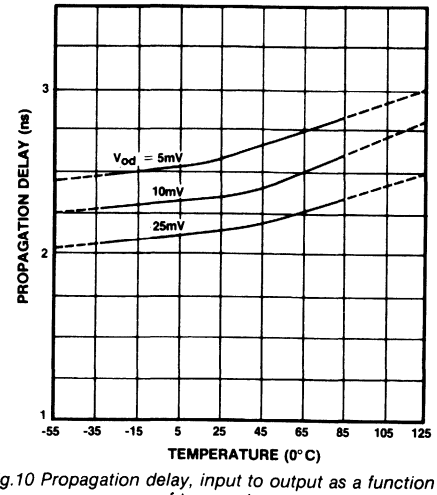



*Fig.10 Propagation delay, input to output as a function of temperature*

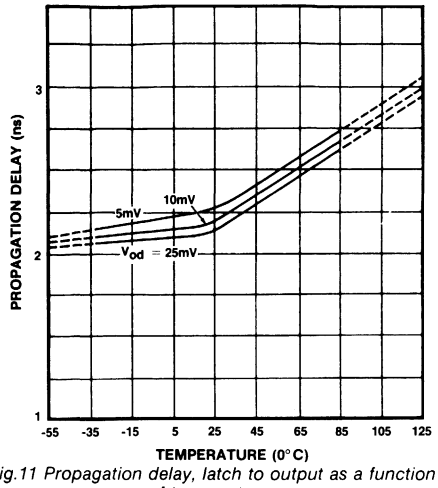



*Fig.11 Propagation delay, latch to output as a function of temperature*

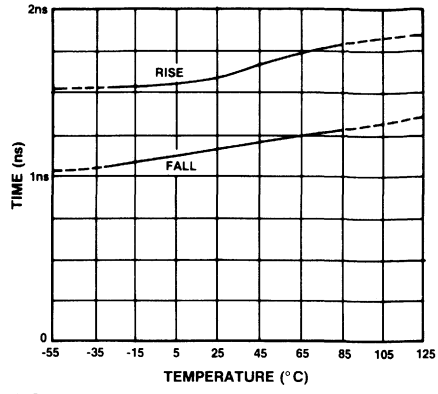



*Fig.12 Output rise and fall times as a function of temperature*

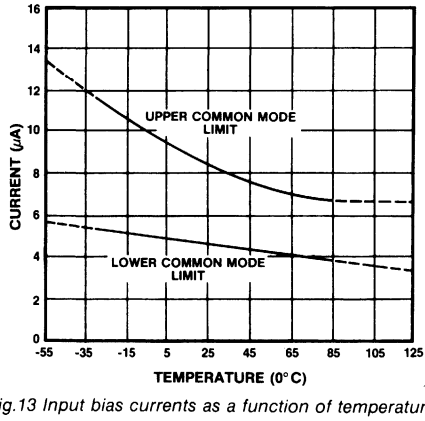



*Fig.13 Input bias currents as a function of temperature*

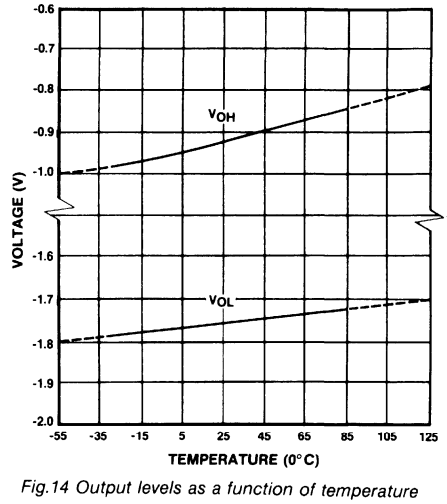



*Fig.14 Output levels as a function of temperature*

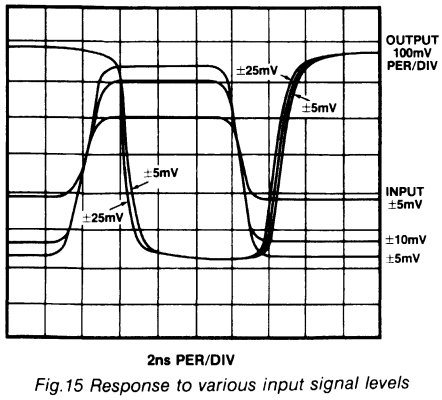



*Fig.15 Response to various input signal levels*

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# SP9680

## ULTRA FAST COMPARATOR

The SP9680 is an ultra fast comparator manufactured using a high performance bipolar process which makes possible very short propagation delays (2.4ns typ.).

The circuit has differential inputs and complementary ECL outputs, capable of driving 50 Ω lines.

The device is manufactured in a low cost mini-dip package and is intended as an alternative to the faster SP9685 in applications where performance premium and the latch facility are not required.

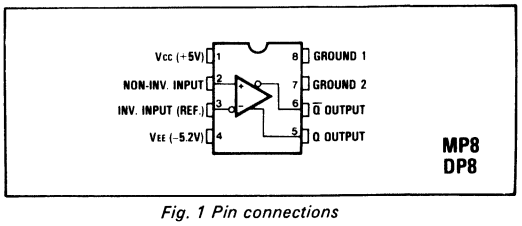
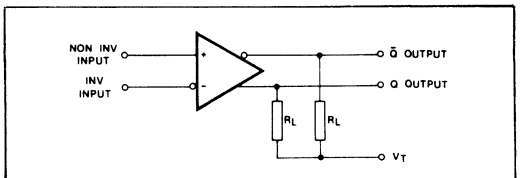



*Fig. 1 Pin connections*

### FEATURES

- Propagation Delay 2.4ns Typ.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- 8-Lead Plastic Package
- Supply Voltages +5, −5.2V
- Operating Temperature Range −30°C to +70°C




The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to −2.0V or 200–2000 Ω connected to −5.2V.

*Fig. 2 Functional diagram*

### ORDERING INFORMATION

**SP9680DP** (Industrial - Plastic DIL package)
**SP9680MP** (Industrial - Miniature Plastic package)

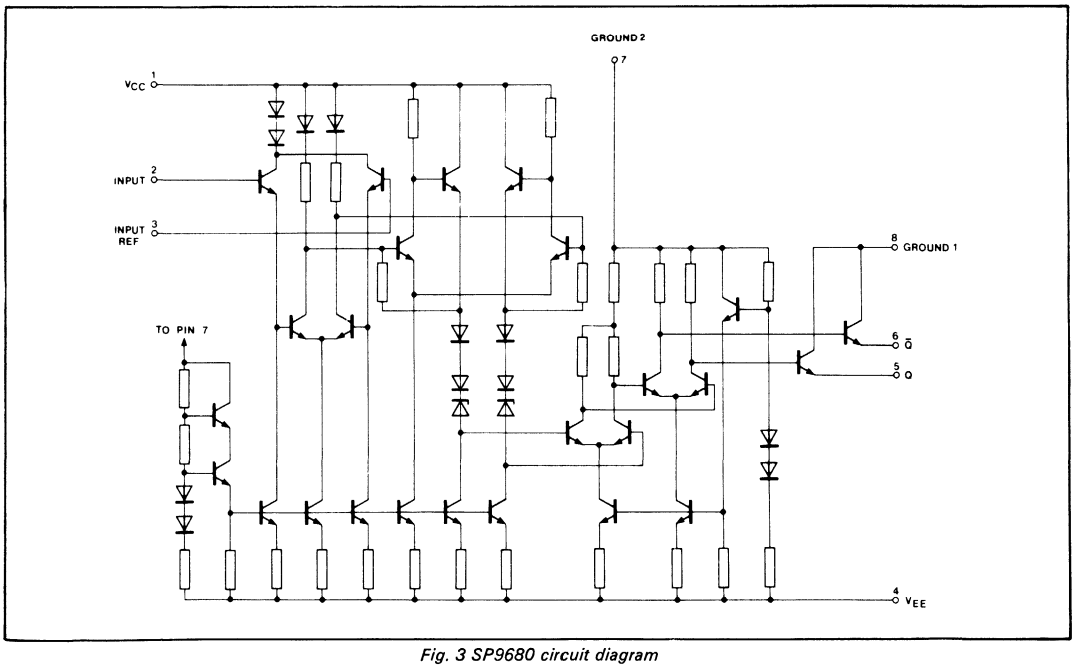



*Fig. 3 SP9680 circuit diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb} = 25°C$
$V_{CC} = 5.00V \pm 0.25V$
$V_{EE} = -5.2V \pm 0.25V$
$R_L = 50\,\Omega$
$V_T = -2.0V$ (See Fig. 2)

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Input offset voltage | −6 | | +6 | mV | Rs <100 Ω |
| Input bias current | | 20 | 40 | μA | |
| Input offset current | | | 10 | μA | |
| Supply current Icc | | 18 | 25 | mA | |
| $I_{EE}$ | | 22 | 35 | mA | |
| Total power dissipation | | 200 | 300 | mW | |
| Input to Q output delay | | 2.4 | 4 | ns | } 100mV pulse,10mV overdrive |
| Input to $\overline{Q}$ output delay | | 2.4 | 4 | ns | |
| Common mode range | −2 | | +2 | V | |
| Common mode rejection ratio | | 80 | | dB | |
| Output logic levels | | | | | |
| Output HIGH | −0.96 | | −0.81 | V | |
| Output LOW | −1.85 | | −1.65 | V | |
| Input capacitance | | 3.5 | | pF | |
| Input resistance | 50 | | | kΩ | |
| Operating temperature range | −30 | | +70 | °C | |

Thermal characteristics $\theta_{JA} = 111°C/W$
$\theta_{JC} = 71°C/W$

## ABSOLUTE MAXIMUM RATINGS

Positive supply voltage $V_{CC}$ +6V
Negative supply voltage $V_{EE}$ −6V
Output current 30mA
Input voltage ±3V
Differential input voltage 3.5V
Storage temperature range -55°C to +150°C
Operating junction temperature <150°C

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PRELIMINARY INFORMATION

# SP92701

## SUB-NANOSECOND ECL LINE RECEIVER AND DRIVER

The SP92701 is designed with an on-chip reference to allow either single ended or differential ECL signals to be received. The inverted and non-inverted outputs can drive 50Ω lines directly.

The use of a fixed current source in the tail of the differential input stage, enables the device to be used in more general applications. These include operational amplifier applications where low propagation delays are required.

### FEATURES

- ECL 10K Compatible
- Single or Differential Operation
- 50 Ohm Line Driving Capability
- Sub-nanosecond Performance
- ECL Reference Output
- Operating Temperature -40°C to +85°C (DG)
- Full Static Protection on All Pins

### APPLICATIONS

- Line Receiver
- Line Driver
- Clock Buffering/Distribution
- Op-amp Circuits
- Fanout Expansion
- Schmitt Trigger Circuits
- Fast Peak Detector

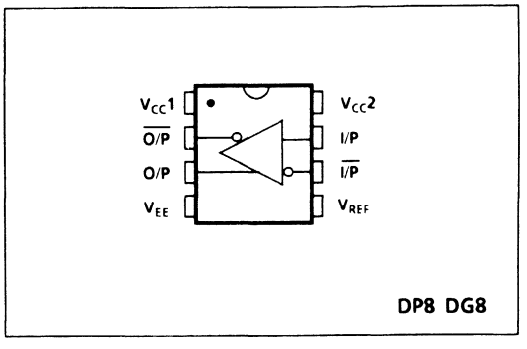



*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**SP92701C DP** (Industrial - Plastic DIL package)
**SP92701B DG** (Industrial - Ceramic DIL package)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $\lvert V_{CC}-V_{EE}\rvert$ | 8V |
| Input voltage | 0V to $V_{EE}$ |
| Differential input voltage | 3.3V |
| Output source current | 50mA |
| Storage temperature range | -55°C to 150°C |
| Junction operating temperature | |
| DG | 175°C |
| DP | 150°C |

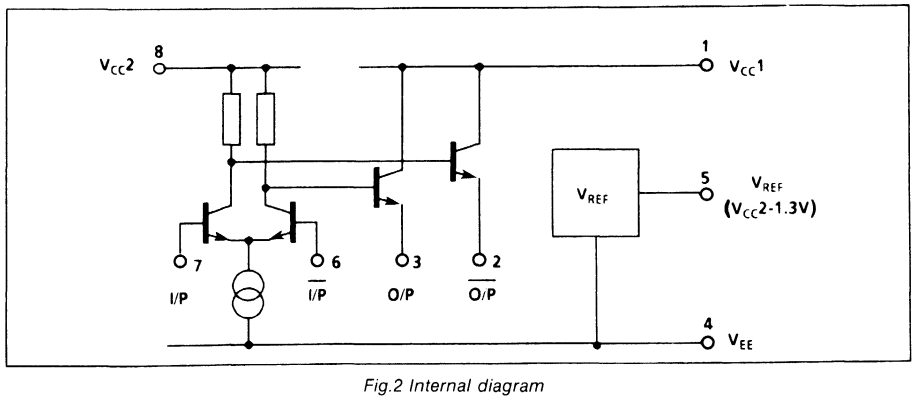



*Fig.2 Internal diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = -40°C to +85°C (DG package), 0°C to +70°C (DP package); $V_{EE}$ = -5.2V ± 0.25V

### DC Characteristics

| Characteristic | Symbol | Value | | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | -40 °c (DG) | | 25 °C (DP & DG) | | 85 °C (DG) | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Power supply current | $I_{EE}$ | | 12 | | 12 | | 12 | mA | No load |
| Input current high | $I_{INH}$ | | | | 350 | | | μA | Inputs ECL high |
| Input leakage current | $I_{cbo}$ | | 50 | | 40 | | 40 | μA | Inputs ECL low |
| Reference voltage | $V_{REF}$ | -1.43 | -1.29 | -1.35 | -1.23 | -1.29 | -1.15 | V | |
| High output voltage | $V_{OH}$ | -1.06 | -0.86 | -0.96 | -0.81 | -0.89 | -0.70 | V | Load = 50Ω to -2V |
| Low output voltage | $V_{OL}$ | -1.90 | -1.66 | -1.85 | -1.62 | -1.83 | -1.57 | V | Load = 50Ω to -2V |
| High input voltage | $V_{IH}$ | -1.19 | -0.88 | -1.09 | -0.81 | -1.03 | -0.7 | V | |
| Low input voltage | $V_{IL}$ | -1.90 | -1.53 | -1.85 | -1.48 | -1.83 | -1.44 | V | |

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Common mode range | $V_{cmr}$ | | 2.85 to 0.8 | | V | At 25°C |
| Input sensitivity (differential) | $V_{pp}$ | | 150 | | mV | At 25°C |
| Differential gain | | | 25 | | dB | At 25°C |

### AC Characteristics

$T_{amb}$ = 25°C

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Propagation delay | $t_{pd}$ | | 0.8 | 0.96 | ns | |
| Transition time, 20 % to 80 % | $t_r$, $t_f$ | | 0.8 | 0.95 | ns | |

NOTE Guaranteed but not tested.

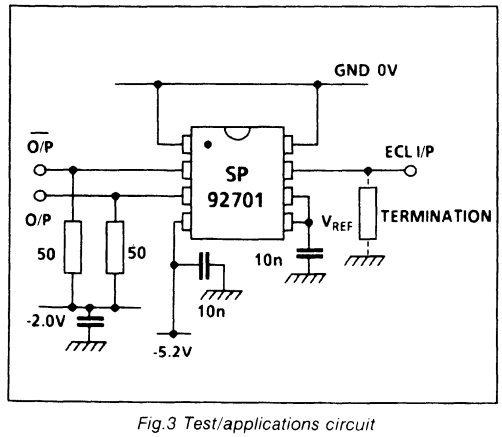



*Fig.3 Test/applications circuit*

## OPERATING NOTES

The SP92701 has been designed primarily for enhancing the edges of ECL signals.

With most systems using ECL it is necessary to minimise the amount of edge jitter on clock signals etc. By reducing the rise times of the ECL edges it is possible to reduce the amount of voltage noise to time jitter conversion that occurs with slower edge speeds.

The SP92701 can also be used to expand fanout and provide conversion from single ended to differential or differential to single ended ECL.

A current source located in the tail of the differential pair (Fig.2) gives the SP92701 a wide common mode range. This enables it to be used in other applications such as comparators or low cost wideband amplifiers.

Used as a line receiver in single ended non-inverting mode, the typical maximum frequency of operation is 700MHz.

### Outputs

The outputs of the SP92701 are open emitter and hence require an external pulldown resistor for evaluation or test. It can also be useful to apply $V_{CC} = +2V$ and $V_{EE} = -3.2V$ for direct drive of 50Ω instruments.

### Schmitt Trigger

Positive feedback can be applied from the output for applications that require input hysteresis.

### Board Layout

Care should be taken with component placement. Use a solid ground plane under the device. Tracks should be short or terminated with their characteristic impedance. The supply pins should be decoupled to ground with good high frequency decoupling capacitors, located close to the device pins.

# SL9999

## 400MHz ADC DRIVER-AMPLIFIER

The Plessey SL9999 is a monolithic high speed high performance operational amplifier. Although primarily intended to drive the inputs of analog to digital converters, the device is capable of driving any other circuit including those that present a low impedance and high capacitive load. Many other internal features such as programmable open loop gain, programmable output current, internal band gap voltage reference, DC buffer and output DC offset circuitry give the device the flexibility for use in a wide range of applications.

### ORDERING INFORMATION

**SL9999C DP** (Commercial Plastic DIL 0° to 70°C)
**SL9999B DG** (Commercial Ceramic DIL -40° to +85°C)
**SL9999B LC** (Commercial LCC -40° to +85°C)
**SL9999C MP** (Commercial Package 0° to 70°C)
**SL9999NA IC** (Naked Chip)
**SL9999AC DG** (MIL 883C Ceramic -55° to +125°C)
**SL9999BB DG** (Plessey High Reliability Ceramic DIL -40° to +85°C)

### FEATURES

- Gain-Bandwidth Product 2GHz at 20dB
- Unity Gain-Bandwidth 400MHz
- Slew Rate 1300V/ µs Rising (typ)
- Slew Rate 630/V µs Falling (typ)
- ±50mA Output Current (Programmable)
- Non-saturating
- High Output Drive
- On-chip LF Buffer for Applying DC Offset
- Flexible Supply Range:
  $V_{CC}$ = +8V to +12V
  $V_{EE}$ = -4.5V to -5.5V
- Output Signal Handling ($V_{CC}$ = +12V, $V_{EE}$ = -5.2V)
  $V_{out}$ = 6V p-p (max.)
- Input Signal Handling ($V_{CC}$ = +12V, $V_{EE}$ = -5.2V)
  $V_{in}$ = +2.8V to -2.5V (max.)

### APPLICATIONS

- High Speed Flash ADC Driver
- Wideband, Buffer/Level Shifter
- Wideband IF Amplification
- Video Amplifier/Line Driver
- Fast Settling Pulse Amplifier
- High Speed Op-Amp Applications

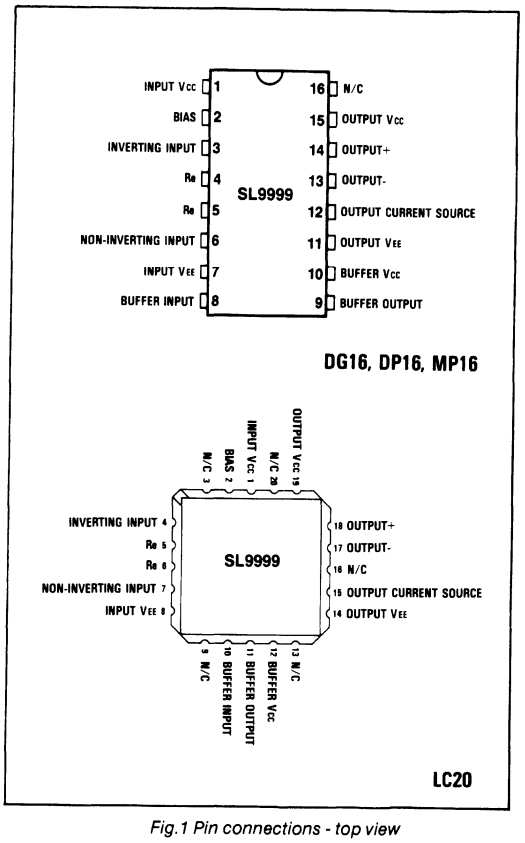



*Fig.1 Pin connections - top view*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage ($V_{CC}$ to $V_{EE}$) | 20V |
| Input Voltage (Inv I/P to Non-Inv I/P) | ±5V |
| Storage Temperature | -65° C to +175° C |
| Chip Operating Temperature | +175° C |
| Operating Temperature: DIL | -55° C to +125° C |
| Thermal Resistances: | |
| DG Chip-to-Ambient: DIL | 120° C/W |
| DG Chip-to-Case: DIL | 40° C/W |
| DP Chip-to-Ambient: DIL | 100° C/W |
| DP Chip-to-Case: DIL | 40° C/W |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25°C, $V_{CC}$ = +12V, $V_{EE}$ = -5V, Test circuit Fig.3.

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Supply current (no load) | | 35 | 43 | mA | $V_{CC}$ = +12V, $V_{EE}$ = -5V |
| Gain-bandwidth product | | 2 | | GHz | ×10 gain |
| Unity gain bandwidth (small sig) | | 400 | | MHz | $R_e$ = 820Ω, $R_L$ = 50Ω |
| Slew rate RISING | 800 | 1300 | | V/μs | $R_L$ = 50Ω |
| Slew rate FALLING | 500 | 630 | | V/μs | $R_L$ = 50Ω |
| Settling time | | 24 | | ns | To 1% (×10 gain) |
| Open loop gain | | 65 | | dB | 50Ω load |
| Maximum $I_{out}$ | | | ±50 | mA | Programmable<br>See Application Notes |
| Output bias current | 15 | 17 | 20 | mA | Pin 12 O/C |
| Supply line rejection | | 40 | | dB | Referred to input |
| Supply voltage $V_{EE}$ to $V_{CC}$ | 12.5 | | 18 | V | |
| Common mode rejection | 55 | | | dB | 50Ω load |
| Input offset (Note 1) | | ±5 | ±15 | mV | $R_e$ = 100Ω |
| Input bias current | | 4.5 | 18 | μA | |
| Buffer bandwidth | | 60 | | MHz | -3dB $R_L$ = 1kΩ |
| Buffer output current | | | 15 | mA | |

NOTE
Input offset is dependent on $R_e$. For lowest offset $R_e$ = 0 ohms.

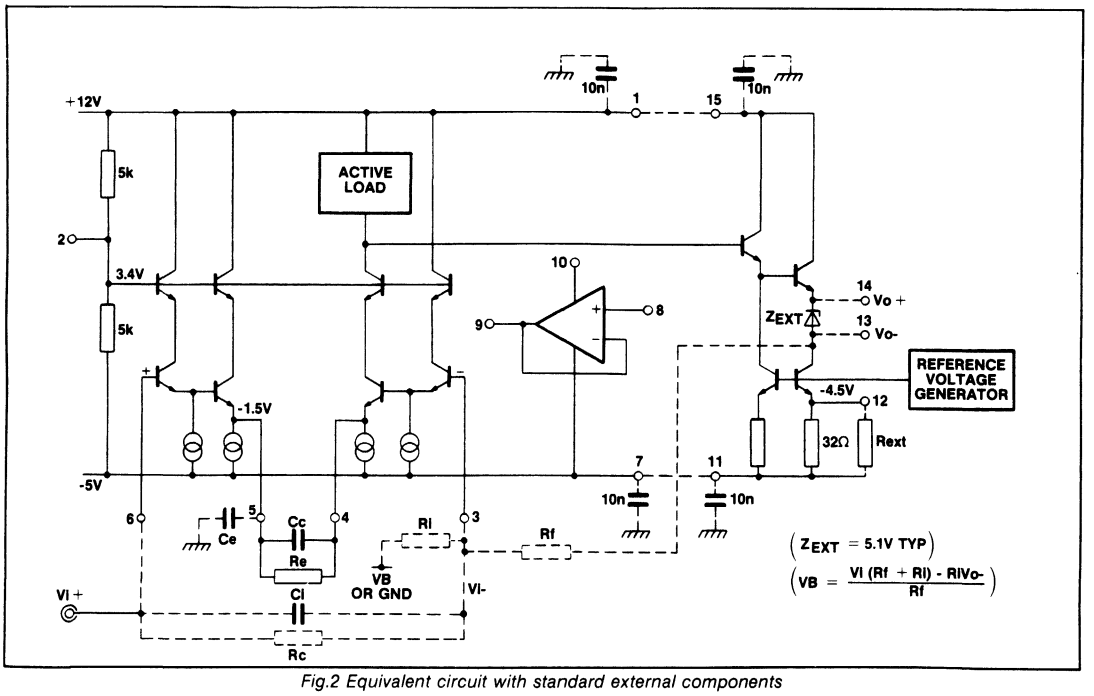



*Fig.2 Equivalent circuit with standard external components*

## APPLICATION NOTES

The SL9999 may be used as a high frequency amplifier in any of the usual op-amp configurations (amplifiers, integrators, etc.).

In most applications, the output of the SL9999 is taken from pin 13 ($V_{out-}$), DC level shifting can be obtained by applying feedback from pin 13 to pin 3 and taking the output from pin 14 ($V_{out+}$, see Fig.2). Alternatively, a DC offset can be applied through the low-drift on-chip buffer (pins 8 and 9) to $V_B$.

The Zener diode between pins 13 and 14 can also be divided into smaller value Zeners or resistors to give a range of DC levels at the output.

### Biasing Conditions (25° C)

For undistorted outputs the peak signal voltages on Vo +, Vo- and the inputs should comply with the following conditions:

A. $Vo+_{(MIN)} \geqslant \frac{V_{CC} + V_{EE}}{2} - 1.4V$

B. $Vo+_{(MAX)} \leqslant V_{CC} - 4.0V$

C. $Vo-_{(MIN)} \geqslant V_{EE} + 1.4V$

D. $Vi+ \text{ and } Vi- \leqslant \frac{V_{CC} + V_{EE}}{2} - 0.9V$

E. $Vi+ \text{ and } Vi- \geqslant V_{EE} + 3.2V$

Bias voltage values at several nodes are indicated on Fig.2.

$R_{ext}$ is connected from pin 12 to pin 11 ($V_{EE}$) to increase output bias current $I_{out}$. This current should not exceed 50mA. The value of $R_{ext}$ is calculated as follows:

$$R_{ext} \equiv \left[\frac{500}{I_{out} - 16}\right] \Omega$$

where $I_{out}$ is in mA.

The on-chip LF buffer has a small-signal bandwidth of 60MHz with 1kΩ load, and has an input/output signal handling capability of 8V. The output can deliver 15mA; an external pull-down resistor is required.

### High Frequency Stability

All component leads should be kept as short as possible, particularly at the summing junction. Also it is important to keep stray capacitance at the summing junction to an absolute minimum.

A ground plane should be used to minimise any earth induced currents between the input and output circuits.

The use of good power supply bypass capacitors (10nF Ceramic) will improve the overall performance. They should be close to the device supply pins. We also recommend electrolytic capacitors in parallel with Ceramic for supply decoupling.

Locate the signal source and load close to the circuit with proper termination - for 50Ω source use a 50Ω bead resistor. Other resistors should be carbon composition.

### Voltage Gain

Stable closed loop operation is ensured by changing the value of the degeneration resistor ($R_e$) between pins 4 and 5 according to the selected closed loop gain. As closed loop gain decreases the value of $R_e$ should be increased.

A graph of recommended $R_e$ with gain is given in Fig.4.

### Power Dissipation

A Zener diode is used between pins 13 and 14 to dissipate power externally and to provide a DC offset at the output.

For -5V, +12V range a 4.7V to 5.1V Zener may be used.

For lower cost applications a bypass resistor can conveniently replace the Zener diode. Its value may be calculated from the voltage drop and current through the output stage. For example, for 15mA output current a 33Ω resistor could be used.

Although some power is dissipated in the external Zener, a heatsink on the SL9999 will be necessary if the power to be dissipated exceeds 800mW.

### Bandwidth Compensation

Bandwidth at higher gains can be improved by a capacitor ($C_c$) across the degeneration resistor $R_e$. For example, a non-inverting closed loop gain of 10, 10pF will increase the bandwidth to 280MHz at 50Ω load condition.

A decoupling capacitor ($C_e$) from pin 5 will compensate the first pole roll-off and hence reduce the noise bandwidth. For a 200MHz bandwidth an 18pF capacitor may be used with the suggested PCB layout on page 6.

A capacitor ($C_i$) and resistor ($R_c$) of suitable value between the two inputs will reduce high frequency peaking.

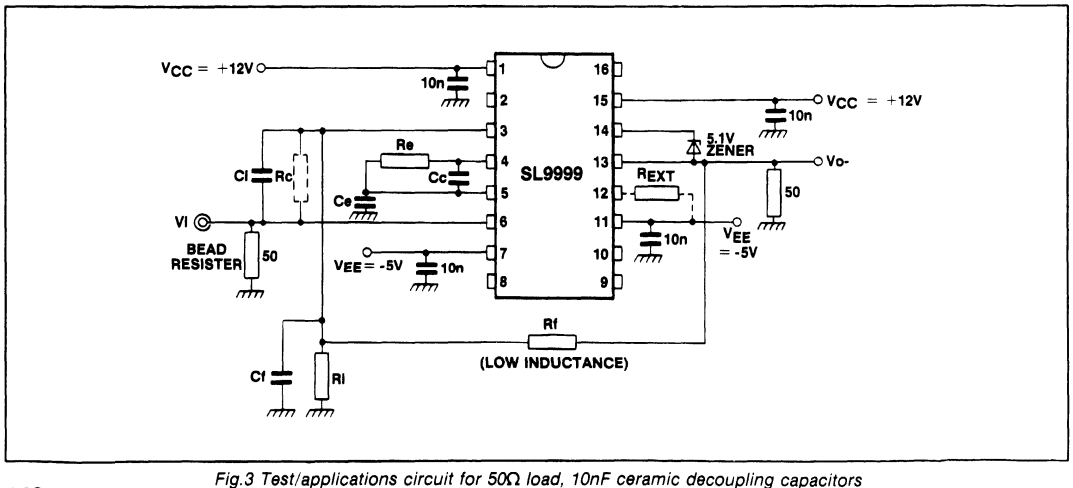



*Fig.3 Test/applications circuit for 50Ω load, 10nF ceramic decoupling capacitors*

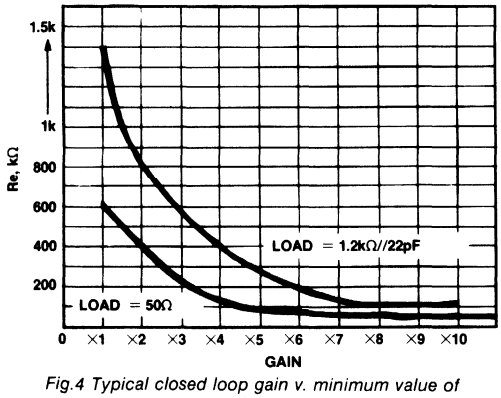



*Fig.4 Typical closed loop gain v. minimum value of degeneration resistor $R_e$*

*NOTE: Input offset is proportional to $R_e$ value*

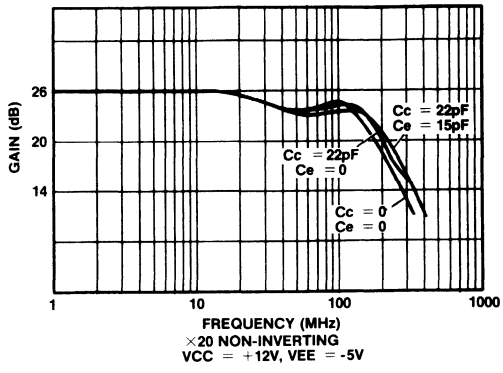



*Fig.5 Typical frequency response for the test circuit of Fig.3, ×20 gain, non-inverting, 50Ω load, $R_f$ = 10.6kΩ, $R_1$ = 560Ω, $R_e$ = 22Ω.*

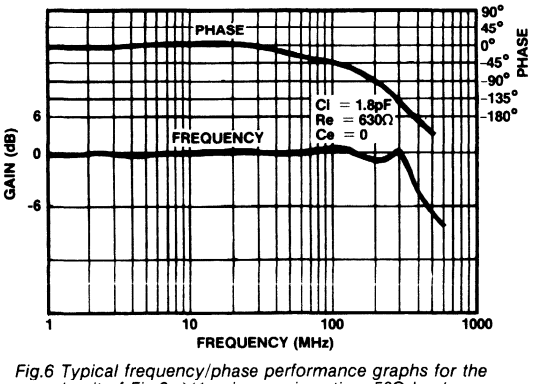



*Fig.6 Typical frequency/phase performance graphs for the circuit of Fig.3, ×1 gain, non-inverting, 50Ω load, $R_f$ = 560Ω, $R_1$ = ∞.*

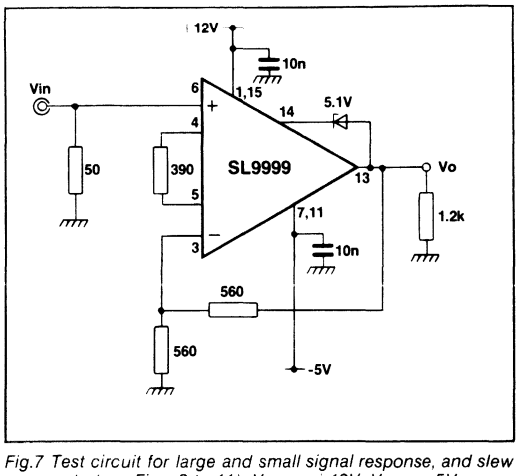



*Fig.7 Test circuit for large and small signal response, and slew rate (see Figs. 8 to 11). $V_{CC}$ = +12V, $V_{EE}$ = -5V.*

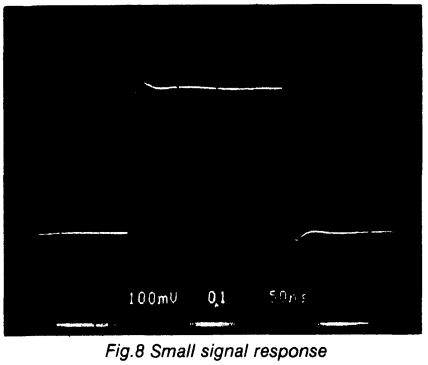



*Fig.8 Small signal response*

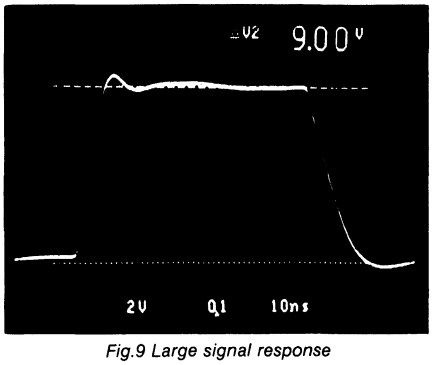



*Fig.9 Large signal response*

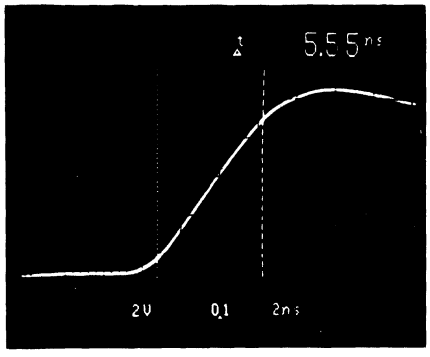



*Fig.10 Rising edge 10% to 90% points 1300V/μs*

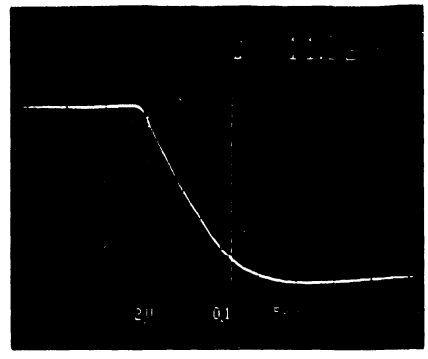


*Fig.11 Falling edge 10% to 90% points 630V/μs*

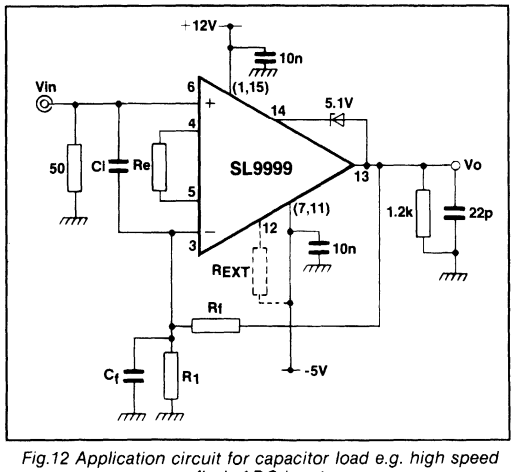



*Fig.12 Application circuit for capacitor load e.g. high speed flash ADC input*

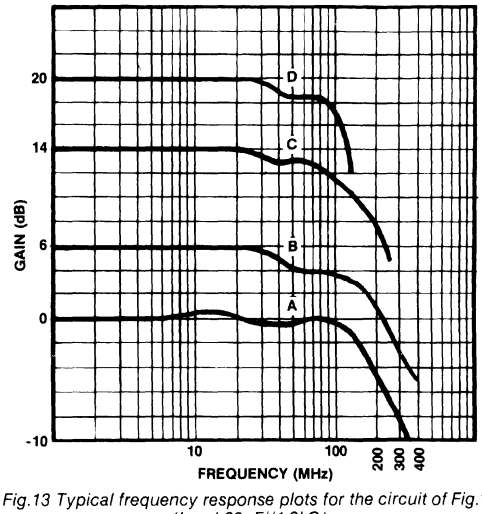



*Fig.13 Typical frequency response plots for the circuit of Fig.12 (Load 22pF//1.2kΩ).*

## TYPICAL APPLICATION

| Response (see Fig.13) | Gain | $R_f$ (Ω) | $R_i$ (Ω) | $R_e$ (Ω) | $C_f$ (Pf) | $R_{ext}$ (Ω) | VO/P (p-p) | $V_{CC}$ (V) | $V_{EE}$ (V) |
|---|---|---|---|---|---|---|---|---|---|
| A | ×1 | 2.2k | ∞ | 1.8k | 0 | ∞ | 1 | +12 | -5 |
| B | ×2 | 560 | 560 | 1.2k | 18 | 50 | 2 | +12 | -5 |
| C | ×5 | 2.2k | 560 | 270 | 10 | ∞ | 1 | +12 | -5 |
| D | ×10 | 5.6k | 560 | 68 | 0 | 10 | 1 | +12 | -5 |

*Table 1 Recommended components values for the test circuit of Fig.12*

NOTE
$C_f$ and $C_i$ are dependent on layout and used to compensate the effects of strays.

For applications that require accurate gain flatness over the full frequency range, the inverting mode of operation is recommended. See Fig.14.

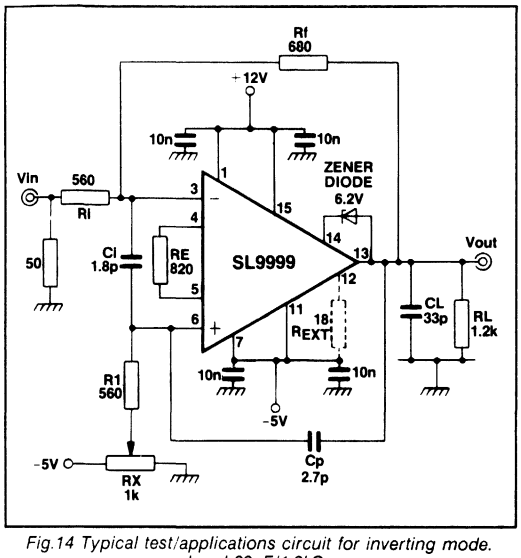



*Fig.14 Typical test/applications circuit for inverting mode. Load 33pF/1.2kΩ.*

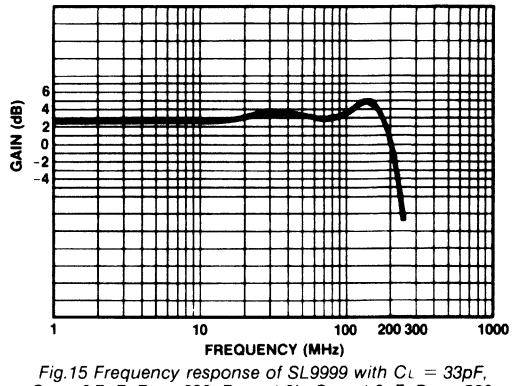
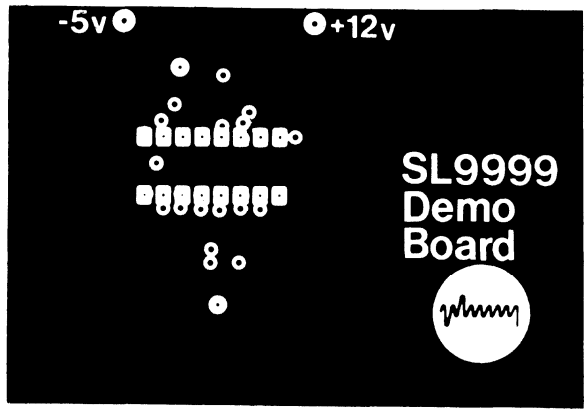
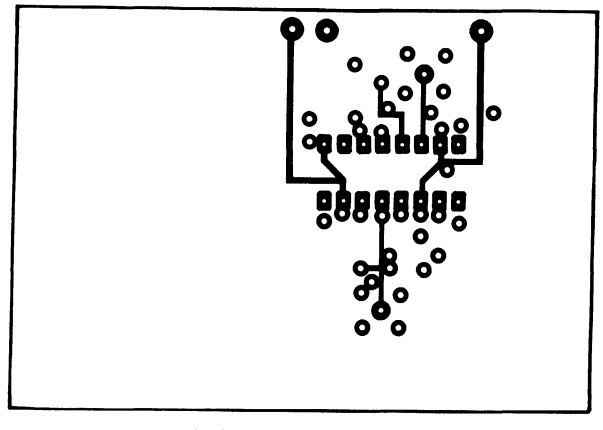



*Fig.15 Frequency response of SL9999 with $C_L$ = 33pF, $C_p$ = 2.7pF, $R_f$ = 680, $R_L$ = 1.2k, $C_i$ = 1.8pF, $R_1$ = 560, $V_O$ = 1V p-p (See Test Circuit of Fig.14)*

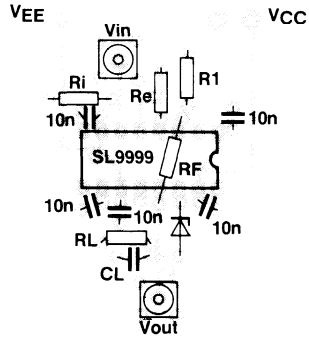
## CONSTRUCTION




*(a) SL9999 ground plane, component side*

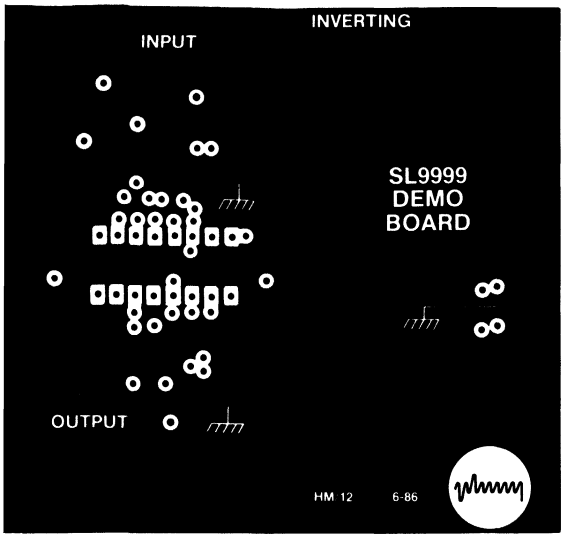


*(b) SL9999 board, track side*

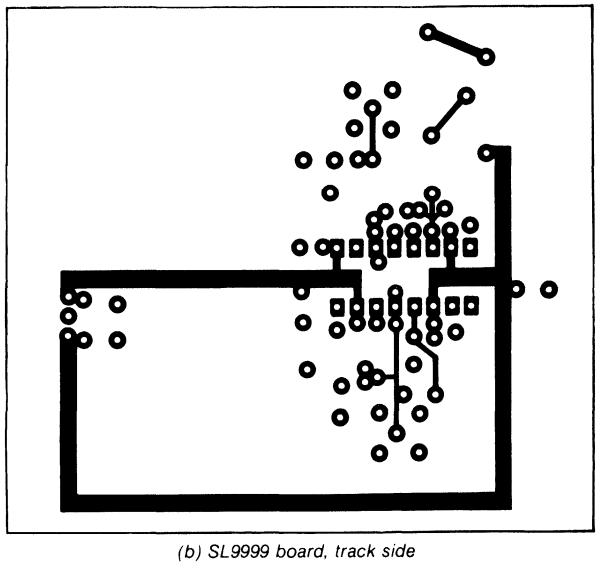



*(c) Component location. NOTE: I/P and O/P are sub-vis type 50Ω connectors.*

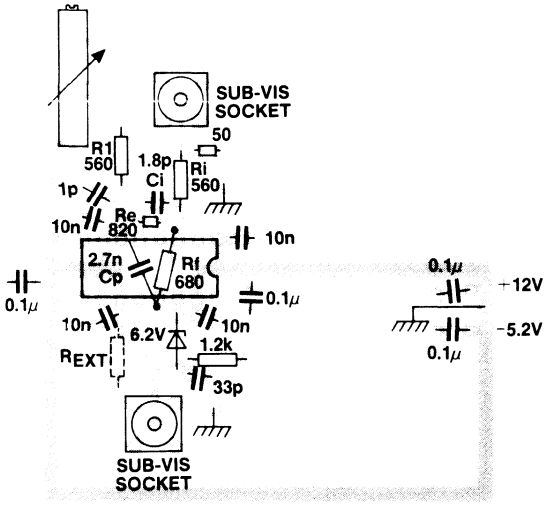
*Fig.16 PCB layout for SL9999 demonstration board (Fig.12) viewed from component side and underside*




(a) SL9999 ground plane, component side



(b) SL9999 board, track side




(c) Component location (1:1 scale)

*Fig.17 PCB layout for SL9999 demonstration board. NOTE: I/P and O/P are sub-vis type 50Ω connectors. Rf and Cf are on the track side. Gold socket pins to mount SL9999 for test circuit*

# Technical Data

## 3. Specialised memory products

PLESSEY
Semiconductors

# MJ2812, MJ2812M 32 WORDS x 8 BIT FIFO MEMORY
# MJ2813, MJ2813M 32 WORDS x 9 BIT FIFO MEMORY

The MJ2812 and MJ2813 are 32-word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three state outputs controlled by an output enable pin (OE). Data on the data inputs ($D_0$ – $D_7$) is written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word.

Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs ($Q_0$ – $Q_7$) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready signal (IR) indicates that the device is ready to accept data and also provides a memory full signal.

Both the MJ2812 and MJ2813 have master reset inputs which initialise the FIFO control logic and clear all data from the device (reset to all lows). A FLAG signal goes high when the memory is approximately half full.

The MJ2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the $D_0$ input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built in parallel-to-serial converter, so that data can be shifted out of the Q7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals PL, IR, PD and OR are designed so that two FIFOs can be placed end-to-end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

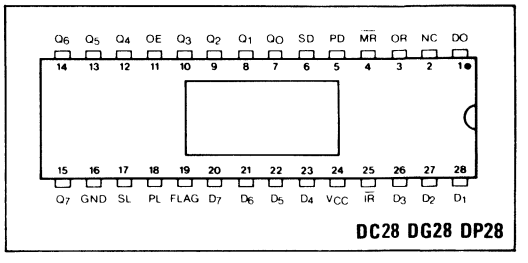



*Fig. 1 MJ2812 (32 x 8) pin connections*

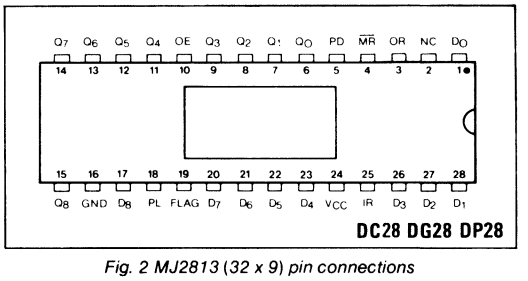



*Fig. 2 MJ2813 (32 x 9) pin connections*

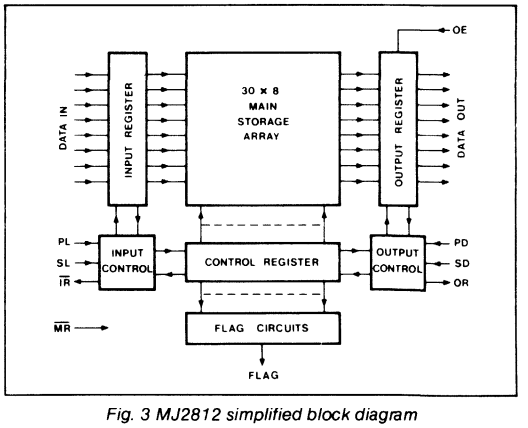



*Fig. 3 MJ2812 simplified block diagram*

## FEATURES

- Serial or Parallel Inputs and Outputs (MJ2812 only)
- 32 Words x 8 Bits (MJ2812) and 32 Words x 9 Bits (MJ2813)
- Easily Stacked – Sideways or Lengthways
- Independent Reading and Writing
- Half-Full FLAG
- Data Rates up to 2.0MHz
- Last Word Retention
- TTL – Compatible Tri-state Outputs
- Input and Output Ready Signals
- Master Reset
- Single +5V Supply

## APPLICATIONS

- Smoothing Data Rates from Keyboards
- Buffer Between Differently-Clocked Systems (Short Fast Bursts into Steady Data Stream, and Vice Versa)
- Temporary Storage in Error Removing Systems which use Repeated Transmission
- Buffer Store in Interrupt-Orientated Systems
- Computer-to-Line Printer Buffer

## OPERATING RANGE

| Type number | Ambient temperature | $V_{CC}$ | Ground |
|---|---|---|---|
| MJ2812/MJ2813 | 0°C to +70°C | 5.0V ±5% | 0V |
| MJ2812M/MJ2813M | −55°C to +125°C | 5.0V ±5% | 0V |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
As specified in Operating Range table (above)

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output high voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH} = -0.3mA$ |
| Output low voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL} = 1.6mA$ |
| Input high voltage | $V_{IH}$ | 2.5 | | | V | |
| Input low voltage | $V_{IL}$ | | | 0.8 | V | |
| Input leakage current | $V_{IL}$ | | | 10 | µA | $V_{IN} = 0V$ |
| Input high current | $V_{IH}$ | | | 10 | µA | $V_{IN} = 5.25V$ |
| $V_{CC}$ current | $I_{CC}$ | | 70 | 114 | mA | $T_A = 0°C$ to $+70°C$ |
| | | | 70 | 120 | mA | $T_A = -55°C$ to $+125°C$ |

**Switching Characteristics**

| Characteristic | Symbol | Type | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Maximum parallel load or dump frequency | $f_p$ | 2812/3 | 2.05 | | | Mhz | |
| | | 2812M/3M | 1.5 | | | MHz | |
| Delay, PL or SL high to IR inactive | $t_{IR+}$ | 2812/3 | | 90 | 200 | ns | |
| | | 2812M/3M | | 90 | 250 | ns | |
| Delay, PL or SL low to IR active | $t_{IR-}$ | 2812/3 | | 140 | 350 | ns | |
| | | 2812M/3M | | 140 | 400 | ns | |
| Minimum PL or PD high time | $t_{pwH(P)}$ | All | | | 80 | ns | |
| Minimum PL or PD low time | $t_{pwL(P)}$ | All | | | 100 | ns | |
| Minimum SL or SD high time | $t_{pwH(S)}$ | All | | | 80 | ns | |
| Minimum SL or SD low time | $t_{pwl(S)}$ | All | | | 80 | ns | |
| Data hold time | $t_{h(D)}$ | All | | 130 | 200 | ns | |
| Data set-up time | $t_{s(D)}$ | All | | | 0 | ns | to PL |
| | | All | | | 0 | ns | to SL |
| Delay, PD or SD high to OR low | $t_{OR+}$ | 2812/3 | | 110 | 240 | ns | OE high |
| | | 2812M/3M | | 110 | 260 | ns | OE high |
| Delay, PD or SD low to OR high | $t_{OR-}$ | 2812/3 | | 180 | 400 | ns | DE high |
| | | 2812M/3M | | 180 | 400 | ns | DE high |
| Ripple through time | $t_{PT}$ | 2812/3 | | 1.0 | 2.5 | µs | FIFO empty |
| | | 2812M/3M | | 1.0 | 3.0 | µs | FIFO empty |
| Delay, OR low to data out changing | $t_{DH}$ | All | | 90 | | ns | PD=low |
| Delay, data out to OR high | $t_{DA}$ | All | | 70 | | ns | PD=high |
| Minimum reset pulse width | $t_{MRW}$ | 2812/3 | | | 290 | ns | |
| | | 2812M/3M | | | 300 | ns | |
| Delay, OE low to output off | $t_{DO}$ | All | | | 250 | ns | |
| Delay, OE high to output active | $t_{EO}$ | All | | | 250 | ns | |
| Delay from PL or SL low to FLAG high or PD or SD low to FLAG low | $t_{DF}$ | All | | | 1.0 | µs | |
| Input capacitance | $c_i$ | All | | | 7 | pF | |

NOTES
1. IR is active high on MJ2813 and active low on MJ2812
2. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

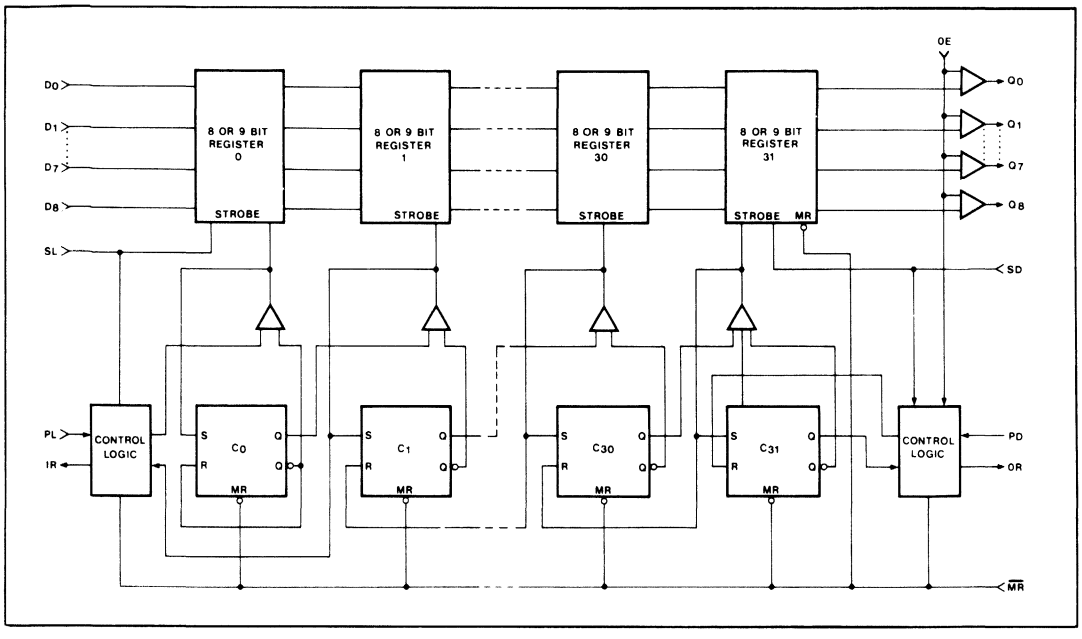



*Fig. 4 Logic block diagram*

## MJ2812 AND MJ2813 FIFO OPERATION

The MJ2812 and MJ2813 FIFO's consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the (n)th bit of the control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the (n)th data register, simultaneously setting the (n+1)th control register bit and clearing the (n)th control register bit, so that the control strobe moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a low-to-high transition on the parallel load (PL) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now 'busy', unable to accept more data. When PL next goes low, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This caused IR to go active, indicating the inputs are available for another data word.

Note: The device will malfunction if a data load is attempted when the inputs are not ready (as indicated by the IR output signals).

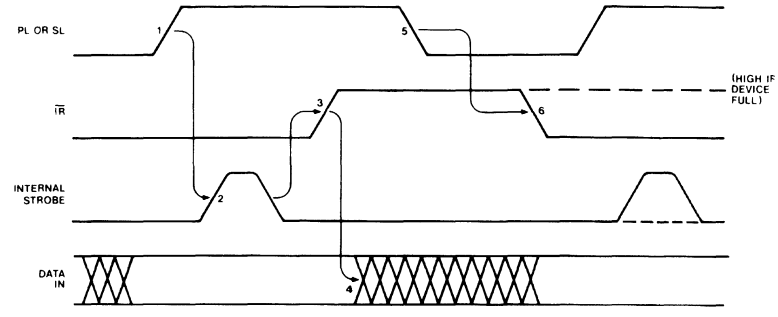
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A low-to-high transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes low, the '0' which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The '0' in the control register than 'bubbles' back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes high, OR will go low as before, but when PD next goes low, there is no data to move into the last location, so OR remains low until more data arrives at the output. The previous word is retained at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes low, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

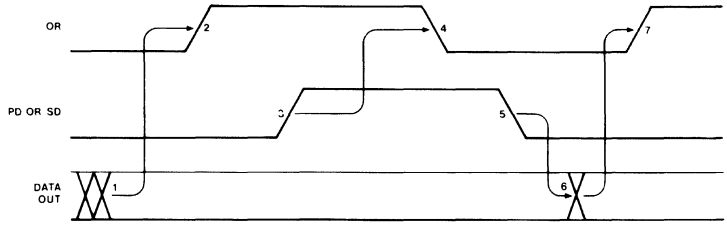
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage temperature | −65°C to +150°C |
| Temperature (ambient) under bias | −55°C to +125°C |
| Voltage on any pin w.r.t. ground (0V) | −0.3V to +9V |
| DC input voltage | −0.3V to +6V |




**MJ2812 INPUT TIMING**

When data is steady PL is brought high (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes high (3) and data may be changed (4). $\overline{IR}$ remains high until PL is brought low (5); then $\overline{IR}$ goes low (6) indicating new data may be entered.




**MJ2812 OUTPUT TIMING**

When data out is steady (1), OR goes high (2). When PD goes high (3), OR goes low (4). When PD goes low again (5), the output data changes (6) and OR returns high (7).

The input and output timing diagram above illustrate the sequence of control on the MJ2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The MJ2813 pattern is similar, but IR is active high instead of active low.

*Fig. 5 MJ2812 timing diagram*

Because the input ready signal is active low on the MJ2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two MJ2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n MJ2812s connected end-to-end store 31n+1 words (instead of 32n). The MJ2813 stores 32n words in this configuration, because IR is active high and does dump the last word written into the second device.

### Flag Output

A flag output is available on the MJ2812 and MJ2813 to indicate when the FIFO is approximately half full. Assuming the memory is empty, the flag output will go high within 1μs of the 13th word being loaded into the memory (14 high-low transitions on PL or 112 transitions on SL). Assuming a full memory the flag output will go low within 1μs of the 20th PD or 160th SD high-low transition, ie. when 13 words remain in the memory.

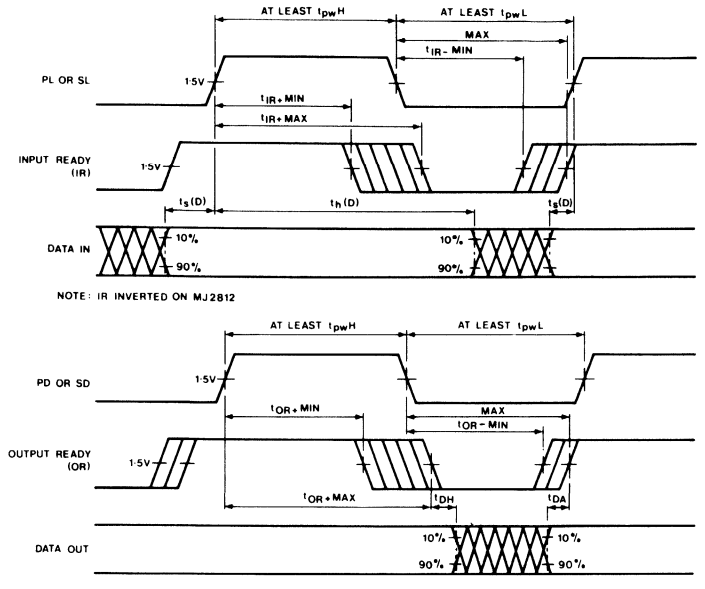
### Serial Input and Output (MJ2812 Only)

The MJ2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to $D_0$ input.

The SL signal operates just like the PL input, causing IR to go high and low as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they have been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the $Q_7$ output. OR moves high and low with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and the new 8-bit word is brought to the output. OR will stay low if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.




**KEY TO TIMING DIAGRAM**

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DONT CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |

*Fig. 6 Timing diagram*

## OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain low, indicating data at the output is not valid.

2. When the output data changes as a result of a pulse on PD, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.

3. If PD is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR-}$) and then will go back low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought low.

4. When the master reset is brought low, the control register and the outputs are cleared and the control logic is initialised. $\overline{IR}$ and OR go low. If PL is high when the master reset goes high then $\overline{IR}$ will remain in the high state until PL is brought low. If PL is low when the master reset is ended, then $\overline{IR}$ will be low until PL goes high.

5. The output enable pin OE inhibits dump commands while it is low and forces the Q outputs to a high impedance state.

6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.

7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

8. The $\overline{IR}$ and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If the specified minimum pulse widths, for PL, SL, PD or SD are not provided *after* an $\overline{IR}$ or OR transition the memory may corrupt and lock out any further data input. The memory should be cleared to restore normal operation.

# MJ2812HS

## 32 WORDS x 8 BIT FIFO MEMORY

The MJ2812HS is a high speed version of the MJ2812 32-word by 8-bit first-in first-out memory. The device has completely independent read and write controls and three state outputs controlled by an output enable pin (OE). Data on the data inputs ($D_0$ - $D_7$) is written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word.

Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs ($Q_0$ - $Q_7$) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready signal ($\overline{IR}$) indicates that the device is ready to accept data and also provides a memory full signal.

The MJ2812HS has master reset inputs which initialise the FIFO control logic and clear all data from the device (reset to all lows). A FLAG signal goes high when the memory is approximately half full.

The MJ2812HS can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the $D_0$ input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built in parallel-to-serial converter, so that data can be shifted out of the $Q_7$ output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals PL, $\overline{IR}$, PD and OR are designed so that two FIFOs can be placed end-to-end, with OR of the first driving PL of the second and $\overline{IR}$ of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep. Cascadability is only guaranteed up to 3MHz data rate.

### FEATURES

- Serial or Parallel Inputs and Outputs
- 32 Words x 8 Bits
- Stand Alone
- Easily Stacked Sideways
- Data Rates up to 5.0MHz
- Independent Reading and Writing
- Half-Full FLAG
- Last Word Retention
- TTL — Compatible Tri-state Outputs
- Input and Output Ready Signals
- Master Reset
- Single +5V Supply

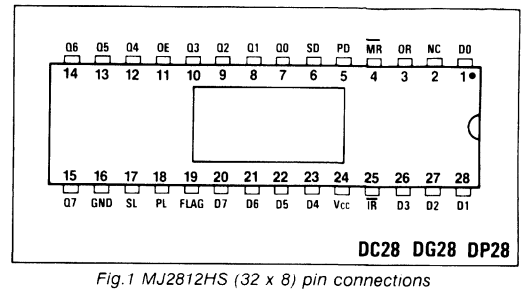



*Fig.1 MJ2812HS (32 x 8) pin connections*

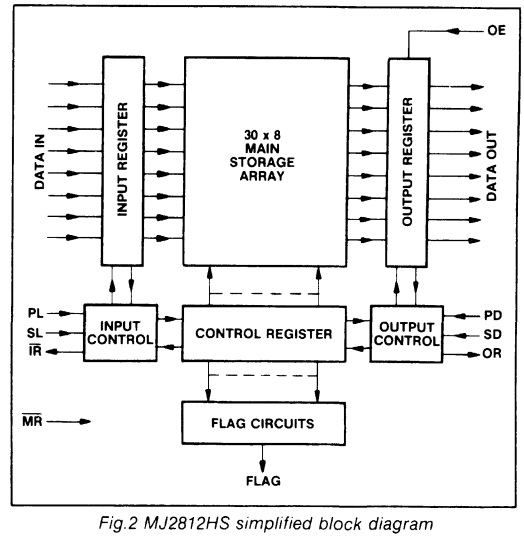



*Fig.2 MJ2812HS simplified block diagram*

### APPLICATIONS

- Smoothing Data Rates from Keyboards
- Buffer Between Differently-Clocked Systems (Short Fast Bursts into Steady Data Stream, and Vice Versa)
- Temporary Storage in Error Removing Systems which use Repeated Transmission
- Buffer Store in Interrupt-Orientated Systems
- Computer-to-Line Printer Buffer

## OPERATING RANGE

| Type number | Ambient temperature | Vcc | Ground |
|---|---|---|---|
| MJ2812HS | 0°C to +70°C | 5.0V ± 5% | 0V |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
As specified in Operating Range table (above)

### Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output high voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -0.3mA |
| Output low voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6mA |
| Input high voltage | $V_{IH}$ | 2.5 | | | V | |
| Input low voltage | $V_{IL}$ | | | 0.8 | V | |
| Input leakage current | $V_{IL}$ | | | 10 | μA | $V_{IN}$ = 0V |
| Input high current | $V_{IH}$ | | | 10 | μA | $V_{IN}$ = 5.25V |
| Vcc current | $I_{CC}$ | | 70 | 114 | mA | $T_{amb}$ = 0°C to +70°C |
| | | | 70 | 120 | mA | $T_{amb}$ = -55°C to +125°C |

### Switching Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum parallel load or dump frequency | $f_p$ | 4.1† | 5 | | MHz | |
| Delay, PL or SL high to $\overline{IR}$ inactive | $t_{IR+}$ | | 180 | 200 | ns | |
| Delay, PL or SL low to $\overline{IR}$ active | $t_{IR}$ | | 200 | 350 | ns | |
| Minimum PL or PD high time | $t_{pwH(P)}$ | | | 80 | ns | |
| Minimum PL or PD low time | $t_{pwL(P)}$ | | | 100 | ns | |
| Minimum SL or SD high time | $t_{pwH(S)}$ | | | 80 | ns | |
| Minimum SL or SD low time | $t_{pwl(S)}$ | | | 80 | ns | |
| Data hold time | $t_{h(D)}$ | | | 200 | ns | |
| Data set-up time | $t_{s(D)}$ | | | 0 | ns | to PL |
| | | | | 0 | ns | to SL |
| Delay, PD or SD high to OR low | $t_{OR+}$ | | 125 | 240 | ns | OE high |
| Delay, PD or SD low to OR high | $t_{OR-}$ | | 200 | 400 | ns | DE high |
| Ripple through time | $t_{PT}$ | | 1.0 | 2.5 | μs | FIFO empty |
| Delay, PD low to data out changing | $t_{DH}$ | | | 240 | ns | |
| Delay, data out to OR high | $t_{DA}$ | 0 | | | ns | PD = high |
| Minimum reset pulse width | $t_{MRW}$ | | | 290 | ns | |
| Delay, OE low to output off | $t_{DO}$ | | | 250 | ns | |
| Delay, OE high to output active | $t_{EO}$ | | | 250 | ns | |
| Delay from PL or SL low to FLAG high or PD or SD low to FLAG low | $t_{DF}$ | | 700 | 1.0 | ns | |
| Input capacitance | $C_I$ | | | 7 | pF | |

NOTES
1. $\overline{IR}$ is active low.
2. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

† Cascadability is only guaranteed up to 3MHz.

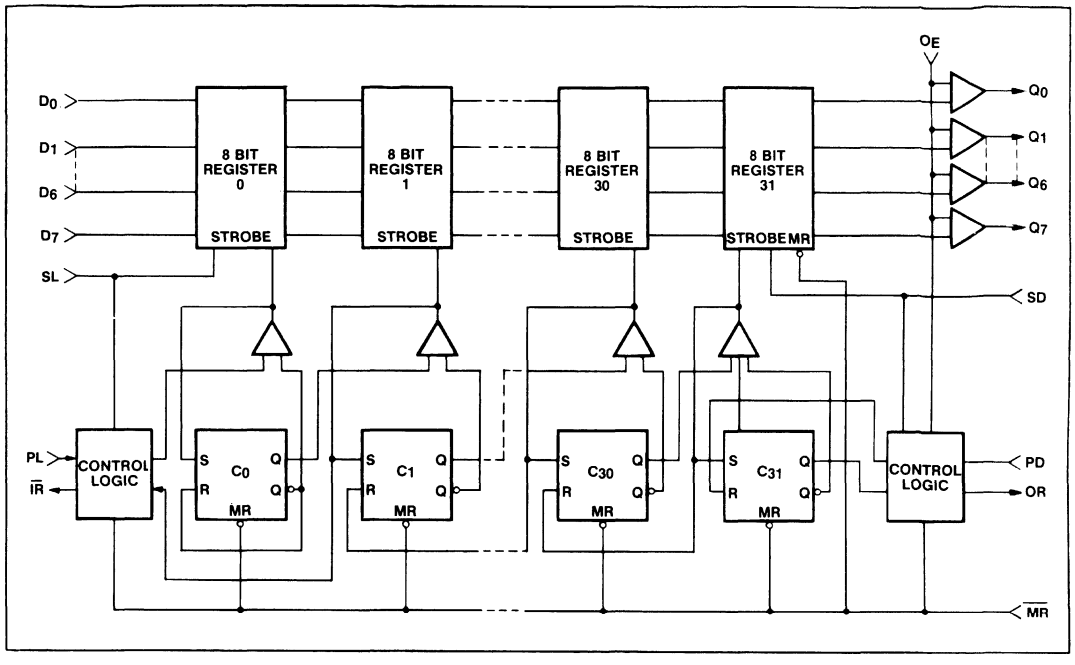



*Fig.3 Logic block diagram*

## MJ2812HS FIFO OPERATION

The MJ2812HS FIFO consists internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the (n)th bit of the control register contains a '1' and the (n + 1)th bit contains a '0', then a strobe is generated causing the (n + 1)th data register to read the contents of the (n)th data register, simultaneously setting the (n + 1)th control register bit and clearing the (n)th control register bit, so that the control strobe moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through opertion stops when the data reaches a register n with a '1' in the (n + 1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a low-to-high transition on the parallel load (PL) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready ($\overline{IR}$) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now 'busy', unable to accept more data. When PL next goes low, the fall through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This caused $\overline{IR}$ to go active, indicating the inputs are available for another data word.

Note: The device will malfunction if a data load is attempted when the inputs are not ready (as indicated by the $\overline{IR}$ output signals).

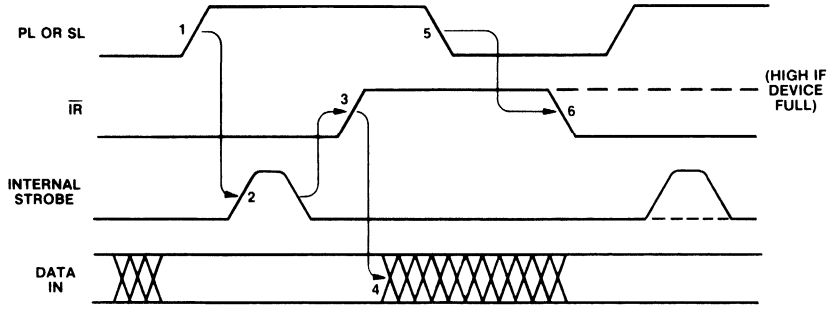
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A low-to-high transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes low, the '0' which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The '0' in the control register then 'bubbles' back toward the input as the data shifts towards the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes high, OR will go low as before, but when PD next goes low, there is no data to move into the last location, so OR remains low until more data arrives at the output. The last data word will be retained at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes low, and $\overline{IR}$ will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the $\overline{IR}$ output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

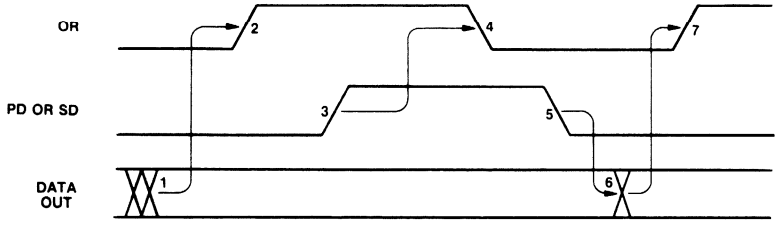
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage temperature | -65° C to +150° C |
| Temperature (ambient) under bias | -55° C to +125° C |
| Voltage on any pin w.r.t. ground (0V) | -0.3V to +9V |
| DC input voltage | -0.3V to +6V |




**MJ2812HS INPUT TIMING**

When data is steady PL is brought high (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes high (3) and data may be changed (4). $\overline{IR}$ remains high until PL is brought low (5); then $\overline{IR}$ goes low (6) indicating new data may be entered.




**MJ2812HS OUTPUT TIMING**

When data out is steady (1), OR goes high (2). When PD goes high (3), OR goes low (4). When PD goes low again (5), the output data changes (6) and OR returns high (7).

The input and output timing diagram above illustrate the sequence of control on the MJ2812HS. Note that PL matches OR and IR matches PD in time, as though the signals were driving each other.

*Fig.4 MJ2812HS timing diagram*

Because the input ready signal is active low on the MJ2812HS a peculiarity occurs when several devices are placed end-to-end. When the second unit of two MJ2812HSs fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n MJ2812HSs connected end-to-end store 31n + 1 words (instead of 32n).

## Flag Output

A flag output is available on the MJ2812HS to indicate when the FIFO is approximately half full. Assuming the memory is empty, the flag output will go high within 1$\mu$s of the 13th word being loaded into the memory (14 high-low transitions on PL or 112 transitions on SL). Assuming a full memory the flag output will go low within 1$\mu$s of the 20th PD or 160th SD high-low transition, i.e. when 13 words remain in the memory.

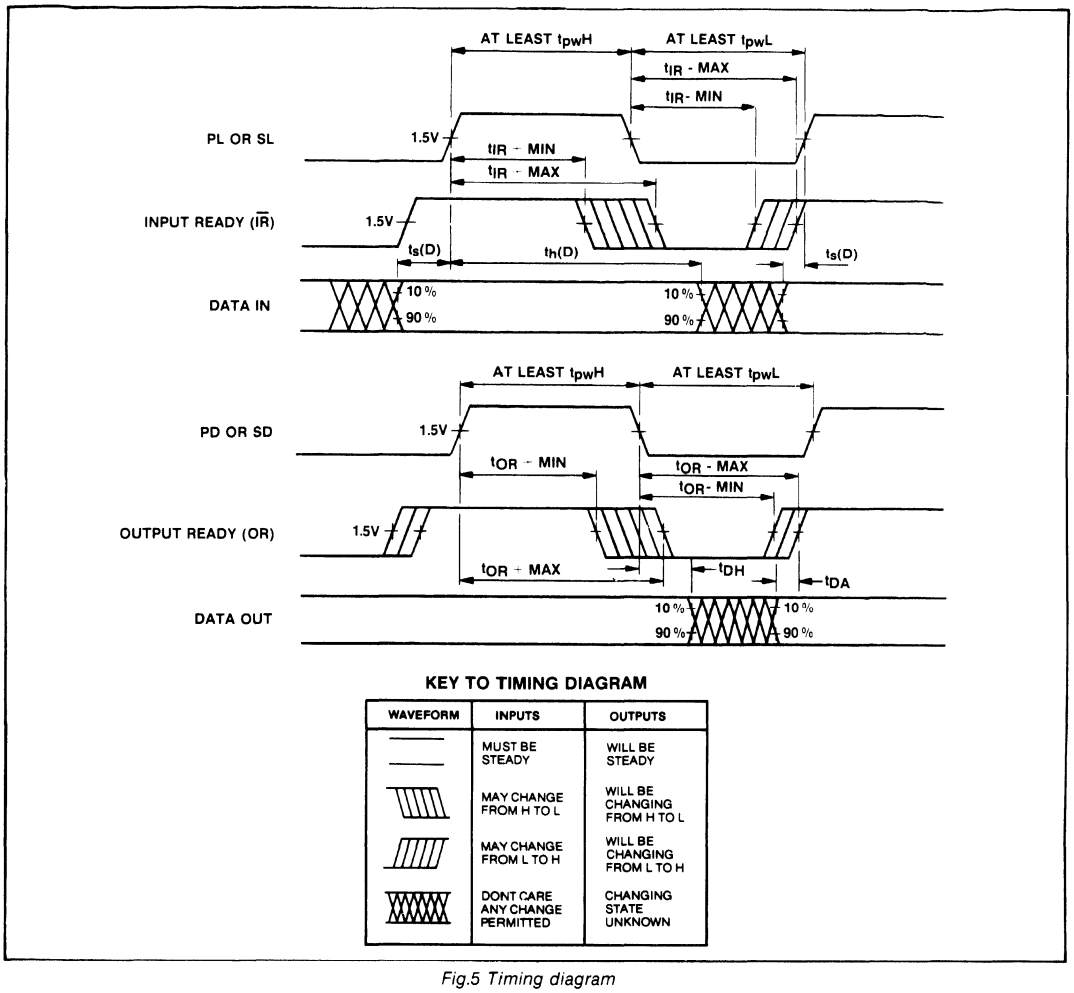
## Serial Input and Output

The MJ2812HS also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to $D_0$ input.

The SL signal operates just like the PL input, causing $\overline{IR}$ to go high and low as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they have been loaded in parallel. Following the 8th SL pulse, $\overline{IR}$ will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the $Q_7$ output. OR moves high and low with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and the new 8-bit word is brought to the output. OR will stay low if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.




**KEY TO TIMING DIAGRAM**

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DONT CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |

*Fig.5 Timing diagram*

## OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain low, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on PD, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so any time OR is high, there is good, stable data on the outputs.
3. If PD is held high while the memory is emptied and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR+}$) and then will go back low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought low.
4. When the master reset is brought low, the control register and the outputs are cleared and the control logic is initialised. $\overline{IR}$ and OR go low. If PL is high when the master reset goes high then $\overline{IR}$ will remain in the high state until PL is brought low. If PL is low when the master reset is ended, then $\overline{IR}$ will be low until PL goes high.
5. The output enable pin OE inhibits dump commands while it is low and forces the Q outputs to a high impedance state.
6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.
7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.
8. The $\overline{IR}$ and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If the specified minimum pulse widths, for PL, SL, PD or SD are not provided *after* an $\overline{IR}$ or OR transition the memory may corrupt and lock out any further data input. The memory should be cleared to restore normal operation.

PLESSEY
Semiconductors

# MJ2841

## 64-WORD x 4-BIT FIRST-IN FIRST-OUT MEMORY

The MJ2841 is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four bit parallel word $D_0$-$D_3$ under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs $Q_0$-$Q_3$. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written.

A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFO's to obtain deeper stacks.

Parallel expansion to wider words only requires that rows of FIFO's be placed side by side. Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage temperature | -55°C to +125°C |
| Ambient operating temperature | -10°C to +85°C |
| Lead temperature (soldering, 10s max.) | 330°C |
| Voltage on any pin with respect to ground | -0.3V to +7V |

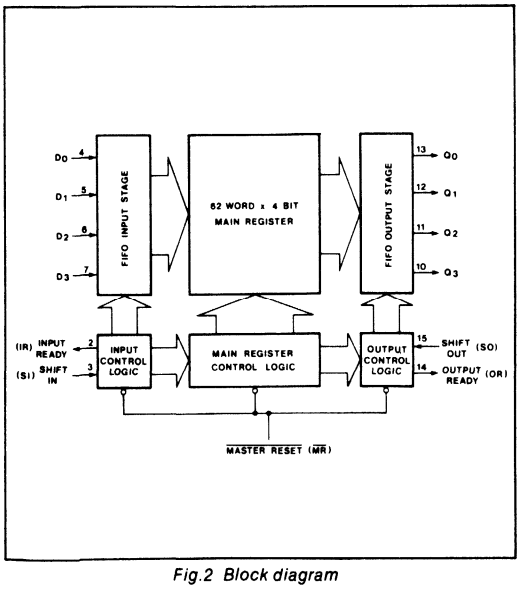



*Fig.2 Block diagram*

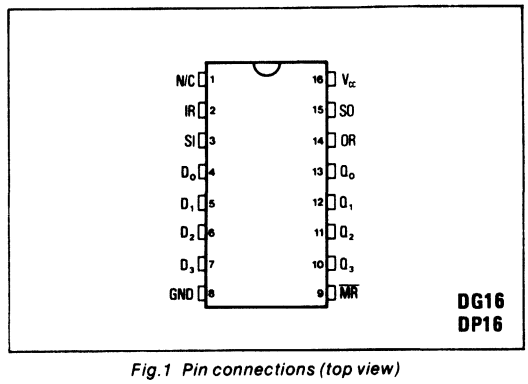



*Fig.1 Pin connections (top view)*

### FEATURES

- Single 5V Supply
- 1.75MHz Guaranteed Data Rate (Typically 4MHz)
- Pin Compatible with AM2841/Fairchild 3341
- Asynchronous Buffer For Up To 64 Four Bit Words
- Easily Expandable To Larger Buffers

### MJ2841 FIFO OPERATION

The MJ2841 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the $n^{th}$ bit of control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the $n^{th}$ data register, simultaneously setting the (n+1)th control register bit, so that the control flag moves with the data. In this fashion, data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs $D_0$-$D_3$ by applying a low to high transition on the shift in (SI) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes low indicating that data has been entered into the first data register and

the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the first control register bit is cleared. This causes IR to go high indicating the inputs are available for another data word.

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the four data outputs $Q_0$-$Q_3$. An input signal, shift out (SO) is used to shift the data out of the FIFO. A low to high transition on SO clears the last register bit, causing OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the '0' which is now present at the last register allows the data in the next to last register position to move into the last register position and on to the outputs. The '0' in the control register then 'bubbles' back towards the input as the data shifts towards the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes high, OR will go low as before, but when SO next goes low, there is no data to move into the last location so OR remains low until more data arrives at the output. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the outputs to all low).

## OPERATING NOTES

**1.** When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However OR will remain low, indicating data at the output is not valid.

**2.** When the output data changes as a result of a pulse on SO, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.

**3.** If SO is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR}+$) and then will go back to low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought low.

**4.** When the master reset is brought low, the control register and the outputs are cleared. IR goes high and OR goes low. If SI is high when the master reset goes high then the data on the inputs will be written into the memory and IR will return to the low state until SI is brought low. If SI is low when the master reset is ended, the IR will go high, but the data on the inputs will not enter the memory until SI goes high.

## ELECTRICAL CHARACTERISTICS

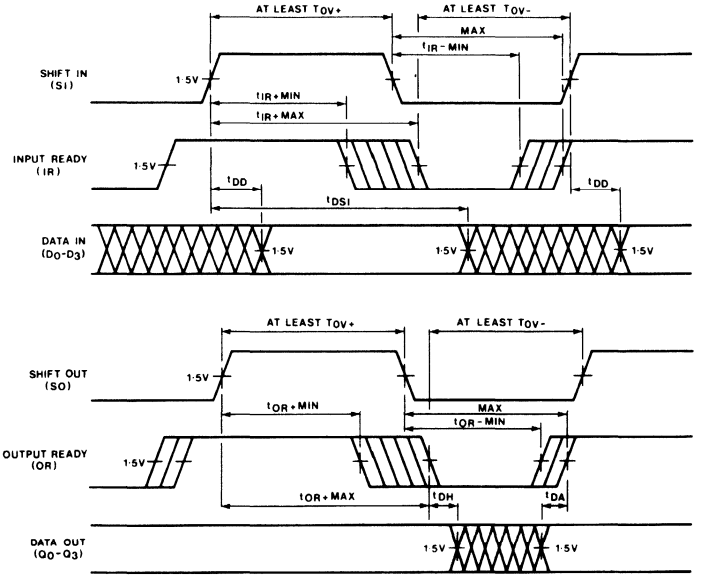
**Test conditions (unless otherwise stated):**
Supply voltage ($V_{CC}$) = +5V ±5%, $T_{amb}$ = 0°C to +70°C Typical Values at $V_{CC}$ = 5V and $T_{amb}$ = +25°C
All voltages with respect to ground

### Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| O/P high voltage | $V_{OH}$ | 2.7 | 3.2 | | V | $I_{OH}$ = -0.2mA |
| O/P low voltage | $V_{OL}$ | | 0.2 | 0.5 | V | $I_{OL}$ = 2mA |
| I/P high level | $V_{IH}$ | 2.5 | | | V | |
| I/P low level | $V_{IL}$ | | | 0.8 | V | |
| I/P leakage current | $I_{IL}$ | -5 | | +10 | μA | $V_{IN}$ = 0V or 5V |
| Supply current | $I_{CC}$ | | 50 | 81 | mA | |

### Switching Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. SI or SO frequency | $f_{MAX}$ | 1.75 | 4.4 | | MHz | |
| Delay, SI high to IR low | $t_{IR}+$ | | 50 | 120 | ns | |
| Delay, SI low to IR high | $t_{IR}-$ | | 80 | 200 | ns | |
| Min. time SI and IR both high | $t_{OV}+$ | | <25 | 45 | ns | |
| Min. time SI and IR both low | $t_{OV}-$ | | <25 | 45 | ns | |
| Data release time | $t_{DSI}$ | | 45 | 110 | ns | |
| Data set-up time | $t_{DD}$ | | 45 | 110 | ns | |
| Delay, SO high to OR low | $t_{OR}+$ | | 80 | 190 | ns | |
| Delay, SO low to OR high | $t_{OR}-$ | | 120 | 290 | ns | |
| Ripple through time | $t_{PT}$ | | 2.5 | 7 | μs | FIFO empty |
| Delay, OR low to data out | $t_{DH}$ | 50 | 85 | | ns | SO = low |
| Min. reset pulse width | $t_{MRW}$ | | 20 | 50 | ns | |
| Delay, data out to OR high | $t_{DA}$ | 0 | 35 | | ns | SO = high |
| Input capacitance | CI | | | 7 | pF | Any pin |




**KEY TO TIMING DIAGRAM**

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DONT CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |

*Fig.3 Timing diagram*

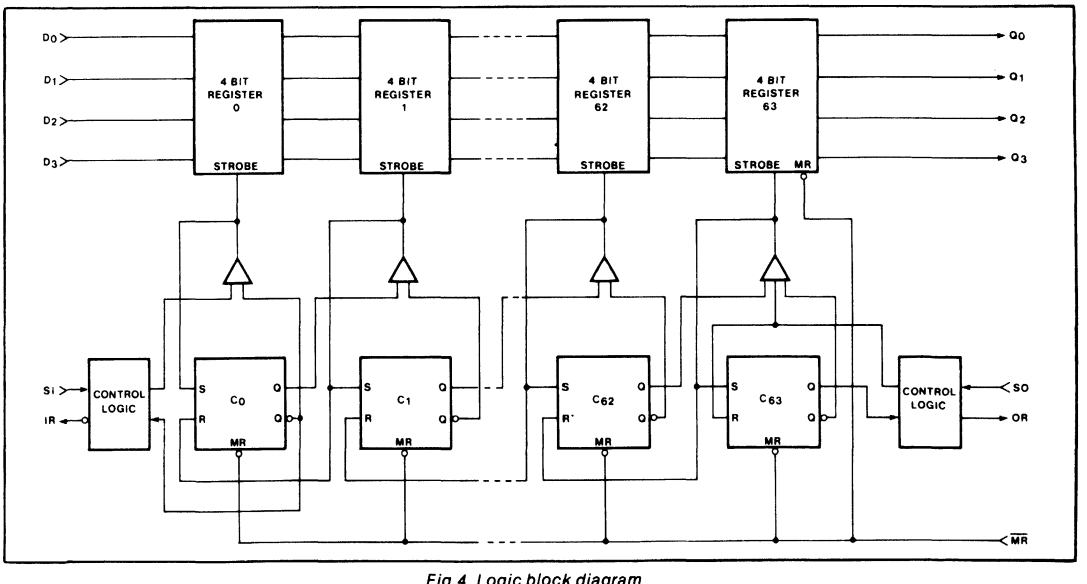



*Fig.4 Logic block diagram*

# MV66030

## 64-WORD x 9-BIT FIRST-IN FIRST-OUT MEMORY

The MV66030 is an asynchronous first-in first-out memory, organised as 64 9-bit words. The device accepts a 9-bit parallel word, D0 - D8, under control of the shift in (SI) input. Multiple devices can be used in parallel to satisfy wider data requirements or can be cascaded to any depth to give more words of storage. Data entered into the FIFO ripples through the device to the outputs Q0 - Q8. Up to 64 words may be entered before any words are read from the memory. The stored words stack up at the output in the order in which they were entered.

Activating the shift out control (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals respectively indicate that the device can accept new data or that the output contains valid data. If the input ready output remains inactive, the device is full. If the output ready signal remains inactive, the device is empty.

Since reading and writing operations are completely independent, the device can be used as a buffer between two digital systems operating asynchronously and with widely differing clock frequencies.

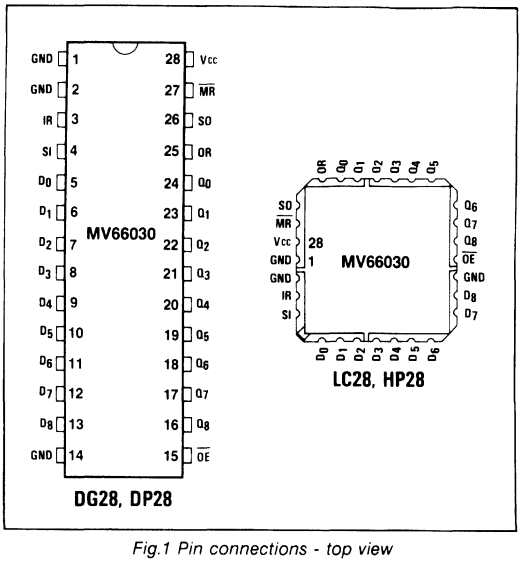



*Fig.1 Pin connections - top view*

### FEATURES

- 25MHz Guaranteed Data Rate when Cascaded (MV66030-25)
- < 200mW at 25MHz
- < 55mW Standby
- Operating Temperature Range:
  -40°C to +85°C Industrial
  -55°C to +125°C Military
- Single 5V Supply, ±10% Tolerance
- Tri-State Outputs

### APPLICATIONS

- Asynchronous Buffer between Digital Systems
- I/O Formatting in DSP Systems
- Video Time Base Correction
- Printer Buffers
- Disk or Tape Interfaces

### ASSOCIATED PRODUCTS

**MV65030** 64 by 9, Tristate 35MHz, Stand-alone FIFO
**MV66401/2/3/4** 64 by 4/5, Bistate/Tristate Cascadable FIFOs
**MV65401/2/3/4** 64 by 4/5, Bistate/Tristate 35MHz Stand-alone FIFOs
**MV61901/2/3** 1K by 9 FIFOs

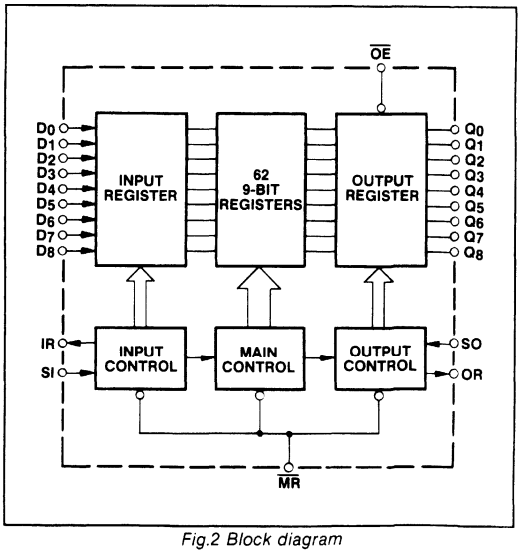



*Fig.2 Block diagram*

## FIFO OPERATION

The MV66030 FIFO contain 64 nine bit data registers. Data is initially loaded from the data inputs D0 - D8 by applying a low to high transition on the shift in (SI) input. IR goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the IR goes high indicating the inputs are available for another data word.

The data falling through the registers stacks up at the output end. A high on OR indicates there is valid data on the data outputs Q0 - Q8. A shift out (SO) can then be used to shift the data out of the FIFO. A low to high transition on SO causes OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the data in the next to last register position moves into the last register position and on to the outputs. If the memory is emptied by reading out all of the data, then, when the last word is being read out and SO goes high, OR will go low as before. When SO next goes low however, there is no data to move into the last location so OR will remain low until more data is entered. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The data word can be extended in width by using more than one FIFO as shown in Fig.10. The status flags must be gated as shown to allow for possible delay variations between devices.

The depth of the FIFO can be extended by tying the data outputs of one device to the data inputs of the next, as shown in Fig.10, the IR input of the receiving device is connected to SO pin of the sending device. Similarly the OR pin of the sending device is connected to the SI pin of the receiving device.

An overriding master reset (MR) is used to reset all control register bits and remove the data from the output (i.e. reset the output to all low).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5V to 7.0V |
| Input voltage $V_{IN}$ (see Note 3) | -0.9V to $V_{CC}$ +0.9V |
| DC voltage applied to output when high impedance | -0.5V to 7.0V |
| Clamp diode current per pin (see Note 2) | +18mA |
| Storage temperature $T_S$ | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -55°C to +125°C |
| Package power dissipation DP | 450mW |
| DG | 1000mW |
| LC | 1000mW |
| HP | 500mW |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage $V_{CC}$ | 5V ± 10% |
| Min. input high level $V_{IH}$ | +2V |
| Max. input low level $V_{IL}$ | +0.8V |
| Ambient temperature | |
| Industrial | -40°C to 85°C |
| Military | -55°C to 125°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Under Recommended operating conditions

### DC Characteristics

| Characteristic | Symbol | INDUSTRIAL | | | | MILITARY | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | MV66030-10 | | MV66030-25 | | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output high level<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = -1mA | $V_{OH}$ | 2.4 | | 2.4 | | | | V | |
| Output low level<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 8mA | $V_{OL}$ | | 0.5 | | 0.5 | | | V | |
| Input leakage<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{IN}$ | -10 | +10 | -10 | +10 | | | μA | |
| Output leakage GND ⩽ $V_{OUT}$ ⩽ $V_{CC}$<br>$V_{CC}$ = $V_{CC}$ max. | $I_{OZ}$ | -50 | +50 | -50 | +50 | | | μA | |
| Short circuit current | $I_{OS}$ | | 80 | | 80 | | | mA | Note 2 |
| Supply current | $I_{CC}$ | | 30 | | 40 | | | mA | $V_{CC}$ = max.<br>$T_{amb}$ = 85°C<br>$I_{LOAD}$ = 0mA |
| Standby current | | | 10 | | 10 | | | mA | $V_{CC}$ = max.<br>$I_{LOAD}$ = 0mA<br>All inputs at $V_{IL}$ |

**AC Characteristics - Using test circuit, except where stated.**

| Characteristic | Symbol | INDUSTRIAL | | | | MILITARY | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | MV66030-10 | | MV66030-25 | | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Maximum operating frequency | $f_O$ | 10 | | 25 | | | | MHz | Note 4 |
| SI HIGH time | $t_{PHSI}$ | 30 | | 15 | | | | ns | +85°C, 4.5V Note 11 |
| SI LOW time | $t_{PLSI}$ | 40 | | 20 | | | | ns | |
| Data setup to SI | $t_{SSI}$ | 0 | | 0 | | | | ns | Note 5 |
| Data hold from SI | $t_{HSI\ (a)}$ | 50 | | 30 | | | | ns | Note 5,6 |
| | $t_{HSI\ (b)}$ | $t_{PHSI}$ +5 | | $t_{PHSI}$ +5 | | | | ns | |
| Delay, SI HIGH to IR LOW | $t_{DLIR}$ | | 30 | | 18 | | | ns | Note 10 |
| Delay, SI LOW to IR HIGH | $t_{DHIR}$ | | 40 | | 22 | | | ns | Note 10 |
| SO HIGH time | $t_{PHSO}$ | 30 | | 12 | | | | ns | +85°C, 4.5V Note 11 |
| SO LOW time | $t_{PLSO}$ | 40 | | 20 | | | | ns | |
| Delay, SO HIGH to OR LOW | $t_{DLOR}$ | | 30 | | 18 | | | ns | Note 10 |
| Delay, SO LOW to OR HIGH | $t_{DHOR}$ | | 40 | | 22 | | | ns | Note 10 |
| Data setup to OR HIGH | $t_{SOR}$ | -20 | | -15 | | | | ns | |
| Data hold from SO LOW | $t_{HSO}$ | 10 | | 8 | | | | ns | |
| IR pulse HIGH | $t_{PIR}$ | 9 | | 6 | | | | ns | -40°C, 5.5V Note 11 |
| OR pulse HIGH | $t_{POR}$ | 10 | | 7 | | | | ns | -40°C, 5.5V Note 11 |
| Data setup to IR | $t_{SIR}$ | 0 | | 0 | | | | ns | Note 8 |
| Data hold from IR | $t_{HIR}$ | 50 | | 30 | | | | ns | Note 8 |
| Bubble through time | $t_{BT}$ | | 2400 | | 1200 | | | ns | |
| $\overline{MR}$ pulse width | $t_{PMR}$ | 60 | | 50 | | | | ns | Note 9 |
| $\overline{MR}$ HIGH to SI HIGH | $t_{DSI}$ | 60 | | 50 | | | | ns | |
| $\overline{MR}$ LOW to OR LOW | $t_{DOR}$ | | 60 | | 50 | | | ns | |
| $\overline{MR}$ LOW to IR HIGH | $t_{DIR}$ | | 60 | | 50 | | | ns | |
| $\overline{MR}$ LOW to output LOW | $t_{LZMR}$ | | 60 | | 50 | | | ns | Note 7 |
| Output valid from $\overline{OE}$ LOW | $t_{OOE}$ | | 60 | | 40 | | | ns | |
| Output HIGH-Z from $\overline{OE}$ HIGH | $t_{HZOE}$ | | 60 | | 40 | | | ns | |

NOTES
4. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$.
5. $t_{SSI}$ and $t_{HSI}$ apply when memory is not full.
6. Hold time is the lesser of the two parameters (a) and (b).
7. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.
8. These times apply when the device is full and SI is held high.
9. For cascade applications, $t_{PMR}$ must be double that specified.
10. Under cascade conditions.
11. Plessey devices are guaranteed to cascade at 25MHz (under typical operating conditions $t_{PHSI}$ = 10ns, $t_{POR}$ = 13ns, $t_{PHSO}$ = 8ns, $t_{PIR}$ = 12ns).

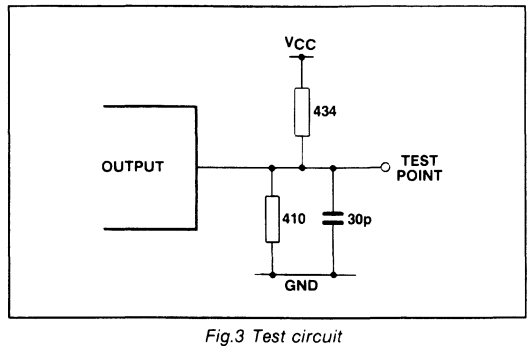



*Fig.3 Test circuit*

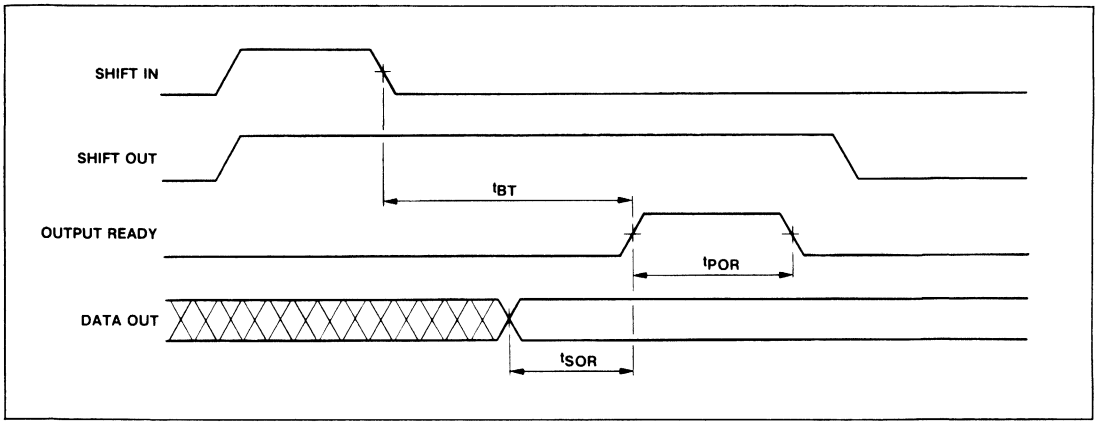



*Fig.7 Data In to Data Out fall through time*

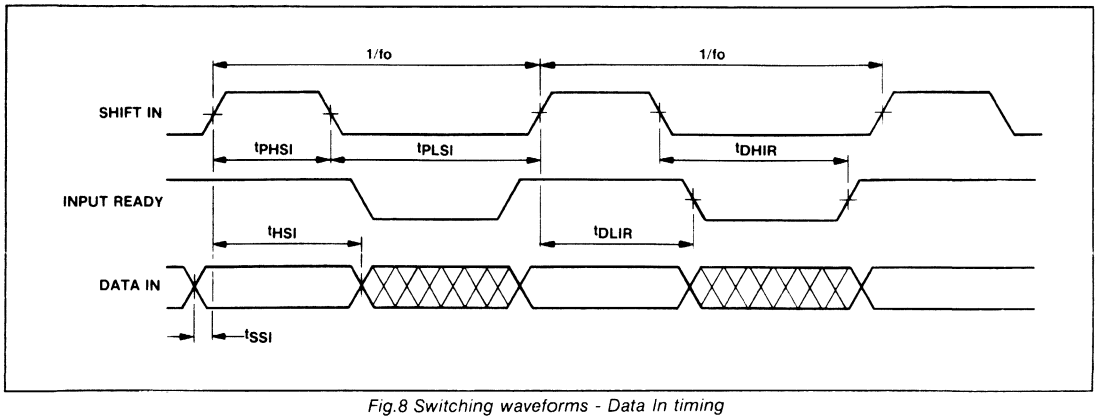



*Fig.8 Switching waveforms - Data In timing*

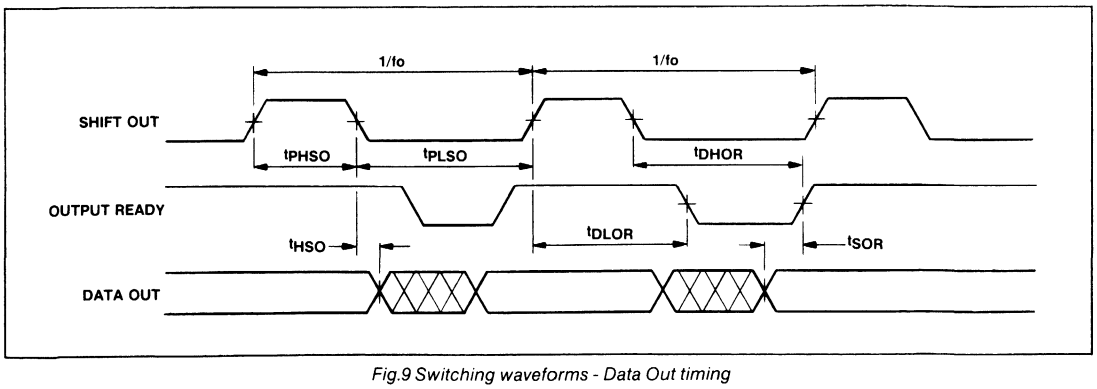



*Fig.9 Switching waveforms - Data Out timing*

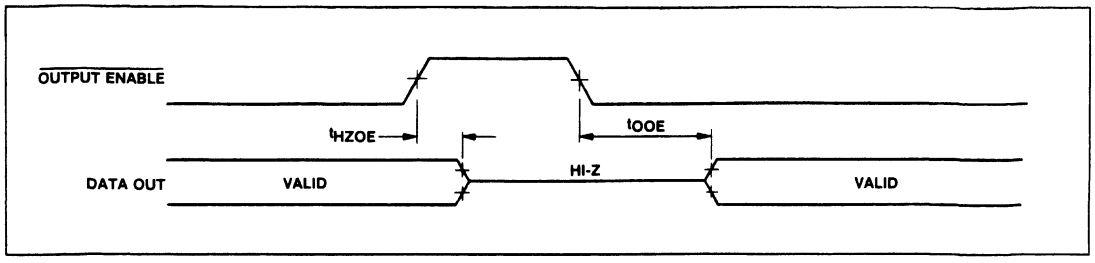



*Fig.4 Output enable timing*

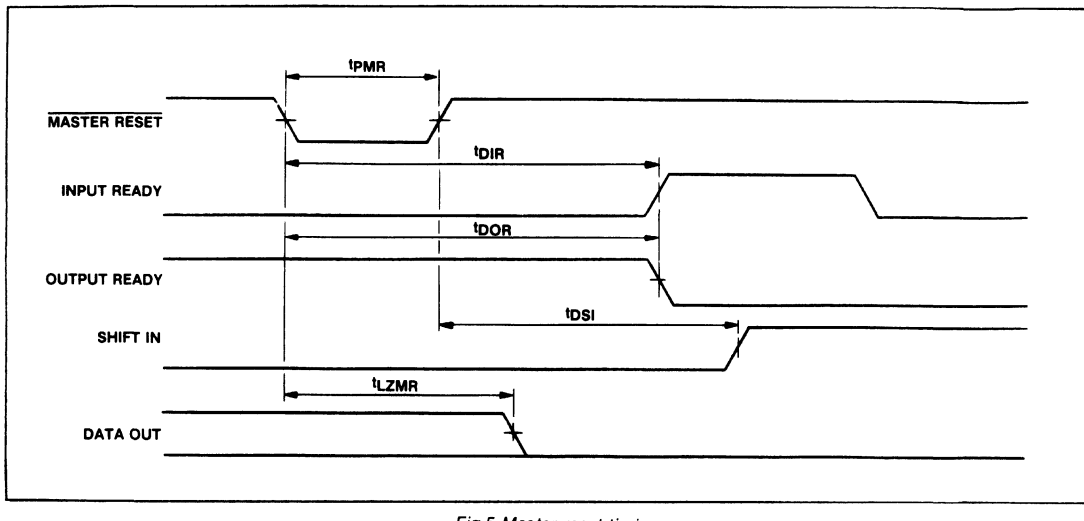



*Fig.5 Master reset timing*

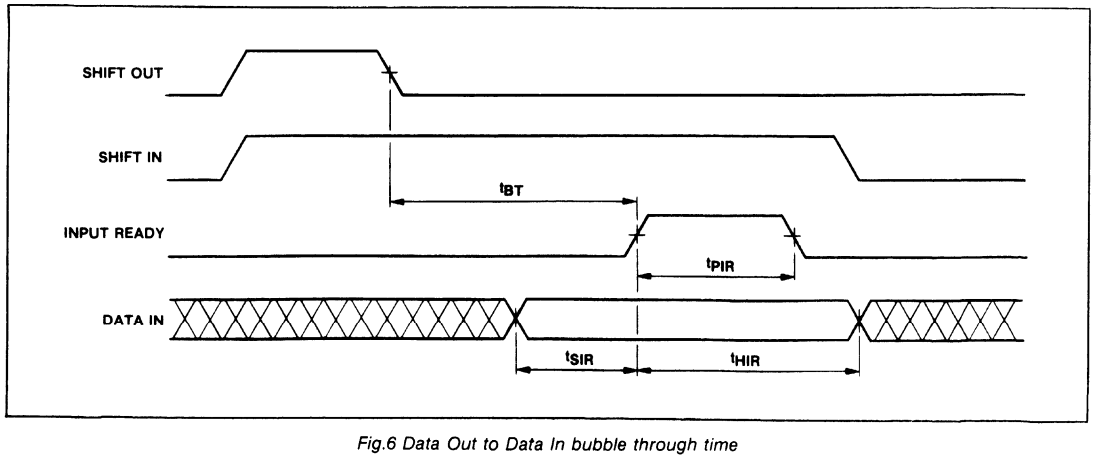



*Fig.6 Data Out to Data In bubble through time*

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.

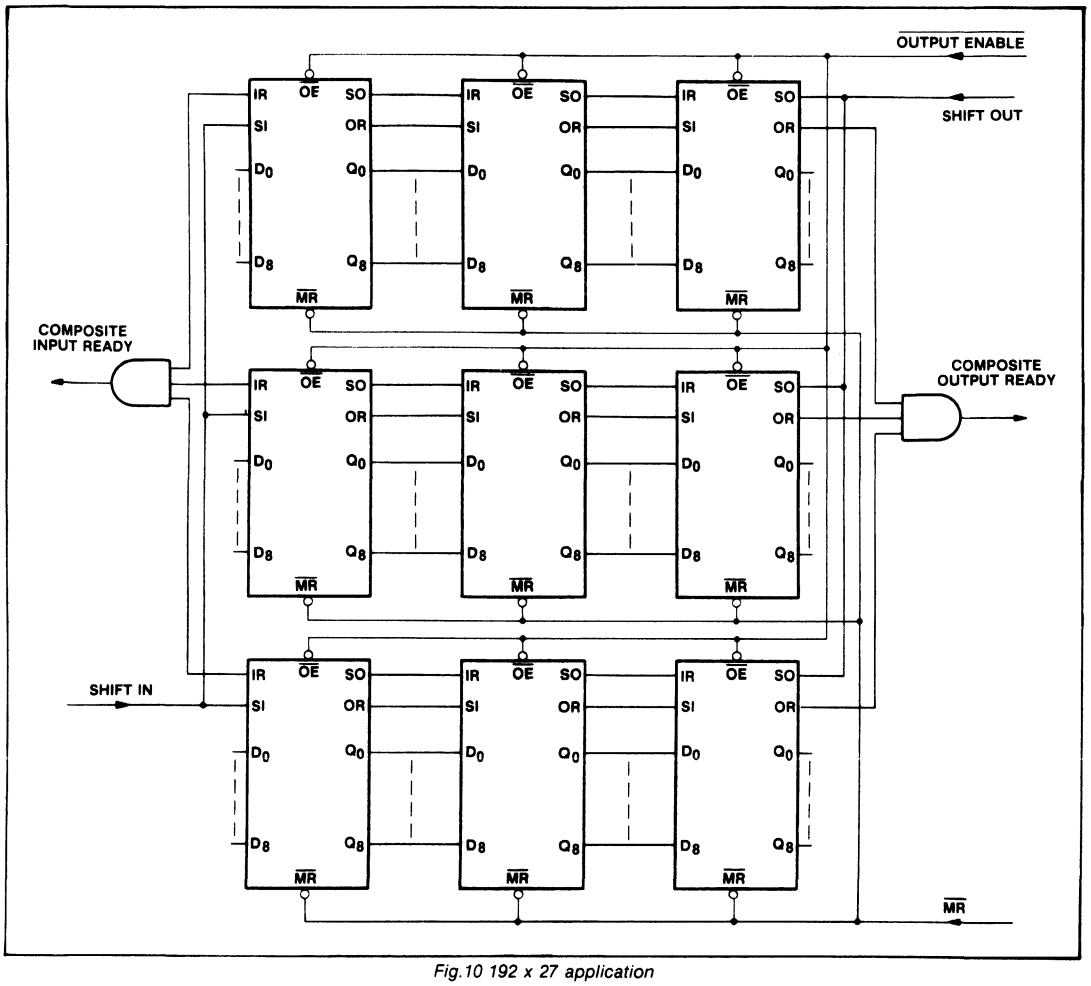



*Fig.10 192 x 27 application*

## USER NOTES

1. When the memory is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle ($t_{POR}$) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All Plessey MV66XXX FIFO's will cascade with other MV66XXX devices, but may not cascade with pin compatible devices from other manufacturers.

## TYPICAL CHARACTERISTICS

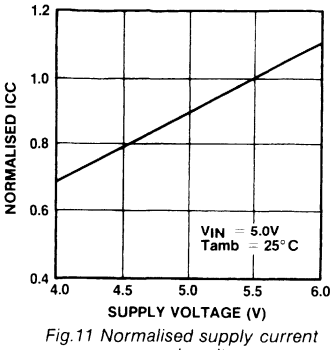



*Fig.11 Normalised supply current vs. supply voltage*

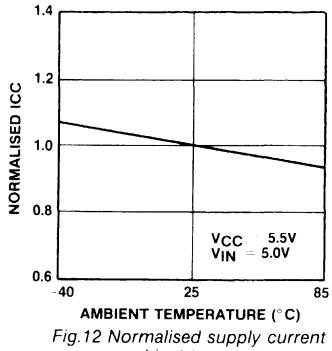



*Fig.12 Normalised supply current vs. ambient temperature*

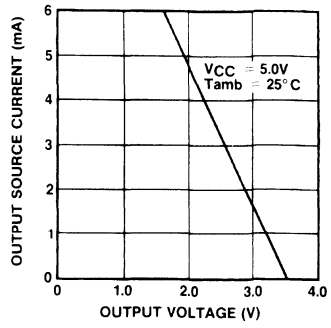



*Fig.13 Output source current vs. output voltage*

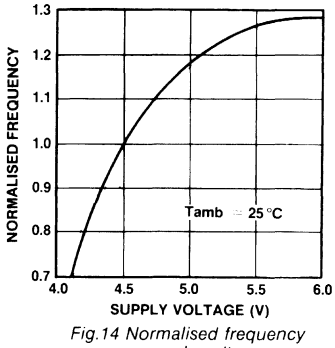



*Fig.14 Normalised frequency vs. supply voltage*

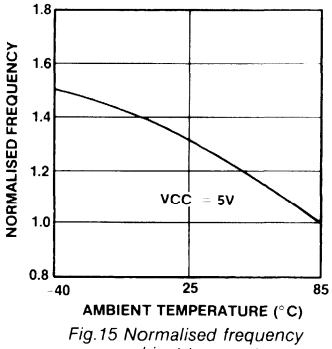



*Fig.15 Normalised frequency vs. ambient temperature*

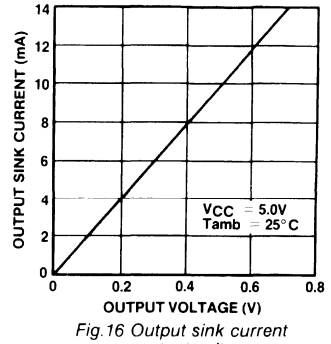



*Fig.16 Output sink current vs. output voltage*

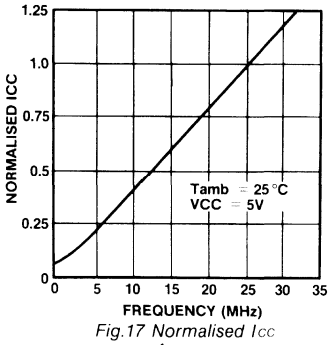



*Fig.17 Normalised Icc vs. frequency*

## ORDERING INFORMATION

**Industrial**

**MV66030-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66030-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66030-10 B0 DP** (Industrial - Plastic DIL package)
**MV66030-25 B0 DP** (Industrial - Plastic DIL package)
**MV66030-10 B0 LC** (Industrial - LCC package)
**MV66030-25 B0 LC** (Industrial - LCC package)
**MV66030-10 B0 HP** (Industrial - Quad package)
**MV66030-25 B0 HP** (Industrial - Quad package)

**Military**

**MV66030 A0 DG** (Military - Ceramic DIL package)
**MV66030 A0 LC** (Military - LCC package)

Call for availability on High Reliability parts and MIL 883C screening.

PLESSEY
Semiconductors

PRELIMINARY INFORMATION

# MV65030

## 64-WORD x 9-BIT FIRST-IN FIRST-OUT MEMORY

*(SUPERSEDES MARCH 1987 EDITION)*

The MV65030 is an asynchronous first-in first-out memory, organised as 64 9-bit words. The device accepts a 9-bit parallel word, D0 - D8, under control of the shift in (SI) input. Multiple devices can be used in parallel to satisfy wider data requirements. Data entered into the FIFO ripples through the device to the outputs Q0 - Q8. Up to 64 words may be entered before any words are read from the memory. The stored words stack up at the output in the order in which they were entered.

Activating the shift out control (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals respectively indicate that the device can accept new data or that the output contains valid data. If the input ready output remains inactive, the device is full. If the output ready signal remains inactive, the device is empty.

Since reading and writing operations are completely independent, the device can be used as a buffer between two digital systems operating asynchronously and with widely differing clock frequencies.

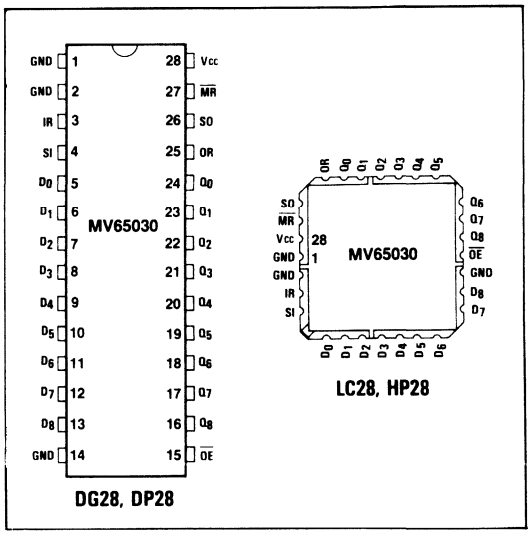



*Fig.1 Pin connections - top view*

- 35MHz Guaranteed Data Rate, 40MHz Typical (MV65030-35)
- < 200mW at 40MHz
- < 55mW Standby
- Operating Temperature Range:
  -40°C to +85°C Industrial
  -55°C to +125°C Military
- Single 5V Supply, ±10% Tolerance
- Tri-State Outputs

### APPLICATIONS

- Asynchronous Buffer between Digital Systems
- I/O Formatting in DSP Systems
- Video Time Base Correction
- Printer Buffers
- Disk or Tape Interfaces

### ASSOCIATED PRODUCTS

**MV65401/2/3/4** 64 by 4/5, Bistate/Tristate Stand-alone FIFOs
**MV66401/2/3/4** 64 by 4/5, Bistate/Tristate Cascadable FIFOs
**MV66030** 64 by 9, Tristate Cascadable FIFO
**MV61901/2/3** 1K by 9 FIFOs

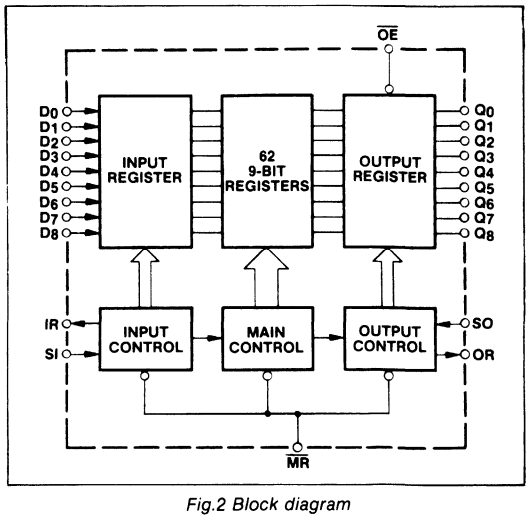



*Fig.2 Block diagram*

## FIFO OPERATION

The MV65030 FIFO contain 64 nine bit data registers. Data is initially loaded from the data inputs D0 - D8 by applying a low to high transition on the shift in (SI) input. IR goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the IR goes high indicating the inputs are available for another data word.

The data falling through the registers stacks up at the output end. A high on OR indicates there is valid data on the data outputs Q0 - Q8. A shift out (SO) can then be used to shift the data out of the FIFO. A low to high transition on SO causes OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the data in the next to last register position moves into the last register position and on to the outputs. If the memory is emptied by reading out all of the data, then, when the last word is being read out and SO goes high, OR will go low as before. When SO next goes low however, there is no data to move into the last location so OR will remain low until more data is entered. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The data word can be extended in width by using more than one FIFO as shown in Fig.10. The status flags must be gated as shown to allow for possible delay variations between devices.

An overriding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the output to all low).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5V to 7.0V |
| Input voltage $V_{IN}$ (see Note 3) | -0.9V to $V_{CC}$ +0.9V |
| DC voltage applied to output when high impedance | -0.5V to 7.0V |
| Clamp diode current per pin (see Note 2) | +18mA |
| Storage temperature $T_S$ | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -55°C to +125°C |
| Package power dissipation DP | 450mW |
| DG | 1000mW |
| LC | 1000mW |
| HP | 500mW |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage $V_{CC}$ | 5V ± 10% |
| Min. input high level $V_{IH}$ | +2V |
| Max. input low level $V_{IL}$ | +0.8V |
| Ambient temperature | |
| Industrial | -40°C to 85°C |
| Military | -55°C to 125°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Under Recommended operating conditions

### DC Characteristics

| Characteristic | Symbol | INDUSTRIAL | | | | MILITARY | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | MV65030-25 | | MV65030-35 | | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output high level<br>$V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OH} = -1mA$ | $V_{OH}$ | 2.4 | | 2.4 | | | | V | |
| Output low level<br>$V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OL} = 8mA$ | $V_{OL}$ | | 0.5 | | 0.5 | | | V | |
| Input leakage<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{IN}$ | -10 | +10 | -10 | +10 | | | μA | |
| Output leakage GND ⩽ $V_{OUT}$ ⩽ $V_{CC}$<br>$V_{CC} = V_{CC}$ max. | $I_{OZ}$ | -50 | +50 | -50 | +50 | | | μA | |
| Short circuit current | $I_{OS}$ | | 80 | | 80 | | | mA | Note 2 |
| Supply current | $I_{CC}$ | | 30 | | 40 | | | mA | $V_{CC}$ = max.<br>$T_{amb}$ = 85°C<br>$I_{LOAD}$ = 0mA |
| Standby current | | | 10 | | 10 | | | | $V_{CC}$ = max.<br>$I_{LOAD}$ = 0mA<br>All inputs at $V_{IL}$ |

## AC Characteristics - Using test circuit

| Characteristic | Symbol | INDUSTRIAL | | | | MILITARY | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | MV65030-25 | | MV65030-35 | | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Maximum operating frequency | $f_O$ | 25 | | 35 | | | | MHz | Note 4 |
| SI HIGH time | $t_{PHSI}$ | 15 | | 10 | | | | ns | |
| SI LOW time | $t_{PLSI}$ | 20 | | 15 | | | | ns | |
| Data setup to SI | $t_{SSI}$ | 0 | | 0 | | | | ns | Note 5 |
| Data hold from SI | $t_{HSI\ (a)}$ | 30 | | 20 | | | | ns | Note 5,6 |
| | $t_{HSI\ (b)}$ | $t_{PHSI\ +5}$ | | $t_{PHSI\ +5}$ | | | | ns | |
| Delay, SI HIGH to IR LOW | $t_{DLIR}$ | | 21 | | 15 | | | ns | |
| Delay, SI LOW to IR HIGH | $t_{DHIR}$ | | 25 | | 18 | | | ns | |
| SO HIGH time | $t_{PHSO}$ | 15 | | 8 | | | | ns | |
| SO LOW time | $t_{PLSO}$ | 20 | | 15 | | | | ns | |
| Delay, SO HIGH to OR LOW | $t_{DLOR}$ | | 21 | | 15 | | | ns | |
| Delay, SO LOW to OR HIGH | $t_{DHOR}$ | | 25 | | 20 | | | ns | |
| Data setup to OR HIGH | $t_{SOR}$ | -15 | | -12 | | | | ns | |
| Data hold from SO LOW | $t_{HSO}$ | 8 | | 5 | | | | ns | |
| Bubble through time | $t_{BT}$ | | 1200 | | 1000 | | | ns | |
| $\overline{MR}$ pulse width | $t_{PMR}$ | 50 | | 30 | | | | ns | |
| $\overline{MR}$ HIGH to SI HIGH | $t_{DSI}$ | 50 | | 30 | | | | ns | |
| $\overline{MR}$ LOW to OR LOW | $t_{DOR}$ | | 50 | | 30 | | | ns | |
| $\overline{MR}$ LOW to IR HIGH | $t_{DIR}$ | | 50 | | 30 | | | ns | |
| $\overline{MR}$ LOW to output LOW | $t_{LZMR}$ | | 50 | | 30 | | | ns | Note 7 |
| Output valid from $\overline{OE}$ LOW | $t_{OOE}$ | | 40 | | 28 | | | ns | |
| Output HIGH-Z from $\overline{OE}$ HIGH | $t_{HZOE}$ | | 40 | | 28 | | | ns | |

NOTES
4. $1/f_O > t_{PHSI} + t_{DHIR}$ $1/f_O > t_{PHSO} + t_{DHOR}$.
5. $t_{SSI}$ and $t_{HSI}$ apply when memory is not full.
6. Hold time is the lesser of the two parameters (a) and (b).
7. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.

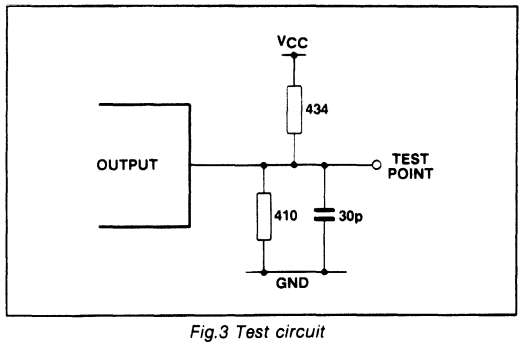



*Fig.3 Test circuit*

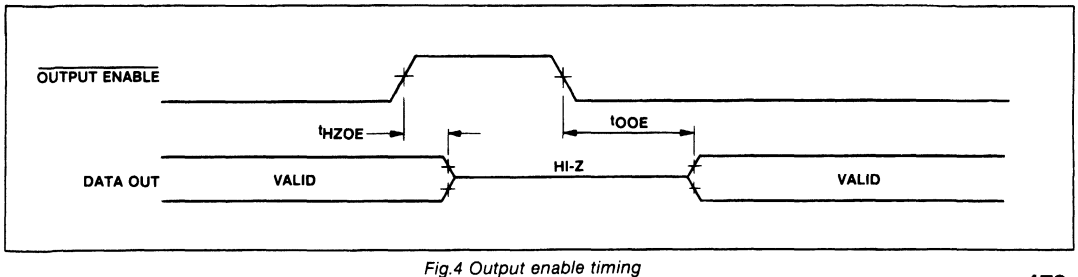



*Fig.4 Output enable timing*

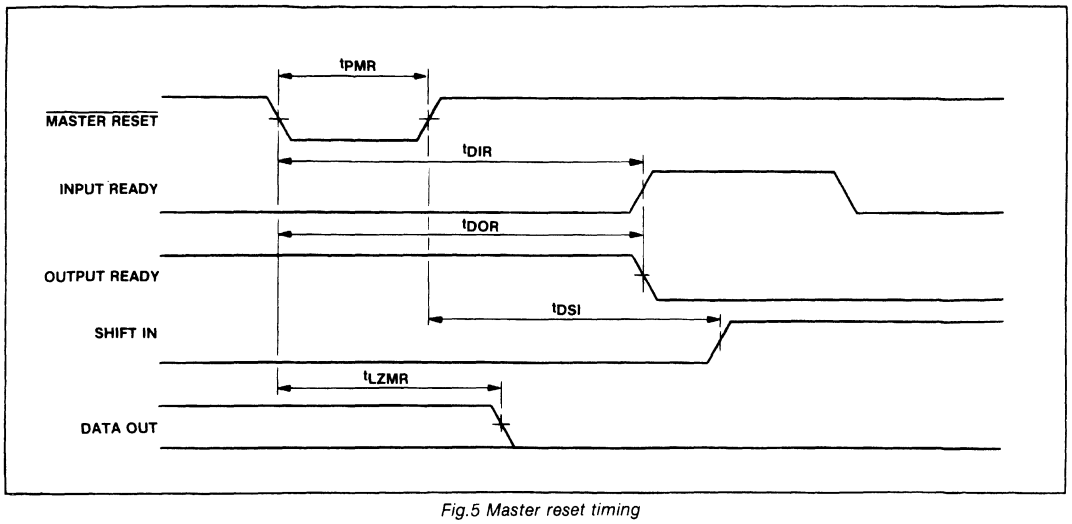



*Fig.5 Master reset timing*

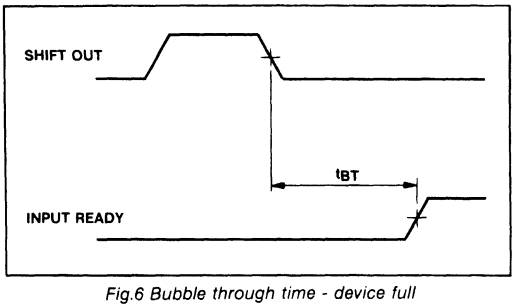



*Fig.6 Bubble through time - device full*

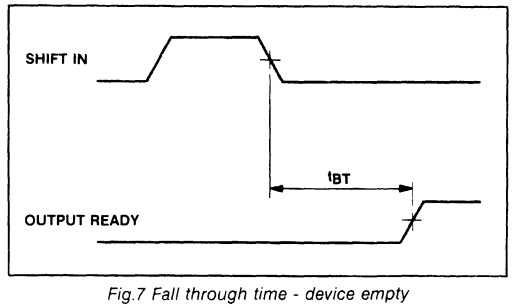



*Fig.7 Fall through time - device empty*

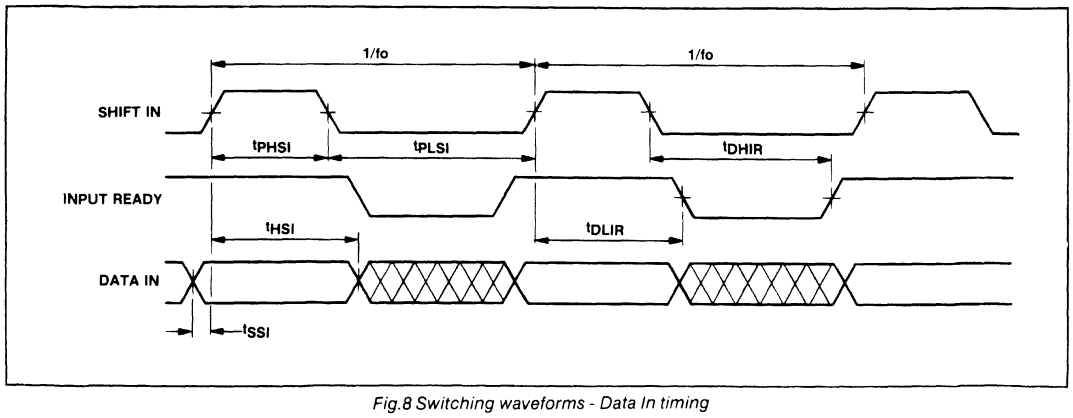



*Fig.8 Switching waveforms - Data In timing*

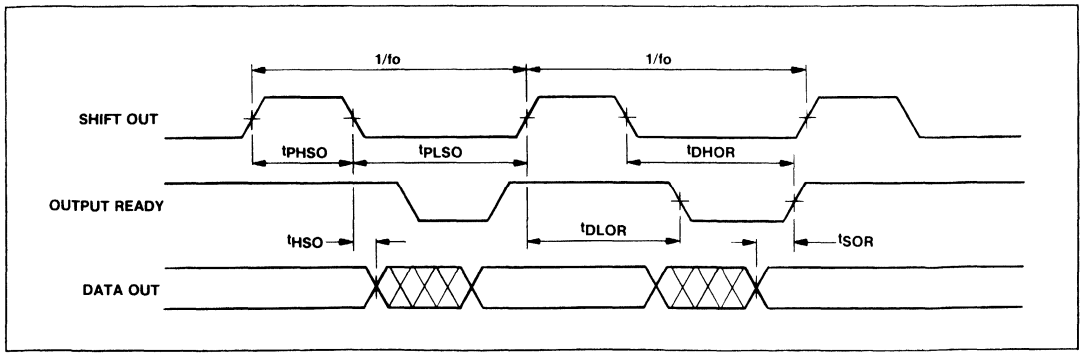



*Fig.9 Switching waveforms - Data Out timing*

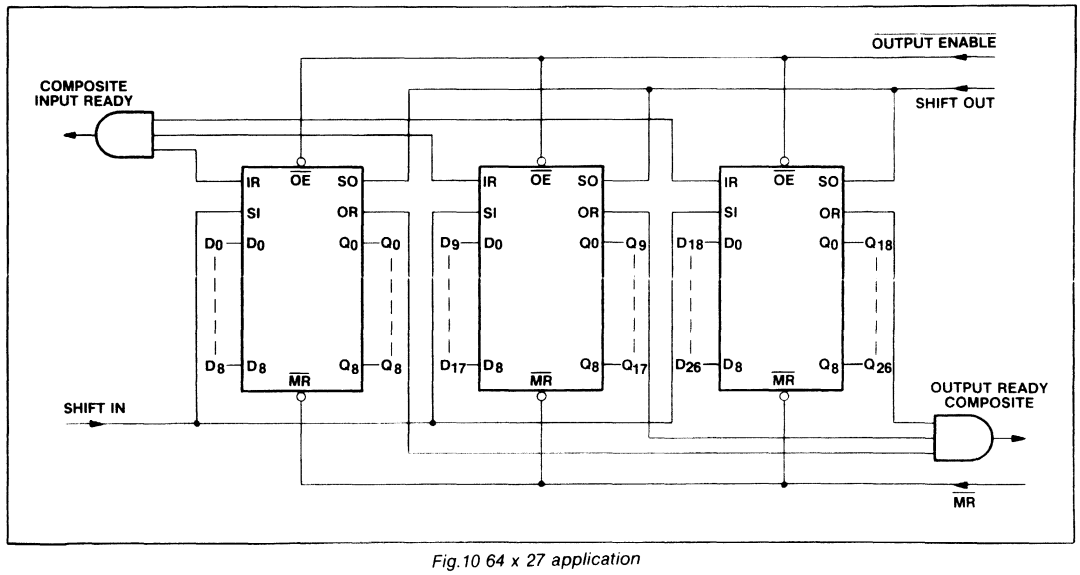



*Fig.10 64 x 27 application*

## USER NOTES

1. When the memory is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.

## TYPICAL CHARACTERISTICS

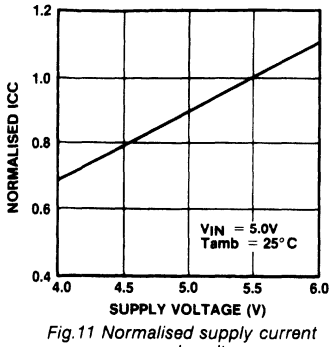



*Fig.11 Normalised supply current vs. supply voltage*

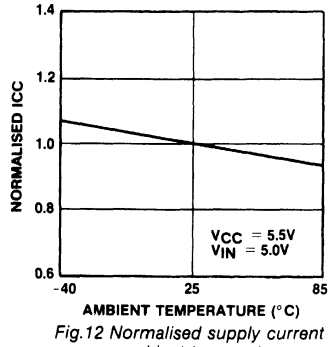



*Fig.12 Normalised supply current vs. ambient temperature*

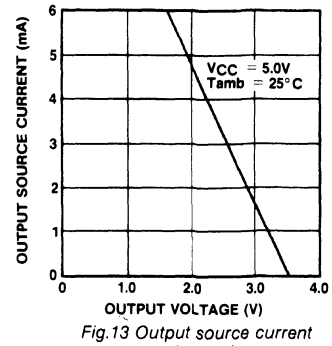



*Fig.13 Output source current vs. output voltage*

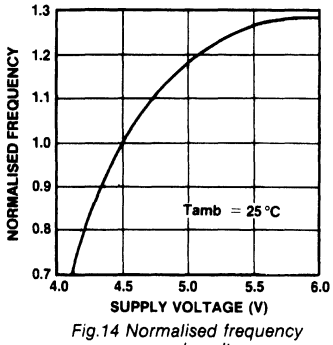



*Fig.14 Normalised frequency vs. supply voltage*

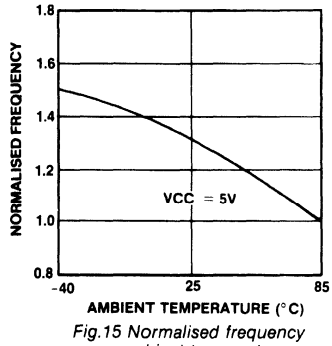



*Fig.15 Normalised frequency vs. ambient temperature*

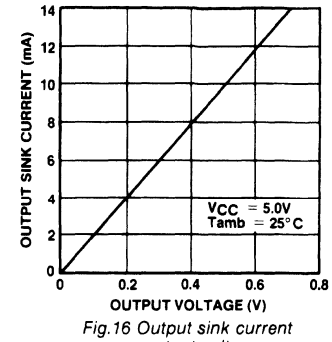



*Fig.16 Output sink current vs. output voltage*

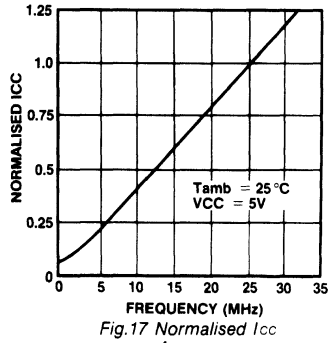



*Fig.17 Normalised Icc vs. frequency*

## ORDERING INFORMATION

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**MV65030-25 B0 DG** (Industrial - Ceramic DIL package)
**MV65030-35 B0 DG** (Industrial - Ceramic DIL package)
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**MV65030-35 B0 DP** (Industrial - Plastic DIL package)
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**MV65030-35 B0 LC** (Industrial - LCC package)
**MV65030-25 B0 HP** (Industrial - Quad package)
**MV65030-35 B0 HP** (Industrial - Quad package)

**Military**

Call for availability on High Reliability parts and MIL 883C screening.

**MV65030 A0 DG** (Military - Ceramic DIL package)
**MV65030 A0 LC** (Military - LCC package)

PLESSEY
Semiconductors

PRELIMINARY INFORMATION

# MV66401/2/3/4

## 64-WORD x 4/5-BIT FIRST-IN FIRST-OUT MEMORIES

The MV66401/2/3/4 are asynchronous first-in first-out memories, organised as 64 by 4 or 5-bit words. Each device accepts a 4/5-bit parallel word, D0 - D4, under control of the shift in (SI) input. Multiple devices can be used to satisfy wider data requirements. Data entered into the FIFO ripples through the device to the outputs Q0 - Q4. Up to 64 words may be entered before any words are read from the memory. The stored words stack up at the output in the order in which they were entered.

Activating the shift out control (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals respectively indicate that the device can accept new data or that the output contains valid data. If the input ready output remains inactive, the device is full. If the output ready signal remains inactive, the device is empty.

Since reading and writing operations are completely independent, the device can be used as a buffer between two digital systems operating asynchronously and with widely differing clock frequencies.

The MV66401/2 are respectively four and five bit devices with TTL compatible outputs. The MV66403/4 have the additional feature of tri-state outputs.

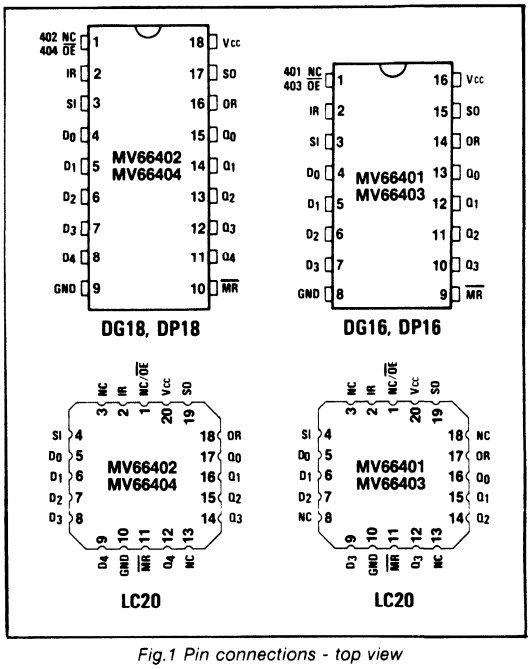



*Fig.1 Pin connections - top view*

- 25MHz Guaranteed Data Rate when Cascaded (MV66401/2/3/4-25)
- < 200mW at 25MHz
- < 55mW Standby
- Operating Temperature Range:
  -40°C to +85°C Industrial
  -55°C to +125°C Military
- Single 5V Supply, ±10% Tolerance
- Tri-State Outputs on the MV66403/4

### APPLICATIONS

- Asynchronous Buffer between Digital Systems
- I/O Formatting in DSP Systems
- Video Time Base Correction
- Printer Buffers
- Disk or Tape Interfaces

### ASSOCIATED PRODUCTS

**MV65401/2/3/4** 64 by 4/5, Bistate/Tristate Stand-alone FIFOs
**MV66030** 64 by 9, Tristate Cascadable FIFO
**MV65030** 64 by 9, Tristate Stand-alone FIFO
**MV61901/2/3** 1K by 9 FIFOs

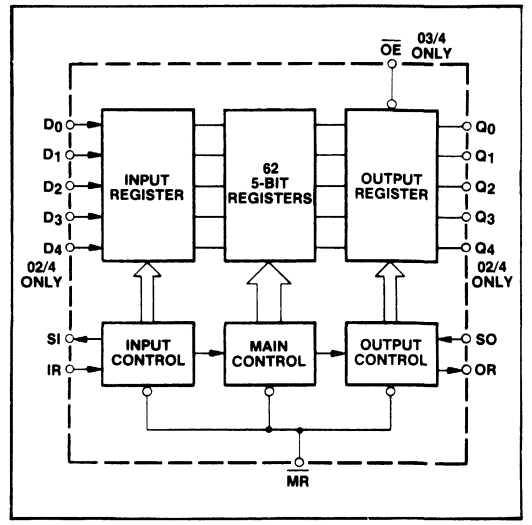



*Fig.2 Block diagram*

## FIFO OPERATION

The MV66401/2/3/4 FIFOs contain 64 four or five bit data registers. Data is initially loaded from the data inputs D0 - D4 by applying a low to high transition on the shift in (SI) input. IR goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the IR goes high indicating the inputs are available for another data word.

The data falling through the registers stacks up at the output end. A high on OR indicates there is valid data on the data outputs Q0 - Q4. A shift out (SO) can then be used to shift the data out of the FIFO. A low to high transition on SO causes OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the data in the next to last register position moves into the last register position and on to the outputs. If the memory is emptied by reading out all of the data, then, when the last word is being read out and SO goes high, OR will go low as before. When SO next goes low however, there is no data to move into the last location so OR will remain low until more data is entered. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The data word can be extended in width by using more than one FIFO as shown in Fig.10. The status flags must be gated as shown to allow for possible delay variations between devices.

The depth of the FIFO can be extended by tying the data outputs of one device to the data inputs of the next, as shown in Fig.11. The IR input of the receiving device is connected to the SO pin of the sending device. Similarly the OR pin of the sending device is connected to the SI pin of the receiving device.

An overriding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the output to all low).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5V to 7.0V |
| Input voltage $V_{IN}$ (see Note 3) | -0.9V to $V_{CC}$ +0.9V |
| DC voltage applied to output when high impedance | -0.5V to 7.0V |
| Clamp diode current per pin (see Note 2) | +18mA |
| Storage temperature $T_S$ | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -55°C to +125°C |
| Package power dissipation DP | 450mW |
| DG | 1000mW |
| LC | 1000mW |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage $V_{CC}$ | 5V ± 10% |
| Min. input high level $V_{IH}$ | +2V |
| Max. input low level $V_{IL}$ | +0.8V |
| Ambient temperature | |
| Industrial | -40°C to 85°C |
| Military | -55°C to 125°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Under Recommended operating conditions

**DC Characteristics**

| Characteristic | Symbol | INDUSTRIAL | | | | MILITARY | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | MV6640X-10 | | MV6640X-25 | | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output high level<br>$V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OH} = -1mA$ | $V_{OH}$ | 2.4 | | 2.4 | | | | V | |
| Output low level<br>$V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OL} = 8mA$ | $V_{OL}$ | | 0.5 | | 0.5 | | | V | |
| Input leakage<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{IN}$ | -10 | +10 | -10 | +10 | | | μA | |
| Output leakage GND ≤ $V_{OUT}$ ≤ $V_{CC}$<br>$V_{CC} = V_{CC}$ max. | $I_{OZ}$ | -50 | +50 | -50 | +50 | | | μA | |
| Short circuit current | $I_{OS}$ | | 80 | | 80 | | | mA | Note 2 |
| Supply current | $I_{CC}$ | | 30 | | 40 | | | mA | $V_{CC}$ = max.<br>$T_{amb}$ = 85°C<br>$I_{LOAD}$ = 0mA |
| Standby current | | | 10 | | 10 | | | mA | $V_{CC}$ = max.<br>$I_{LOAD}$ = 0mA<br>All inputs at $V_{IL}$ |

**AC Characteristics - Using test circuit, except where stated.**

| Characteristic | Symbol | INDUSTRIAL | | | | MILITARY | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | MV6640X-10 | | MV6640X-25 | | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Maximum operating frequency | $f_O$ | 10 | | 25 | | | | MHz | Note 4 |
| SI HIGH time | $t_{PHSI}$ | 30 | | 15 | | | | ns | +85°C, 4.5V Note 11 |
| SI LOW time | $t_{PLSI}$ | 40 | | 20 | | | | ns | |
| Data setup to SI | $t_{SSI}$ | 0 | | 0 | | | | ns | Note 5 |
| Data hold from SI | $t_{HSI\ (a)}$ | 50 | | 30 | | | | ns | Note 5,6 |
| | $t_{HSI\ (b)}$ | $t_{PHSI} - 5$ | | $t_{PHSI} - 5$ | | | | ns | |
| Delay, SI HIGH to IR LOW | $t_{DLIR}$ | | 30 | | 18 | | | ns | Note 10 |
| Delay, SI LOW to IR HIGH | $t_{DHIR}$ | | 40 | | 22 | | | ns | Note 10 |
| SO HIGH time | $t_{PHSO}$ | 30 | | 12 | | | | ns | +85°C, 4.5V Note 11 |
| SO LOW time | $t_{PLSO}$ | 40 | | 20 | | | | ns | |
| Delay, SO HIGH to OR LOW | $t_{DLOR}$ | | 30 | | 18 | | | ns | Note 10 |
| Delay, SO LOW to OR HIGH | $t_{DHOR}$ | | 40 | | 22 | | | ns | Note 10 |
| Data setup to OR HIGH | $t_{SOR}$ | -20 | | -15 | | | | ns | |
| Data hold from SO LOW | $t_{HSO}$ | 10 | | 8 | | | | ns | |
| IR pulse HIGH | $t_{PIR}$ | 9 | | 6 | | | | ns | -40°C, 5.5V Note 11 |
| OR pulse HIGH | $t_{POR}$ | 10 | | 7 | | | | ns | -40°C, 5.5V Note 11 |
| Data setup to IR | $t_{SIR}$ | 0 | | 0 | | | | ns | Note 8 |
| Data hold from IR | $t_{HIR}$ | 50 | | 30 | | | | ns | Note 8 |
| Bubble through time | $t_{BT}$ | | 2400 | | 1200 | | | ns | |
| $\overline{MR}$ pulse width | $t_{PMR}$ | 60 | | 50 | | | | ns | Note 9 |
| $\overline{MR}$ HIGH to SI HIGH | $t_{DSI}$ | 60 | | 50 | | | | ns | |
| $\overline{MR}$ LOW to OR LOW | $t_{DOR}$ | | 60 | | 50 | | | ns | |
| $\overline{MR}$ LOW to IR HIGH | $t_{DIR}$ | | 60 | | 50 | | | ns | |
| $\overline{MR}$ LOW to output LOW | $t_{LZMR}$ | | 60 | | 50 | | | ns | Note 7 |
| Output valid from $\overline{OE}$ LOW | $t_{OOE}$ | | 60 | | 40 | | | ns | |
| Output HIGH-Z from $\overline{OE}$ HIGH | $t_{HZOE}$ | | 60 | | 40 | | | ns | |

NOTES
4. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$.
5. $t_{SSI}$ and $t_{HSI}$ apply when memory is not full.
6. Hold time is the lesser of the two parameters (a) and (b).
7. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.
8. These times apply when the device is full and SI is held high.
9. For cascade applications, $t_{PMR}$ must be double that specified.
10. Under cascade conditions.
11. Plessey devices are guaranteed to cascade at 25MHz (under typical operating conditions $t_{PHSI}$ = 10ns, $t_{POR}$ = 13ns, $t_{PHSO}$ = 8ns, $t_{PIR}$ = 12ns).

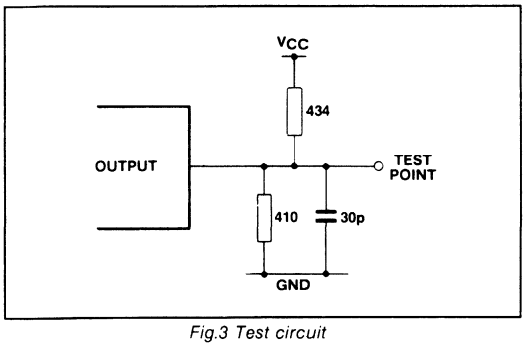



*Fig.3 Test circuit*

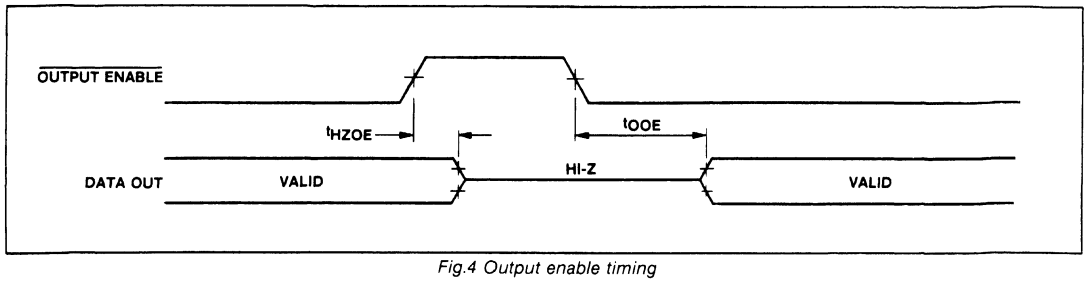



*Fig.4 Output enable timing*

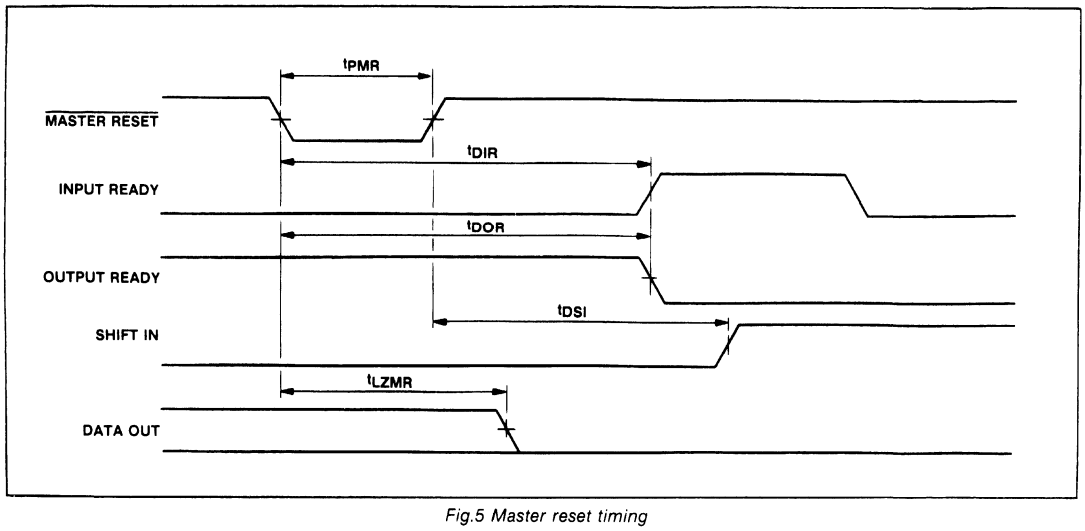



*Fig.5 Master reset timing*

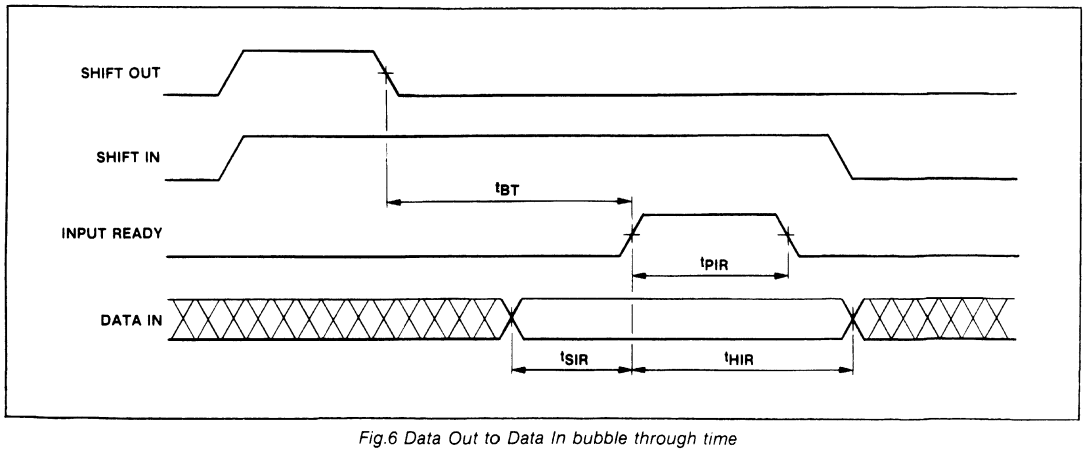



*Fig.6 Data Out to Data In bubble through time*

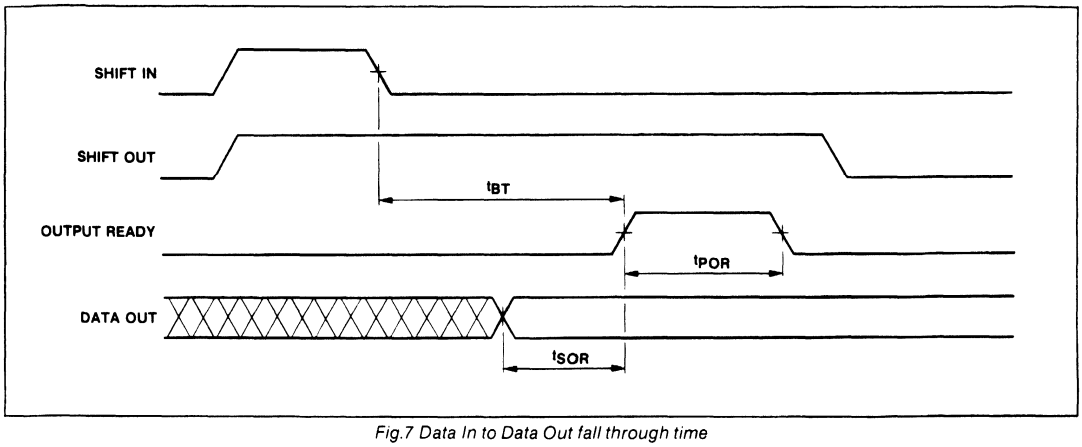



*Fig.7 Data In to Data Out fall through time*

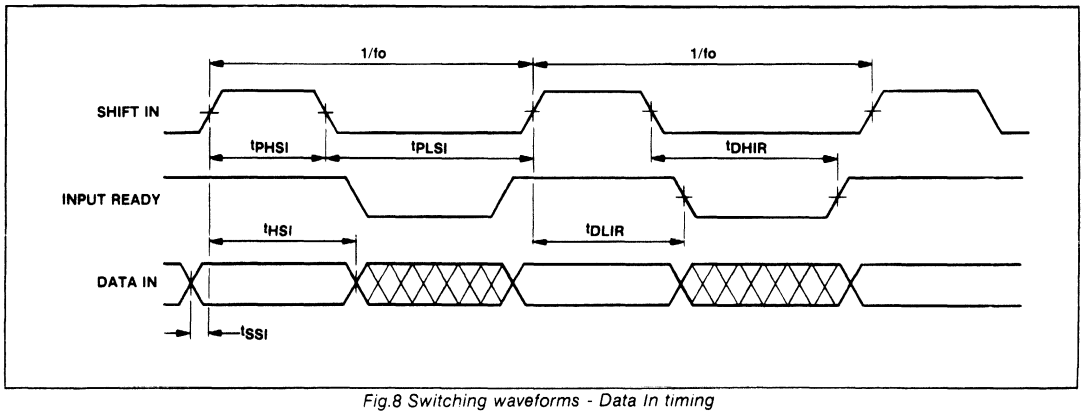



*Fig.8 Switching waveforms - Data In timing*

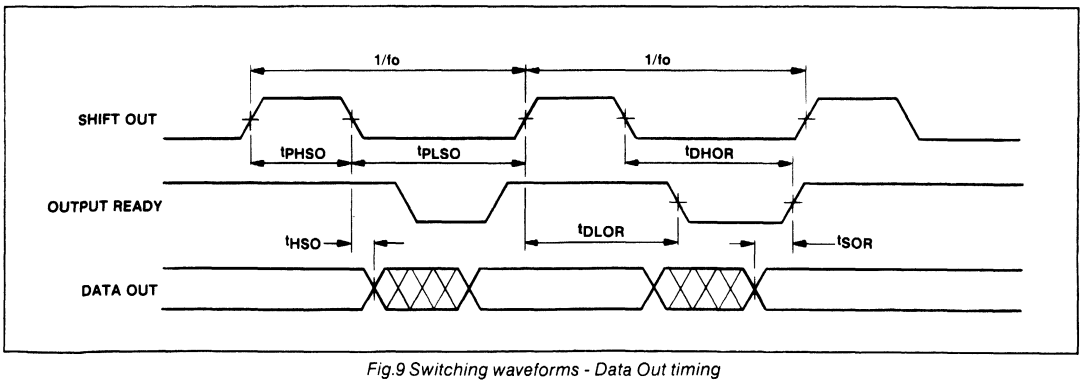



*Fig.9 Switching waveforms - Data Out timing*

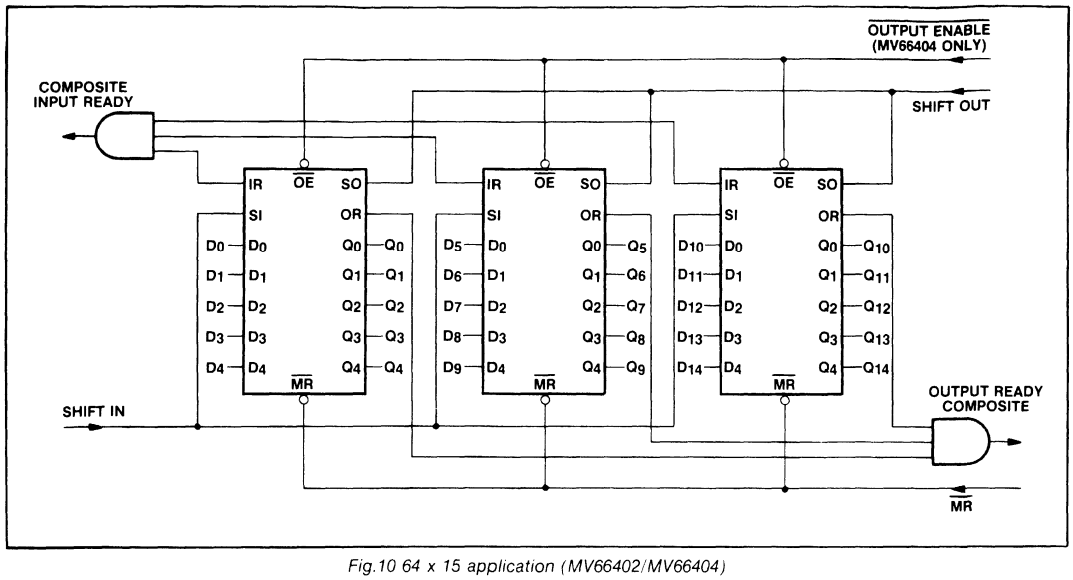



*Fig.10 64 x 15 application (MV66402/MV66404)*

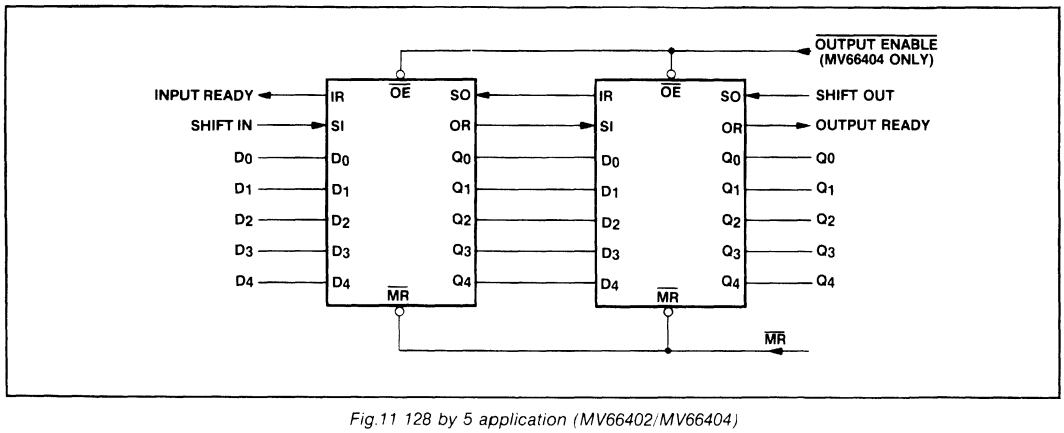



*Fig.11 128 by 5 application (MV66402/MV66404)*

## USER NOTES

1. When the memory is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle ($t_{POR}$) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All Plessey MV66XXX FIFO's will cascade with other MV66XXX devices, but may not cascade with pin compatible devices from other manufacturers.

## TYPICAL CHARACTERISTICS

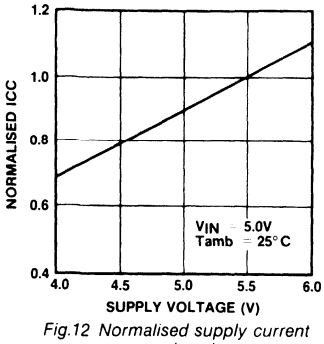



*Fig.12 Normalised supply current vs. supply voltage*

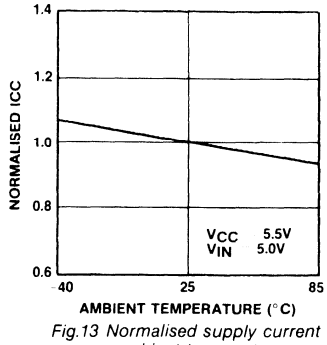



*Fig.13 Normalised supply current vs. ambient temperature*

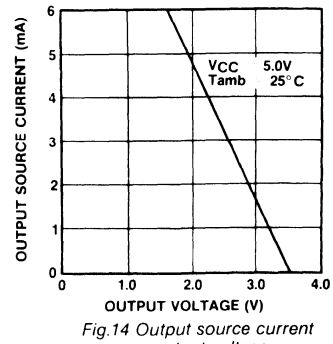



*Fig.14 Output source current vs. output voltage*

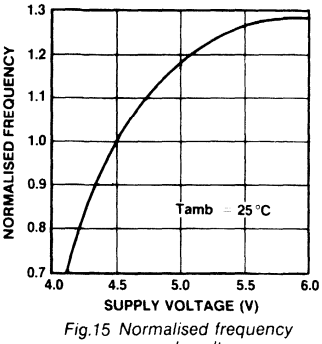



*Fig.15 Normalised frequency vs. supply voltage*

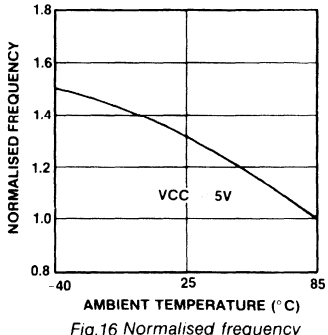



*Fig.16 Normalised frequency vs. ambient temperature*

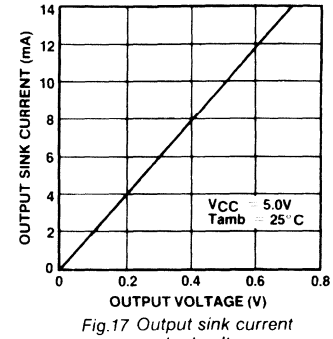



*Fig.17 Output sink current vs. output voltage*

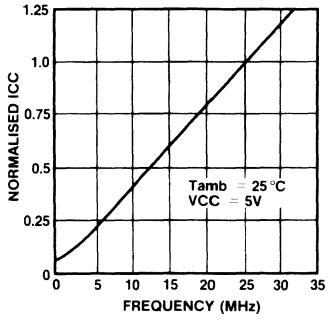



*Fig.18 Normalised Icc vs. frequency*

## ORDERING INFORMATION

**Industrial**

**MV66401-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66401-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66402-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66402-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66403-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66403-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66404-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66404-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66401-10 B0 DP** (Industrial - Plastic DIL package)
**MV66401-25 B0 DP** (Industrial - Plastic DIL package)
**MV66402-10 B0 DP** (Industrial - Plastic DIL package)
**MV66402-25 B0 DP** (Industrial - Plastic DIL package)
**MV66403-10 B0 DP** (Industrial - Plastic DIL package)
**MV66403-25 B0 DP** (Industrial - Plastic DIL package)
**MV66404-10 B0 DP** (Industrial - Plastic DIL package)
**MV66404-25 B0 DP** (Industrial - Plastic DIL package)
**MV66401-10 B0 LC** (Industrial - LCC package)
**MV66401-25 B0 LC** (Industrial - LCC package)
**MV66402-10 B0 LC** (Industrial - LCC package)
**MV66402-25 B0 LC** (Industrial - LCC package)
**MV66403-10 B0 LC** (Industrial - LCC package)
**MV66403-25 B0 LC** (Industrial - LCC package)
**MV66404-10 B0 LC** (Industrial - LCC package)
**MV66404-25 B0 LC** (Industrial - LCC package)

**Military**

**MV66401 A0 DG** (Military - Ceramic DIL package)
**MV66402 A0 DG** (Military - Ceramic DIL package)
**MV66403 A0 DG** (Military - Ceramic DIL package)
**MV66404 A0 DG** (Military - Ceramic DIL package)
**MV66401 A0 LC** (Military - LCC package)
**MV66402 A0 LC** (Military - LCC package)
**MV66403 A0 LC** (Military - LCC package)
**MV66404 A0 LC** (Military - LCC package)

Call for availability on High Reliability parts and MIL 883C screening.

# MV65401/2/3/4

## 64-WORD x 4/5-BIT FIRST-IN FIRST-OUT MEMORIES

*(SUPERSEDES MARCH 1987 EDITION)*

The MV65401/2/3/4 are asynchronous first-in first-out memories, organised as 64 by 4 or 5-bit words. Each device accepts a 4/5-bit parallel word, D0 - D4, under control of the shift in (SI) input. Multiple devices can be used to satisfy wider data requirements. Data entered into the FIFO ripples through the device to the outputs Q0 - Q4. Up to 64 words may be entered before any words are read from the memory. The stored words stack up at the output in the order in which they were entered.

Activating the shift out control (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals respectively indicate that the device can accept new data or that the output contains valid data. If the input ready output remains inactive, the device is full. If the output ready signal remains inactive, the device is empty.

Since reading and writing operations are completely independent, the device can be used as a buffer between two digital systems operating asynchronously and with widely differing clock frequencies.

The MV65401/2 are respectively four and five bit devices with TTL compatible outputs. The MV65403/4 have the additional feature of tri-state outputs.

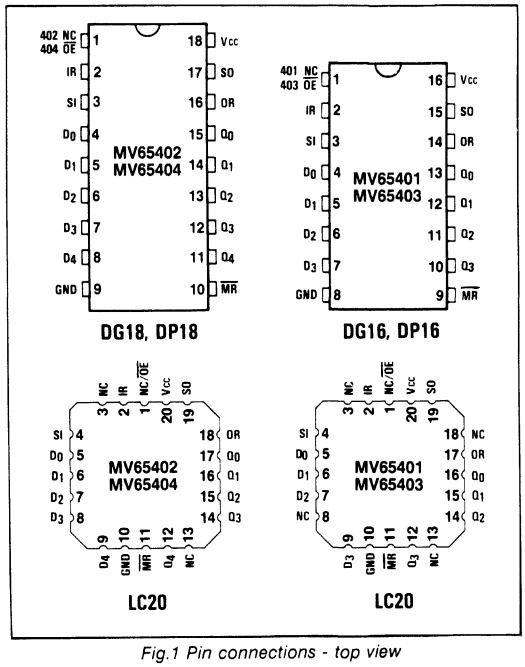



*Fig.1 Pin connections - top view*

- 35MHz Guaranteed Data Rate, 40MHz Typical (MV65401/2/3/4-35)
- < 200mW at 40MHz
- < 55mW Standby
- Operating Temperature Range:
  -40°C to +85°C Industrial
  -55°C to +125°C Military
- Single 5V Supply, ±10% Tolerance
- Tri-State Outputs on the MV65403/4

### APPLICATIONS

- Asynchronous Buffer between Digital Systems
- I/O Formatting in DSP Systems
- Video Time Base Correction
- Printer Buffers
- Disk or Tape Interfaces

### ASSOCIATED PRODUCTS

**MV66401/2/3/4** 64 by 4/5, Bistate/Tristate Cascadable FIFOs
**MV66030** 64 by 9, Tristate Cascadable FIFO
**MV65030** 64 by 9, Tristate Stand-alone FIFO
**MV61901/2/3** 1K by 9 FIFOs

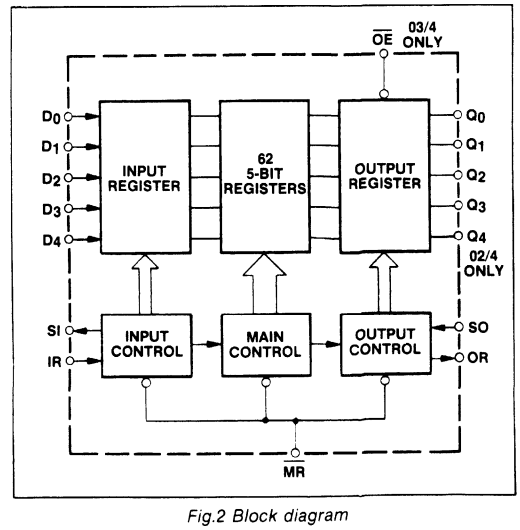



*Fig.2 Block diagram*

## FIFO OPERATION

The MV65401/2/3/4 FIFOs contain 64 four or five bit data registers. Data is initially loaded from the data inputs D0 - D4 by applying a low to high transition on the shift in (SI) input. IR goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the IR goes high indicating the inputs are available for another data word.

The data falling through the registers stacks up at the output end. A high on OR indicates there is valid data on the data outputs Q0 - Q4. A shift out (SO) can then be used to shift the data out of the FIFO. A low to high transition on SO causes OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the data in the next to last register position moves into the last register position and on to the outputs. If the memory is emptied by reading out all of the data, then, when the last word is being read out and SO goes high, OR will go low as before. When SO next goes low however, there is no data to move into the last location so OR will remain low until more data is entered. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The data word can be extended in width by using more than one FIFO as shown in Fig.10. The status flags must be gated as shown to allow for possible delay variations between devices.

An overriding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the output to all low).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5V to 7.0V |
| Input voltage $V_{IN}$ (see Note 3) | -0.9V to $V_{CC}$ +0.9V |
| DC voltage applied to output when high impedance | -0.5V to 7.0V |
| Clamp diode current per pin (see Note 2) | +18mA |
| Storage temperature $T_S$ | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -55°C to +125°C |
| Package power dissipation DP | 450mW |
| DG | 1000mW |
| LC | 1000mW |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operaton under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage $V_{CC}$ | 5V ± 10% |
| Min. input high level $V_{IH}$ | +2V |
| Max. input low level $V_{IL}$ | +0.8V |
| Ambient temperature | |
| Industrial | -40°C to 85°C |
| Military | -55°C to 125°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Under Recommended operating conditions

### DC Characteristics

| Characteristic | Symbol | INDUSTRIAL | | | | MILITARY | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | MV6540X-25 | | MV6540X-35 | | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output high level<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = -1mA | $V_{OH}$ | 2.4 | | 2.4 | | | | V | |
| Output low level<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 8mA | $V_{OL}$ | | 0.5 | | 0.5 | | | V | |
| Input leakage<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{IN}$ | -10 | +10 | -10 | +10 | | | μA | |
| Output leakage GND ⩽ $V_{OUT}$ ⩽ $V_{CC}$<br>$V_{CC}$ = $V_{CC}$ max. | $I_{OZ}$ | -50 | +50 | -50 | +50 | | | μA | |
| Short circuit current | $I_{OS}$ | | 80 | | 80 | | | mA | Note 2 |
| Supply current | $I_{CC}$ | | 30 | | 40 | | | mA | $V_{CC}$ = max.<br>$T_{amb}$ = 85°C<br>$I_{LOAD}$ = 0mA |
| Standby current | | | 10 | | 10 | | | mA | $V_{CC}$ = max.<br>$I_{LOAD}$ = 0mA<br>All inputs at $V_{IL}$ |

## AC Characteristics - Using test circuit

| Characteristic | Symbol | INDUSTRIAL | | | | MILITARY | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | MV6540X-25 | | MV6540X-35 | | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Maximum operating frequency | $f_O$ | 25 | | 35 | | | | MHz | Note 4 |
| SI HIGH time | $t_{PHSI}$ | 15 | | 10 | | | | ns | |
| SI LOW time | $t_{PLSI}$ | 20 | | 15 | | | | ns | |
| Data setup to SI | $t_{SSI}$ | 0 | | 0 | | | | ns | Note 5 |
| Data hold from SI | $t_{HSI\ (a)}$ | 30 | | 20 | | | | ns | Note 5,6 |
| | $t_{HSI\ (b)}$ | $t_{PHSI}$ +5 | | $t_{PHSI}$ +5 | | | | ns | |
| Delay, SI HIGH to IR LOW | $t_{DLIR}$ | | 21 | | 15 | | | ns | |
| Delay, SI LOW to IR HIGH | $t_{DHIR}$ | | 25 | | 18 | | | ns | |
| SO HIGH time | $t_{PHSO}$ | 15 | | 8 | | | | ns | |
| SO LOW time | $t_{PLSO}$ | 20 | | 15 | | | | ns | |
| Delay, SO HIGH to OR LOW | $t_{DLOR}$ | | 21 | | 15 | | | ns | |
| Delay, SO LOW to OR HIGH | $t_{DHOR}$ | | 25 | | 20 | | | ns | |
| Data setup to OR HIGH | $t_{SOR}$ | -15 | | -12 | | | | ns | |
| Data hold from SO LOW | $t_{HSO}$ | 8 | | 5 | | | | ns | |
| Bubble through time | $t_{BT}$ | | 1200 | | 1000 | | | ns | |
| $\overline{MR}$ pulse width | $t_{PMR}$ | 50 | | 30 | | | | ns | |
| $\overline{MR}$ HIGH to SI HIGH | $t_{DSI}$ | 50 | | 30 | | | | ns | |
| $\overline{MR}$ LOW to OR LOW | $t_{DOR}$ | | 50 | | 30 | | | ns | |
| $\overline{MR}$ LOW to IR HIGH | $t_{DIR}$ | | 50 | | 30 | | | ns | |
| $\overline{MR}$ LOW to output LOW | $t_{LZMR}$ | | 50 | | 30 | | | ns | Note 7 |
| Output valid from $\overline{OE}$ LOW | $t_{OOE}$ | | 40 | | 28 | | | ns | |
| Output HIGH-Z from $\overline{OE}$ HIGH | $t_{HZOE}$ | | 40 | | 28 | | | ns | |

NOTES
4. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} = t_{DHOR}$.
5. $t_{SSI}$ and $t_{HSI}$ apply when memory is not full.
6. Hold time is the lesser of the two parameters (a) and (b).
7. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.

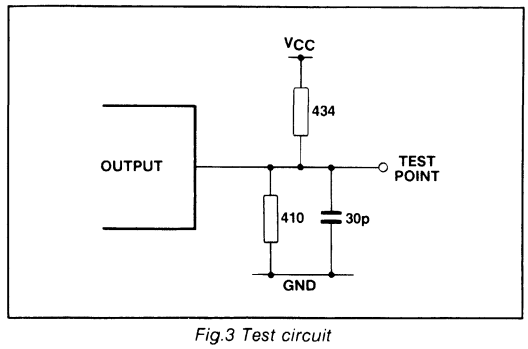



*Fig.3 Test circuit*

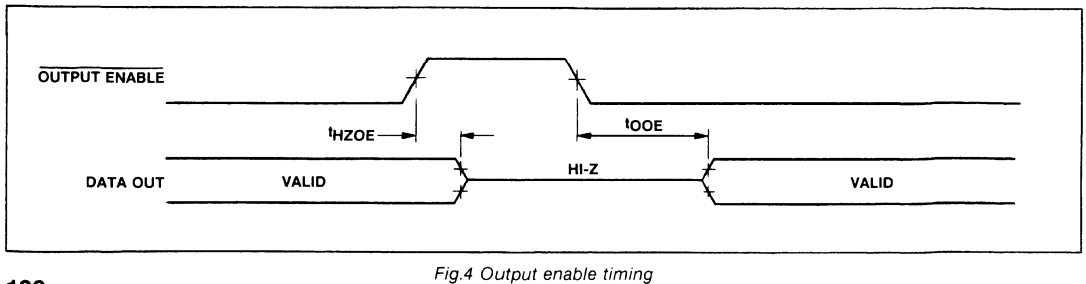



*Fig.4 Output enable timing*

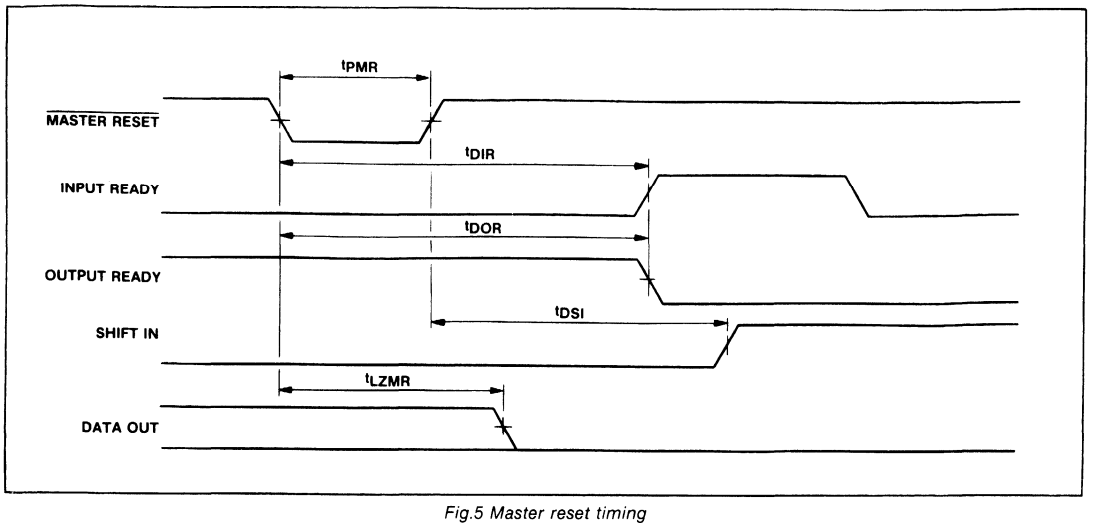



*Fig.5 Master reset timing*

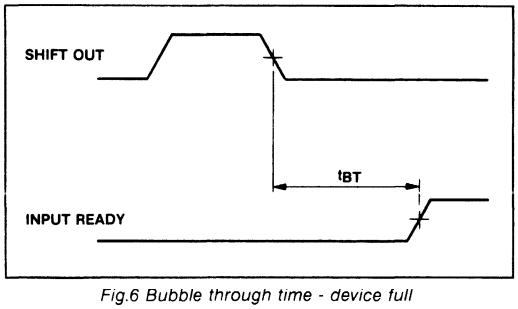



*Fig.6 Bubble through time - device full*

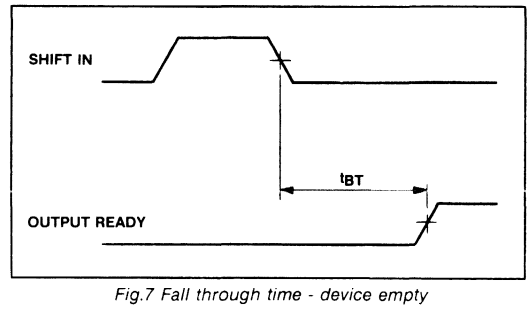



*Fig.7 Fall through time - device empty*

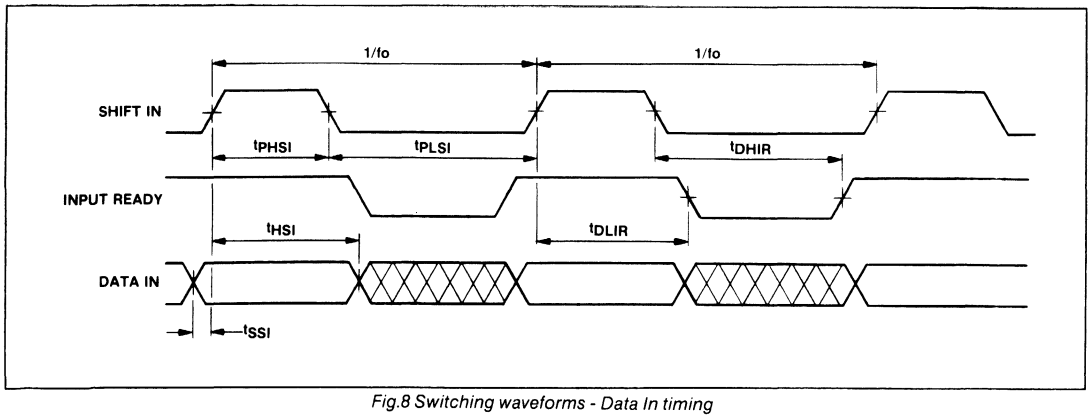



*Fig.8 Switching waveforms - Data In timing*

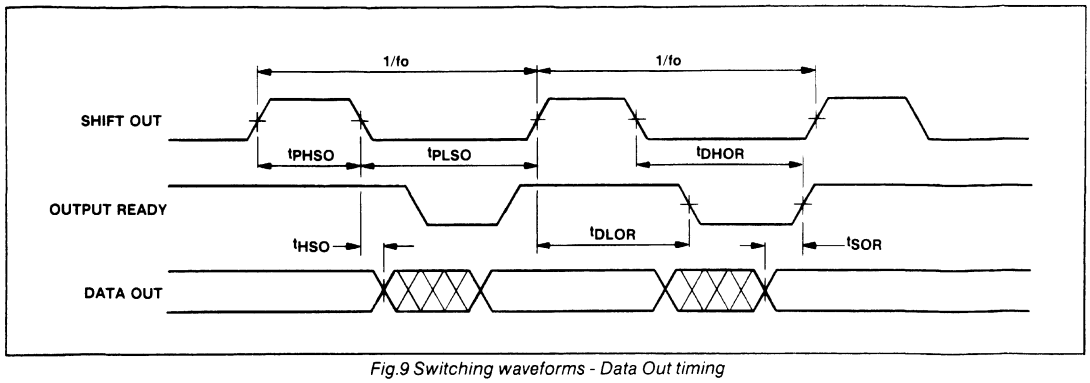



*Fig.9 Switching waveforms - Data Out timing*

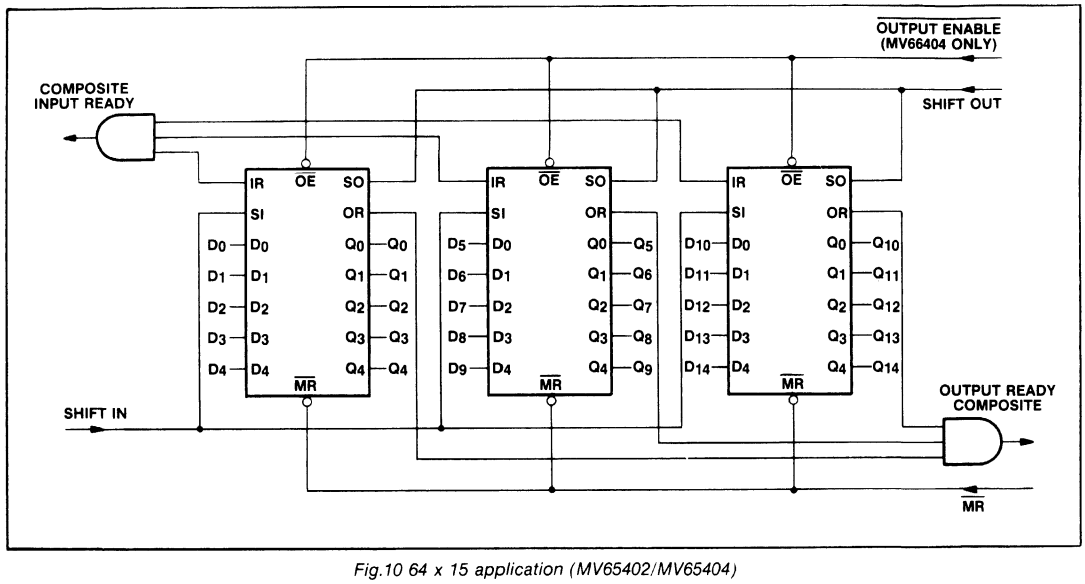



*Fig.10 64 x 15 application (MV65402/MV65404)*

## USER NOTES

1. When the memory is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.

## TYPICAL CHARACTERISTICS

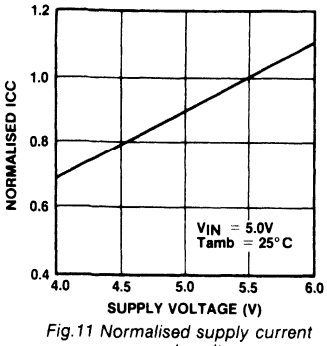



*Fig.11 Normalised supply current vs. supply voltage*

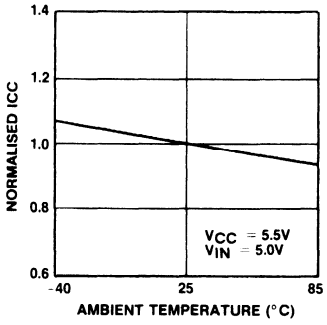



*Fig.12 Normalised supply current vs. ambient temperature*

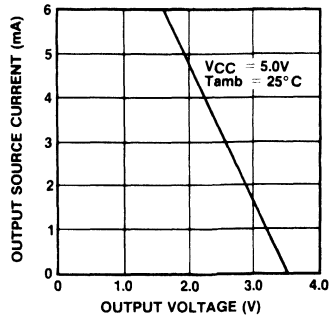



*Fig.13 Output source current vs. output voltage*

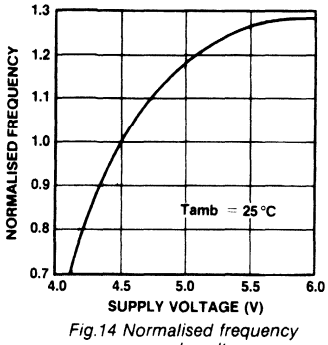



*Fig.14 Normalised frequency vs. supply voltage*

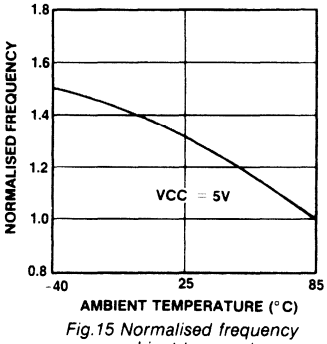



*Fig.15 Normalised frequency vs. ambient temperature*

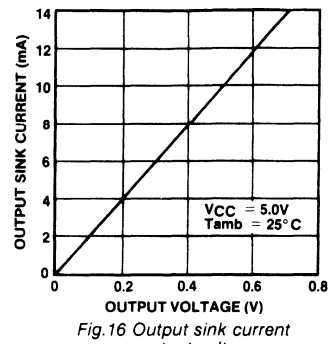



*Fig.16 Output sink current vs. output voltage*

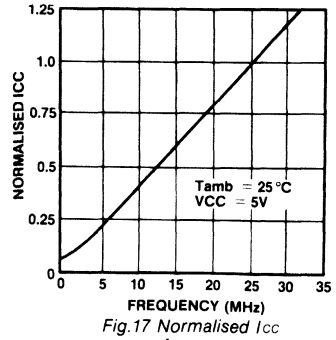



*Fig.17 Normalised Icc vs. frequency*

## ORDERING INFORMATION

### Industrial

**MV65401-25 B0 DG** (Industrial - Ceramic DIL package)
**MV65401-35 B0 DG** (Industrial - Ceramic DIL package)
**MV65402-25 B0 DG** (Industrial - Ceramic DIL package)
**MV65402-35 B0 DG** (Industrial - Ceramic DIL package)
**MV65403-25 B0 DG** (Industrial - Ceramic DIL package)
**MV65403-35 B0 DG** (Industrial - Ceramic DIL package)
**MV65404-25 B0 DG** (Industrial - Ceramic DIL package)
**MV65404-35 B0 DG** (Industrial - Ceramic DIL package)
**MV65401-25 B0 DP** (Industrial - Plastic DIL package)
**MV65401-35 B0 DP** (Industrial - Plastic DIL package)
**MV65402-25 B0 DP** (Industrial - Plastic DIL package)
**MV65402-35 B0 DP** (Industrial - Plastic DIL package)
**MV65403-25 B0 DP** (Industrial - Plastic DIL package)
**MV65403-35 B0 DP** (Industrial - Plastic DIL package)
**MV65404-25 B0 DP** (Industrial - Plastic DIL package)
**MV65404-35 B0 DP** (Industrial - Plastic DIL package)
**MV65401-25 B0 LC** (Industrial - LCC package)
**MV65401-35 B0 LC** (Industrial - LCC package)
**MV65402-25 B0 LC** (Industrial - LCC package)
**MV65402-35 B0 LC** (Industrial - LCC package)
**MV65403-25 B0 LC** (Industrial - LCC package)
**MV65403-35 B0 LC** (Industrial - LCC package)
**MV65404-25 B0 LC** (Industrial - LCC package)
**MV65404-35 B0 LC** (Industrial - LCC package)

### Military

**MV65401 A0 DG** (Military - Ceramic DIL package)
**MV65402 A0 DG** (Military - Ceramic DIL package)
**MV65403 A0 DG** (Military - Ceramic DIL package)
**MV65404 A0 DG** (Military - Ceramic DIL package)
**MV65401 A0 LC** (Military - LCC package)
**MV65402 A0 LC** (Military - LCC package)
**MV65403 A0 LC** (Military - LCC package)
**MV65404 A0 LC** (Military - LCC package)

Call for availability on High Reliability parts and MIL 883C screening.

# MV61901

## 1K WORD x 9-BIT FIRST-IN FIRST-OUT MEMORY

The MV61901 is a dual port RAM that utilises a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device provides full and empty flags to prevent data overflow and underflow, and control logic allows for unlimited expansion in both word size and depth.

The reads and writes are internally sequenced through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins.

The device provides a 9-bit wide storage array to allow for an additional control or parity bit at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. The device also features a RETRANSMIT capability which will reset the read pointer to its initial position when $\overline{RT}$ is pulsed low. This allows for retransmission from the beginning of the previously read block of data.

The MV61901 is offered in three variants according to maximum guaranteed access time, denoted by suffix numbers -50, -80 and -120.

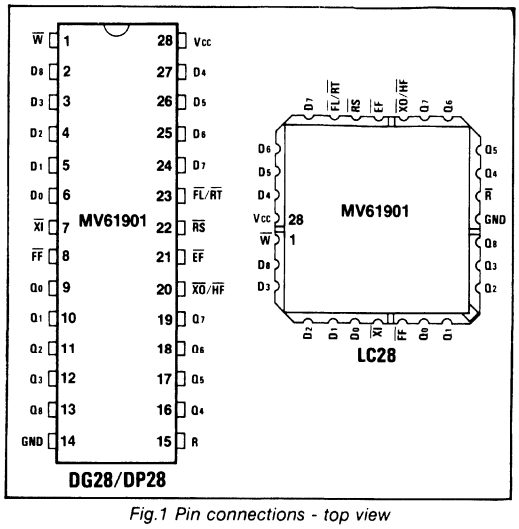



*Fig.1 Pin connections - top view*

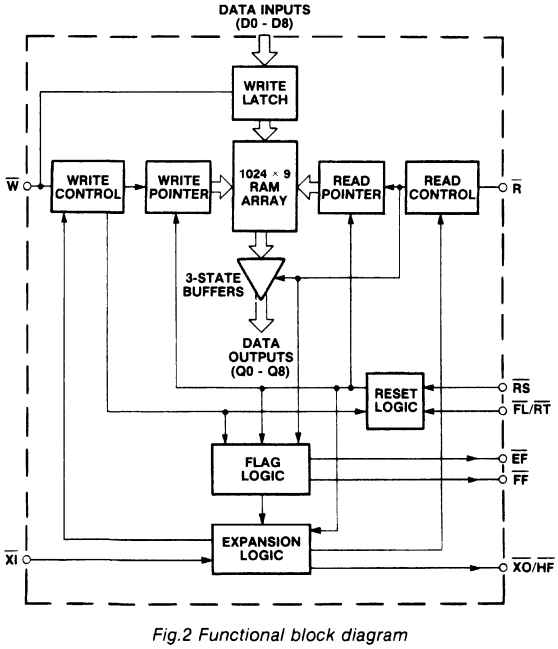



*Fig.2 Functional block diagram*

### FEATURES

- First-In, First-Out Dual Port Memory with Simultaneous Reads and Writes
- Ultra High Speed - 65ns Cycle Time 50ns Access Time (MV61901-50)
- 1024 x 9 Organisation
- Power Consumption less than 250mW at 10MHz
- Fully Cascadable in both Word Depth and/or Bit Width
- Functionally and Pin Compatible with IDT7202A but with Improved Set Up and Hold Times
- Full and Empty Flags
- Half-Full Flag Capability in Single Device Mode
- Auto Retransmit Capability

### APPLICATIONS

- Asynchronous Buffer between Digital Systems
- Disk or Tape Interfaces
- Data Communications

### ASSOCIATED PRODUCTS

| | |
|---|---|
| **MV61902** | 1K x 9 Dipstick FIFO |
| **MV61903** | 1K x 9 Parity FIFO |
| **MV65030** | 64 x 9, Tristate 35MHz standalone FIFO |
| **MV65401/2/3/4** | 64 x 4/5, Bistate/Tristate 35MHz standalone FIFOs |
| **MV66030** | 64 x 9, Tristate 25MHz cascadable FIFO |
| **MV66401/2/3/4** | 64 x 4/5, Bistate/Tristate 25MHz cascadable FIFOs |

## FUNCTIONAL OPERATION

### RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. After power up, a reset must be provided before attempting a write operation. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during the window shown in Fig.3; i.e., $t_{RPW}$ or $t_{WPW}$ before the rising edge of $\overline{RS}$ and should not change until $t_{RSR}$ after the rising edge of $\overline{RS}$. The HALF-FULL FLAG ($\overline{HF}$) and FULL FLAG ($\overline{FF}$) will both be reset to high after master RESET ($\overline{RS}$). The EMPTY FLAG ($\overline{EF}$) will be low.

#### Writing

A write cycle is initiated on the falling edge of WRITE ENABLE ($\overline{W}$) provided the FULL FLAG ($\overline{FF}$) is not set but not completed until the input goes back high. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF-FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF-FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, and inhibit further writes after the current operation, whenever the write pointer equals the read pointer. If the read pointer is not activated after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 1024 writes. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after $t_{RFF}$, and allow a valid write to begin.

#### Reading

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, allowing the 'final' read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after $t_{WEF}$, and a valid READ can then begin.

### FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded. (See Operating Modes.) In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the EXPANSION IN ($\overline{XI}$).

The MV61901 can be made to retransmit data when the RETRANSMIT ENABLE CONTROL ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Correct operation of the flags is maintained. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is only useful when less than 1024 writes are performed between resets, and is not compatible with Depth Expansion Mode.

### EXPANSION IN ($\overline{XI}$)

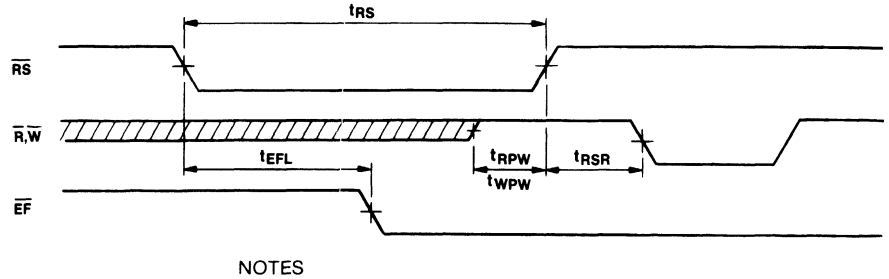
This input is a dual purpose pin. EXPANSION IN ($\overline{XI}$) is grounded to indicate an operation in the single device mode. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

### EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual purpose output. In the single device mode, when EXPANSION IN ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF-FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF-FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.




NOTES
1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R}$ = $V_{IH}$ around the rising edge of $\overline{RS}$.

*Fig.3 Reset*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Under Recommended operating conditions

| Characteristic | Symbol | Value | | | | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | INDUSTRIAL | | | | | | MILITARY | | | |
| | | MV61901 B0 | | | | | | MV61901 A0 | | | |
| | | -50 | | -80 | | -120 | | Min. | Max. | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | | | |
| Output high level<br>$V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OH} = -8mA$ | $V_{OH}$ | 2.4 | | 2.4 | | 2.4 | | | | V | |
| Output low level<br>$V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OL} = 8mA$ | $T_{OL}$ | | 0.4 | | 0.4 | | 0.4 | | | V | |
| Input leakage $V_{IN} = = V_{IH}$ or $V_{IL}$ | $I_{IN}$ | -10 | +10 | -10 | +10 | -10 | +10 | | | $\mu A$ | |
| Output leakage GND $\leqslant V_{OUT} \leqslant V_{CC}$<br>$V_{CC} = V_{CC\ max.}$ | $I_{OZ}$ | -50 | +50 | -50 | +50 | -50 | +50 | | | $\mu A$ | |
| Short circuit | $I_{OS}$ | | | | 80 | | 80 | | | mA | Note 2 |
| Supply current | $I_{CC}$ | | 80 | | 60 | | 40 | | | mA | $V_{CC}$ = max.<br>$T_{amb}$ = 70°C<br>$I_{LOAD}$ = 0mA |
| Standby current | | | 5 | | 5 | | 5 | | | | $V_{CC}$ = max.<br>$I_{LOAD}$ = 0mA<br>All inputs at $V_{IL}$ |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5V to 7.0V |
| Input voltage $V_{IN}$ (see Note 3) | -0.9V to $V_{CC}$ +0.9V |
| DC voltage applied to output when high impedance | -0.5V to 7.0V |
| Clamp diode current per pin (see Note 2) | +18mA |
| Storage temperature Ts | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -55°C to +125°C |
| Package power dissipation | |
| DP | 450mW |
| DG | 1000mW |
| LC | 1000mW |

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage $V_{CC}$ | 5V ± 10% |
| Min. input high level $V_{IH}$ | +2V |
| Max. input low level $V_{IL}$ | +0.8V |
| Ambient temperature | |
| Industrial | -40°C to 85°C |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{CC}$ = 5V ± 10%, $T_{amb}$ = -40°C to +85°C

| Characteristic | Symbol | Value | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | INDUSTRIAL | | | | | | MILITARY | | |
| | | MV61901 B0 | | | | | | MV61901 A0 | | |
| | | -50 | | -80 | | -120 | | Min. | Max. | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | | |
| Read Cycle Time | $t_{RC}$ | 65 | - | 100 | - | 140 | - | | | ns |
| Access Time | $t_A$ | - | 50 | - | 80 | - | 120 | | | ns |
| Read Recovery Time | $t_{RR}$ | 15 | - | 20 | - | 20 | - | | | ns |
| Read Pulse Width | $t_{RPW}$ | 50 | - | 80 | - | 120 | - | | | ns |
| Read Pulse Low to Dta Bus at Low Z | $t_{RLZ}$ | 10 | - | 10 | - | 10 | - | | | ns |
| Write Pulse High to Data Bus at Low Z | $t_{WLZ}$ | 15 | - | 18 | - | 20 | - | | | ns |
| Data Valid from Read Pulse High | $t_{DV}$ | 5 | - | 6 | - | 8 | - | | | ns |
| Read Pulse High to Data Bus at High Z | $t_{RHZ}$ | - | 12 | - | 19 | - | 25 | | | ns |
| Write Cycle Time | $t_{WC}$ | 65 | - | 100 | - | 140 | - | | | ns |
| Write Pulse Width | $t_{WPW}$ | 50 | - | 80 | - | 120 | - | | | ns |
| Write Recovery Time | $t_{WR}$ | 15 | - | 20 | - | 20 | - | | | ns |
| Data Setup Time | $t_{DS}$ | 8 | - | 9 | - | 10 | - | | | ns |
| Data Hold Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | | | ns |
| Reset Cycle Time | $t_{RSC}$ | 65 | - | 100 | - | 140 | - | | | ns |
| Reset Pulse Width | $t_{RS}$ | 50 | - | 80 | - | 120 | - | | | ns |
| Reset Recovery Time | $t_{RSR}$ | 15 | - | 20 | - | 20 | - | | | ns |
| Retransmit Cycle Time | $t_{RTC}$ | 65 | - | 100 | - | 140 | - | | | ns |
| Retransmit Pulse Width | $t_{RT}$ | 50 | - | 80 | - | 120 | - | | | ns |
| Retransmit Recovery Time | $t_{RTR}$ | 15 | - | 20 | - | 20 | - | | | ns |
| Reset to Empty Flag Low | $t_{EFL}$ | - | 16 | - | 25 | - | 30 | | | ns |
| Reset to Half and Full Flag High | $t_{HFH,FFH}$ | - | 13 | - | 19 | - | 24 | | | ns |
| Read Low to Empty Flag Low | $t_{REF}$ | - | 35 | - | 53 | - | 67 | | | ns |
| Read High to Full Flag High | $t_{RFF}$ | - | 16 | - | 25 | - | 30 | | | ns |
| Write High to Empty Flag High | $t_{WEF}$ | - | 48 | - | 74 | - | 87 | | | ns |
| Write Low to Full Flag Low | $t_{WFF}$ | - | 18 | - | 27 | - | 35 | | | ns |
| Write Low to Half-Full Flag Low | $t_{WHF}$ | - | 18 | - | 27 | - | 35 | | | ns |
| Read High to Half-Full Flag High | $t_{RHF}$ | - | 18 | - | 27 | - | 35 | | | ns |

NOTES
Because of the high speed operation of these devices, it is necessary to ensure good decoupling close to the supply pins. Ringing on $\overline{R}$ and $\overline{W}$ lines must not violate $V_{IL}$ and $V_{IH}$ requirements even for periods substantially less than $t_{RPW}$ and $t_{WPW}$ as pointer incrementing may still occur.

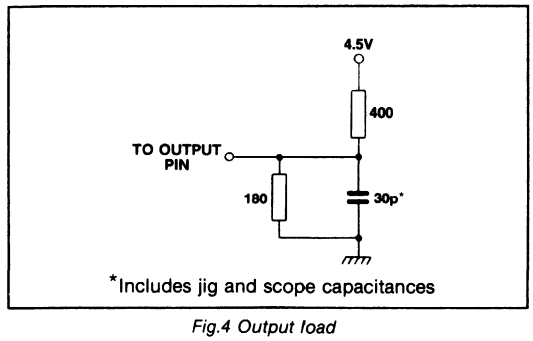



*Fig.4 Output load*

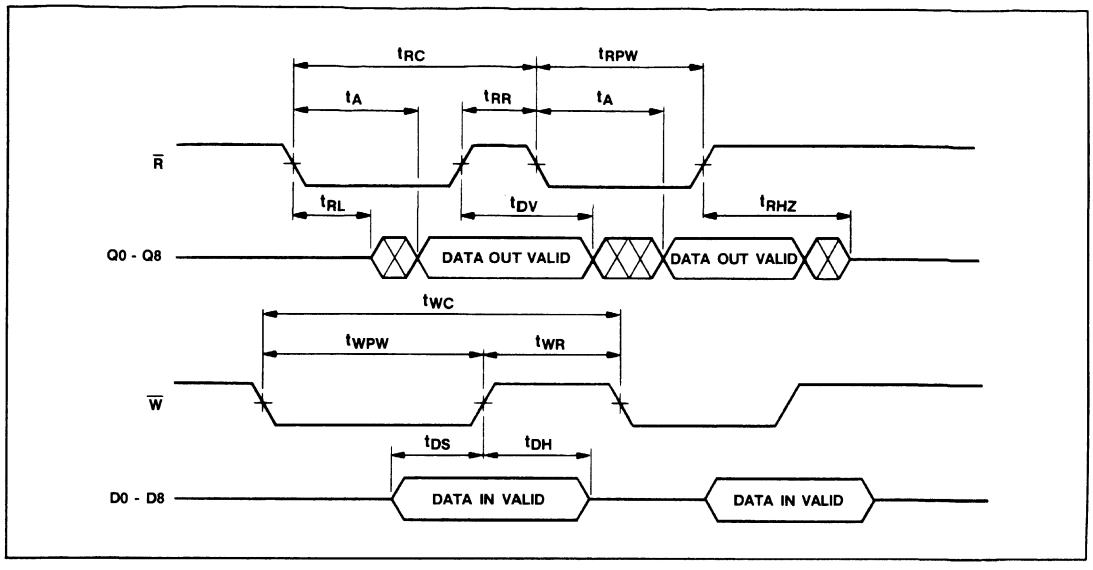



*Fig.5 Asynchronous Write and Read operation*

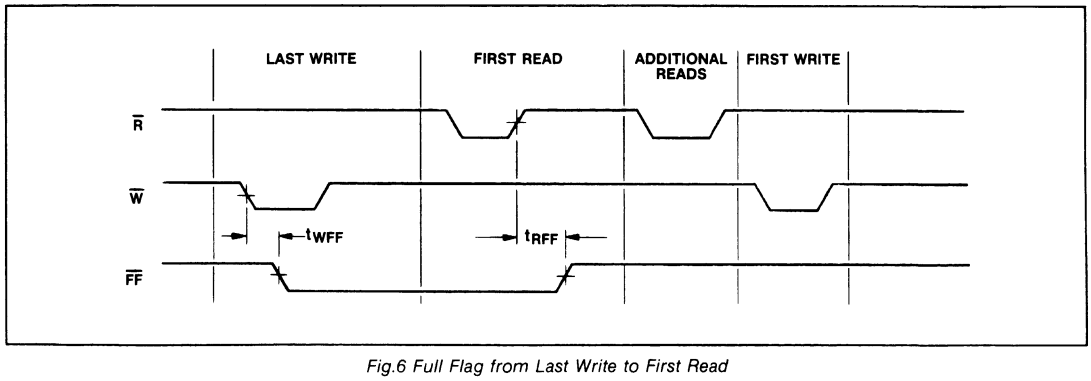



*Fig.6 Full Flag from Last Write to First Read*

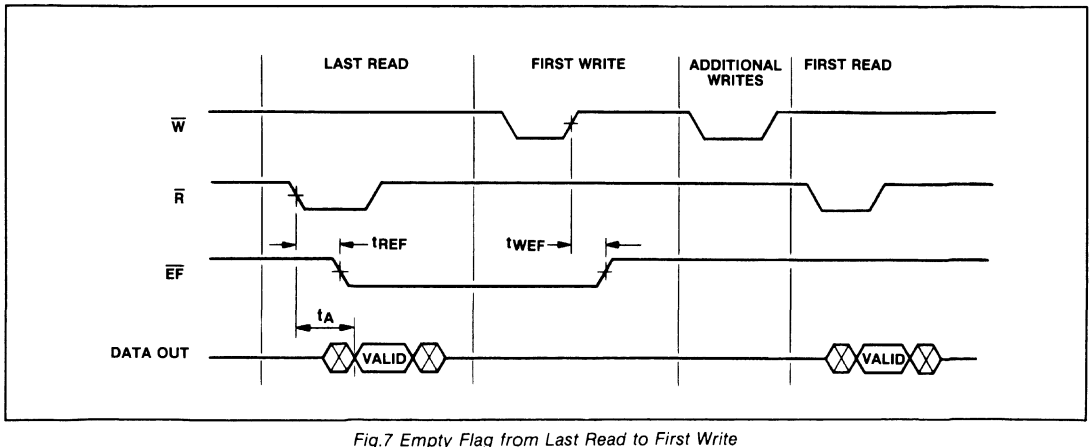



*Fig.7 Empty Flag from Last Read to First Write*

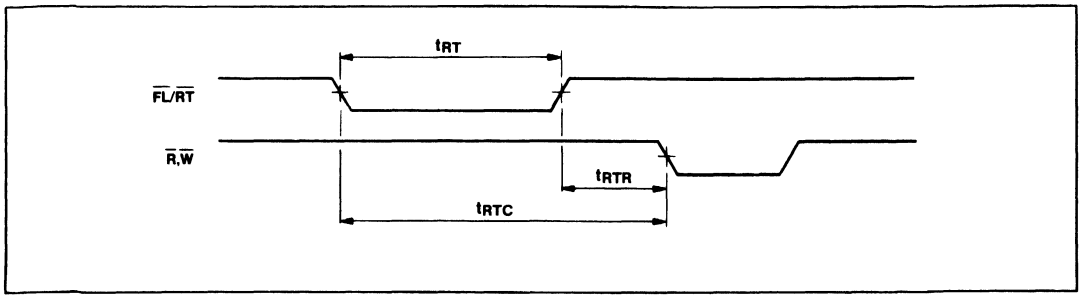



*Fig.8 Retransmit timing*

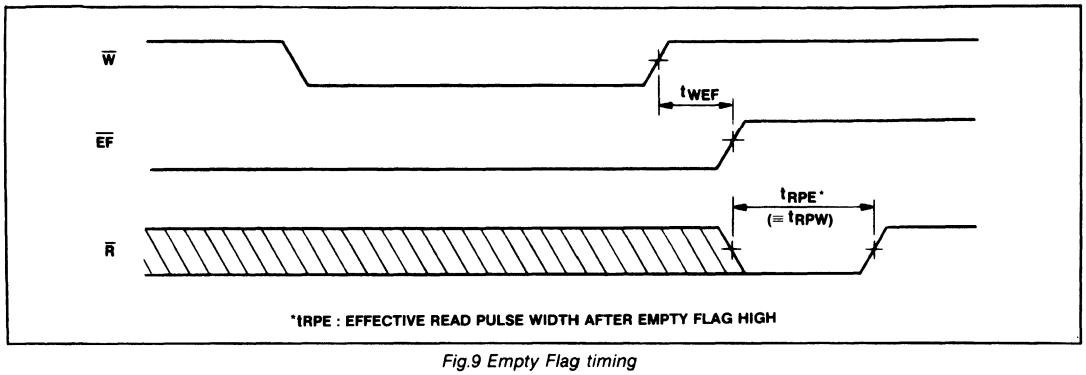



*Fig.9 Empty Flag timing*

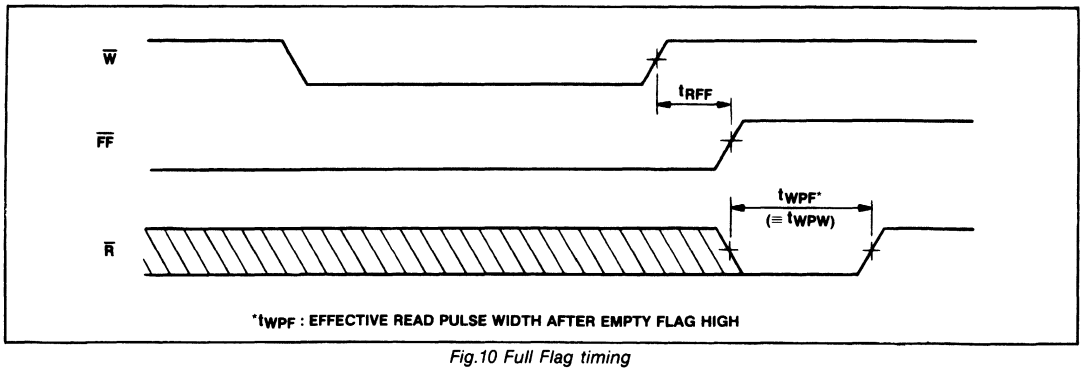



*Fig.10 Full Flag timing*

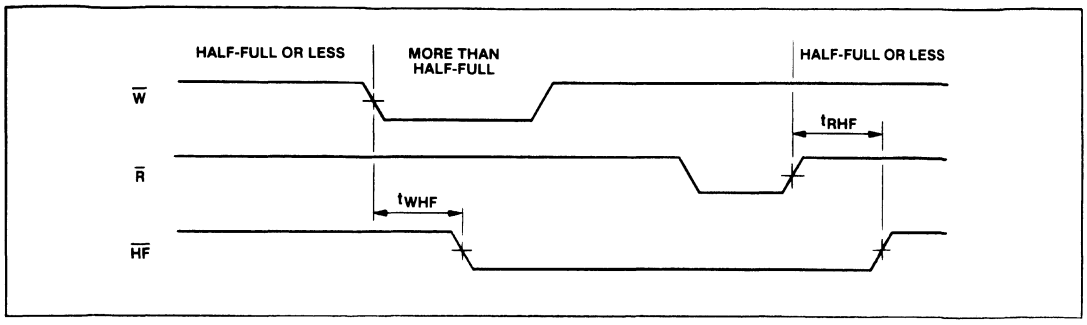



*Fig.11 Half-Full Flag timing*

## OPERATING MODES

### Single device Mode MV61901

A single MV61901 may be used when the application requirements are for 1024 words or less. A Single Device Configuration requires the EXPANSION IN ($\overline{XI}$) control input to be grounded. (See Fig.12.) In this mode the HALF-FULL FLAG ($\overline{HF}$) and RETRANSMIT functions are available.

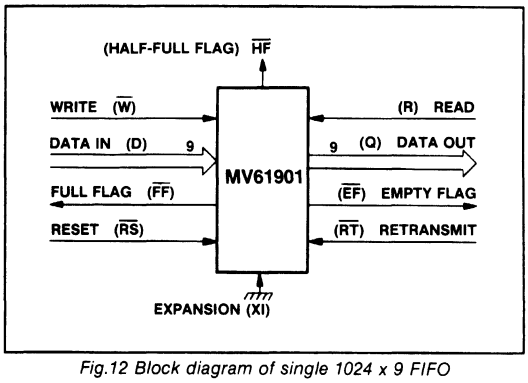
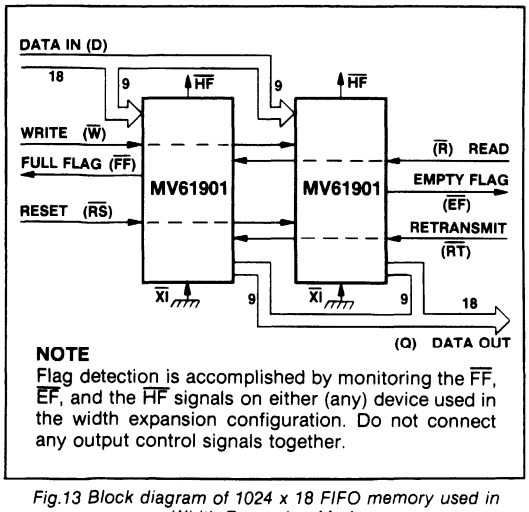



*Fig.12 Block diagram of single 1024 x 9 FIFO*




**NOTE**
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

*Fig.13 Block diagram of 1024 x 18 FIFO memory used in Width Expansion Mode*

### Width Expansion Mode

Word width may be increased by simply connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Fig.13 demonstrates an 18-bit word width obtained by using two MV61901s. Any word width can be attained by adding additional devices.

### Depth Expansion (Daisy Chain) Mode

The MV61901 can easily be adapted to applications when the requirements are for greater than 1024 words. Fig.14 demonstrates Depth Expansion using three MV61901s. Any depth can be attained by adding additional MV61901s. The MV61901 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Fig.14.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Fig.14.
5. The RETRANSMIT ($\overline{RT}$) function and HALF-FULL FLAG ($\overline{HF}$) are not available in the Depth Expansion Mode.

### Compound Expansion Mode

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Fig.15.)

### Bidirectional Mode

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing MV61901s as is shown in Fig.16. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

### Data Flow-Through Modes

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Fig.17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after $t_{RHS}$ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would de-assert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (fig.18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

### TRUTH TABLES

| Mode | Inputs | | | Internal Status | | Outputs | | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{RS}$ | $\overline{RT}$ | $\overline{XI}$ | Read Pointer | Write Pointer | $\overline{EF}$ | $\overline{FF}$ | $\overline{HF}$ |
| Reset | 0 | X | 0 | Location Zero | Location Zero | 0 | 1 | 1 |
| Retransmit | 1 | 0 | 0 | Location Zero | Unchanged | X | X | X |
| Read/Write | 1 | 1 | 0 | Increment (Note 1) | Increment (Note 1) | X | X | X |

NOTE
1. Pointer will increment if flag is high.

*Table 1 RESET and RETRANSMIT - Single device configuration/width expansion mode*

| Mode | Inputs | | | Internal Status | | Outputs | |
|---|---|---|---|---|---|---|---|
| | $\overline{RS}$ | $\overline{FL}$ | $\overline{XI}$ | Read Pointer | Write Pointer | $\overline{EF}$ | $\overline{FF}$ |
| Reset-First Device | 0 | 0 | (Note 1) | Location Zero | Location Zero | 0 | 1 |
| Reset all Other Devices | 0 | 1 | (Note 1) | Location Zero | Location Zero | 0 | 1 |
| Read/Write | 1 | X | (Note 1) | X | X | X | X |

NOTES
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Fig.14.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, XI = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.

*Table 2 RESET and FIRST LOAD truth table - Depth expansion/compound expansion mode*

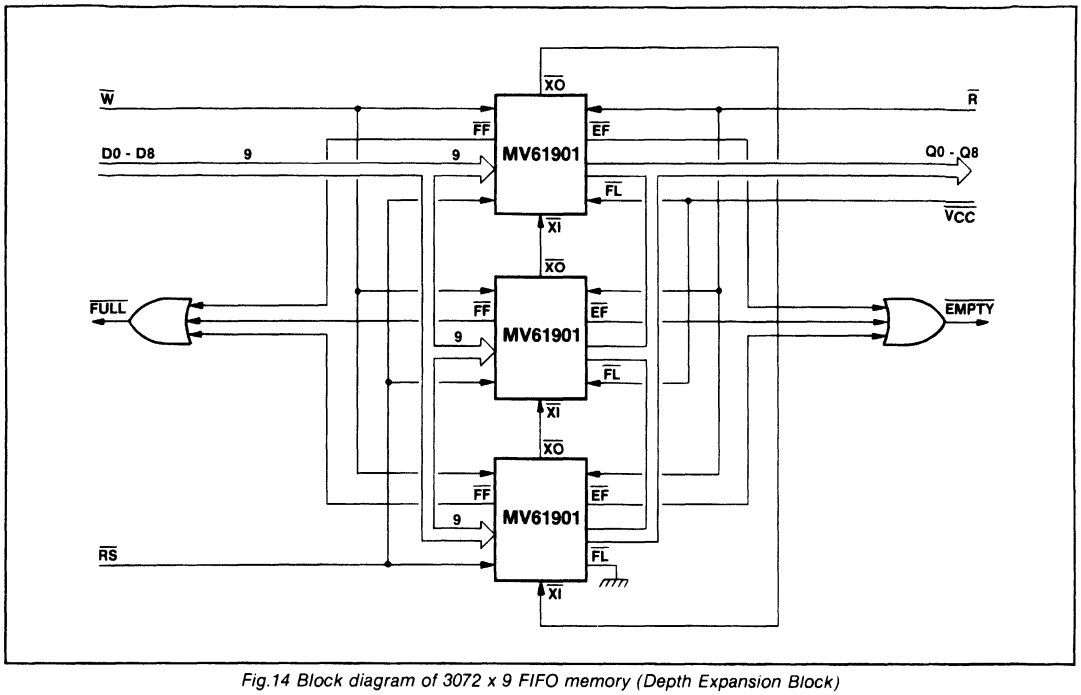
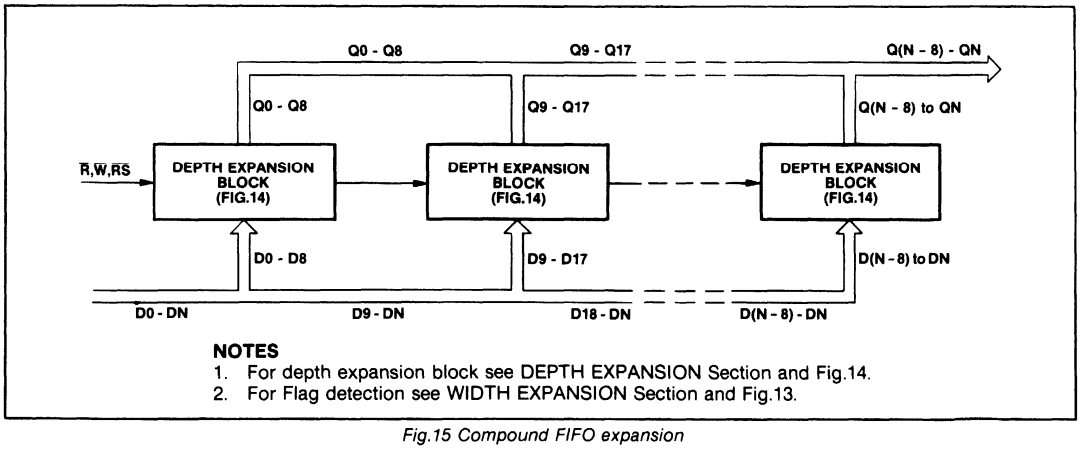



*Fig.14 Block diagram of 3072 x 9 FIFO memory (Depth Expansion Block)*




**NOTES**
1. For depth expansion block see DEPTH EXPANSION Section and Fig.14.
2. For Flag detection see WIDTH EXPANSION Section and Fig.13.

*Fig.15 Compound FIFO expansion*

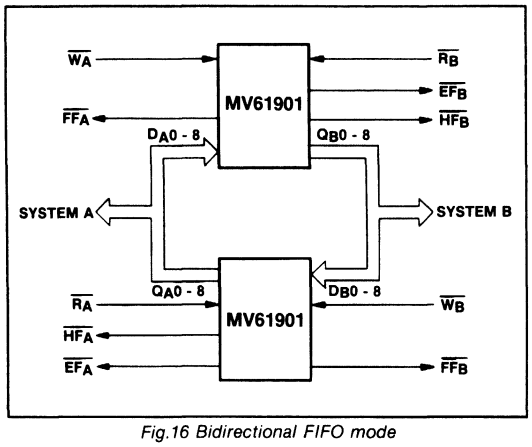



*Fig.16 Bidirectional FIFO mode*

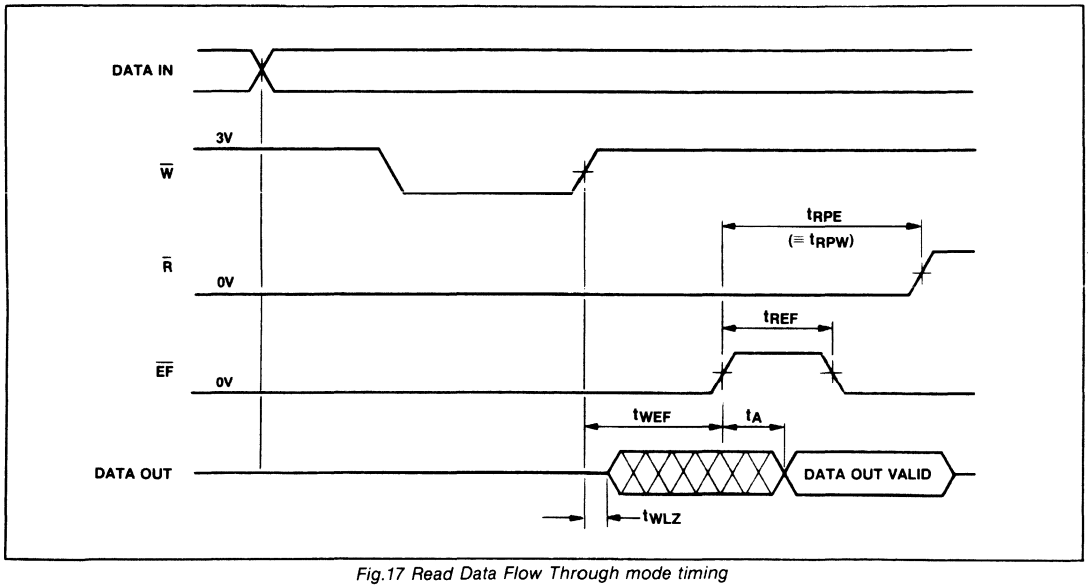



*Fig.17 Read Data Flow Through mode timing*

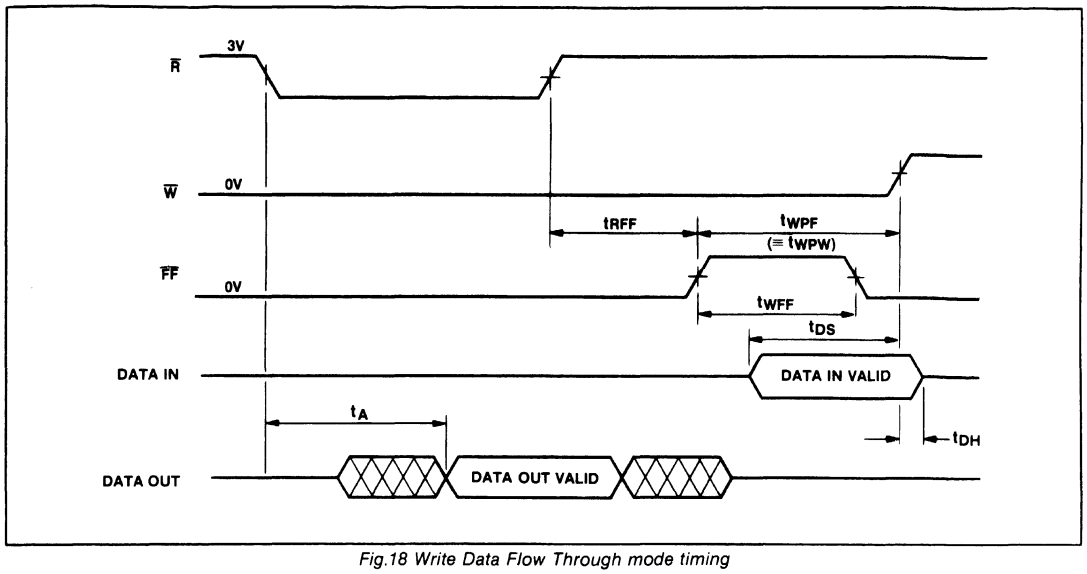



*Fig.18 Write Data Flow Through mode timing*

## ORDERING INFORMATION

**Industrial**

**MV61901-50 B0 DG** (Industrial - Ceramic DIL package)
**MV61901-80 B0 DG** (Industrial - Ceramic DIL package)
**MV61901-120 B0 DG** (Industrial - Ceramic DIL package)
**MV61901-50 B0 DP** (Industrial - Plastic DIL package)
**MV61901-80 B0 DP** (Industrial - Plastic DIL package)
**MV61901-120 B0 DP** (Industrial - Plastic DIL package)
**MV61901-50 B0 LC** (Industrial - LCC package)
**MV61901-80 B0 LC** (Industrial - LCC package)
**MV61901-120 B0 LC** (Industrial - LCC package)

**Military**

Call for availability on High Reliability parts and MIL 883C screening.
**MV61901 A0 DG** (Military - Ceramic DIL package)
**MV61901 A0 LC** (Military - LCC package)

# MV61902

## 1K x 9 DIPSTICK™ FIFO

The MV61902 is one of a new generation of RAM-based FIFOs designed for ease of use. The MV61902 has a user-programmable flag (DIPSTICK) which defaults to a conventional 'half-full' flag on power-up.

The FIFO has input and output registers and a truly asynchronous 3-state output enable to simplify interfacing.

Larger FIFO stores can be constructed by cascading parts in depth or width. In addition the MV61902 can be cascaded in such a way as to increase its speed. Two 10MHz MV61902s can be used to create a 20MHz 2K x 9 FIFO structure.

### FEATURES

- 10MHz 1K word x 9-bit FIFO
- Full and Empty Flags
- User Programmable Flag (DIPSTICK)
- Cascadable in Width, Depth and Speed
- Input and Output Registers
- Asynchronous Output Enable
- 2-micron CMOS
- Power Dissipation 250mW
- Operating Temperature Range -40°C to +85°C

### ORDERING INFORMATION

**MV61902DG** (Commercial - Ceramic DIL package)
**MV61902DP** (Commercial - Plastic DIL package)

### ASSOCIATED PRODUCTS

**MV61903** Parity FIFO 1K x 9
**MV66030** 64 x 9 25MHz FIFO
**MV66401-4** 64 x 4/5 25MHz FIFOs

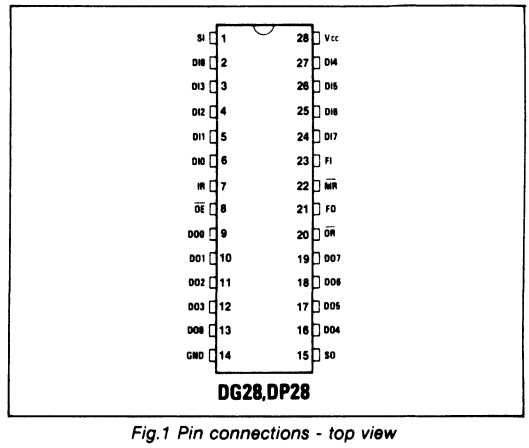



*Fig.1 Pin connections - top view*

### APPLICATIONS

- Disk or Tape Interfaces
- I/O Formatting in DSP Systems
- Video Line Stores
- Printer Buffers
- Data Queueing/De-queueing
- User Programmable Delay Lines

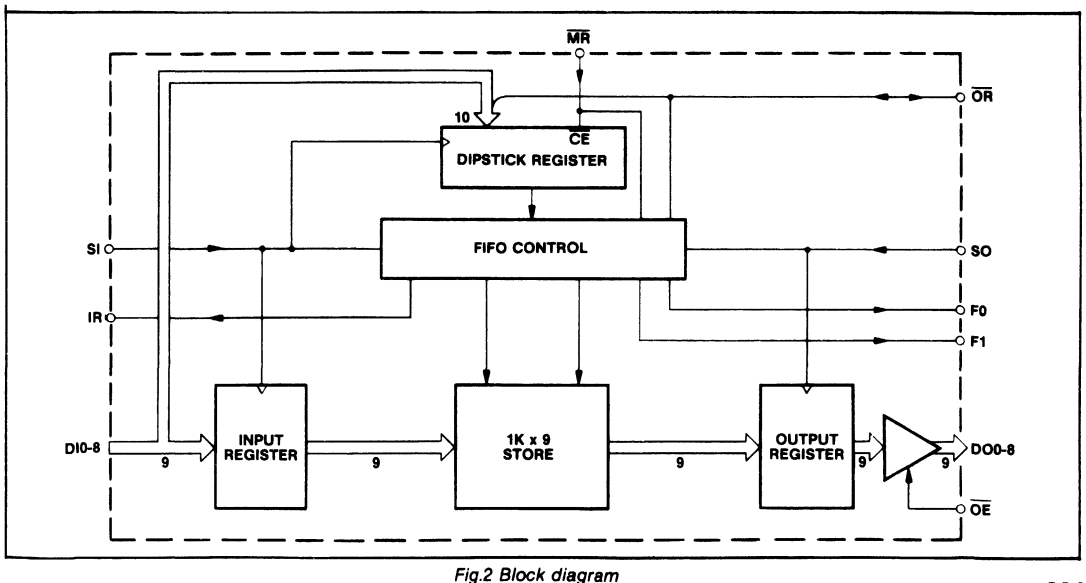



*Fig.2 Block diagram*

## PIN DESCRIPTIONS

| Symbol | Pin No. | Description |
|---|---|---|
| SI | 1 | **Shift in** The SI input is used to load data into the FIFO. On the rising edge of SI, the data present on the DI port is loaded into the input register and the write cycle that places the data within the store is initiated. During programming, the SI input is used to load data into the DIPSTICK Register. |
| SO | 15 | **Shift out** The SO input is used to clock data out from the FIFO. On the rising edge of SO, the data currently read from the store is loaded into the output register and the read cycle that reads the next output from the store is initiated. |
| IR | 7 | **Input ready** The IR flag indicates that the FIFO is ready to receive another input. After a rising edge of SI, IR will go low for the period required to write the new data into the store. Should IR remain low for more than the duration of one cycle the FIFO is full. |
| $\overline{OR}$ | 20 | **Output ready** The $\overline{OR}$ flag indicates that the FIFO is ready to output new data. After a rising edge of SO, $\overline{OR}$ will go high for the period required to read new data from the store. Should $\overline{OR}$ remain high for more than the duration of one cycle the FIFO is empty. During programming the $\overline{OR}$ output acts as a one bit input to LSB of the 10-bit DIPSTICK Register. |
| DI | 6,5,4, 3,27,26, 25,24,2 | **Data input** DI0-8 is the 9-bit data input to the FIFO. This input is internally registered, hence input data may be removed at any time after the rising edge of SI. During programming of DIPSTICK the DI input is the 9 MSBs input to the DIPSTICK Register. |
| DO | 9,10,11, 12,16,17, 18,19,13 | **Data output** DO0-8 is the 9-bit data output from the FIFO. This output is internally registered, hence the output data will not change until shortly after the rising edge of SO. |
| $\overline{MR}$ | 22 | **Master reset** The $\overline{MR}$ input to the FIFO performs two functions:<br>1. Resetting the FIFO to an empty state;<br>2. Enabling the DIPSTICK Register clock and causing $\overline{OR}$ to become an input to the 10th bit of the DIPSTICK Register. |
| OE | 8 | **Output enable** The OE input when high forces the DO0-8 outputs into a high impedance state. |
| F0 & F1 | 21,23 | **Flag outputs** The F0 and F1 flag outputs are encoded to represent 3 flag states, namely FULL (F1 = 1,F0 = 0), EMPTY (F1 = 0,F0 = 1), DIPSTICK (F1 = 1,F0 = 1). The flag outputs change when the last of SI or SO to go high finally goes low - see Section F0 and F1. |

## FUNCTIONAL DESCRIPTION

The MV61902 contains three main blocks; the 1K x 9 STORE and associated registers, the FIFO controller and the DIPSTICK Register.

### 1K x 9 STORE

The 1K x 9 STORE contains the data written into the FIFO. It accepts data from the input register, sources data to the output register, and is controlled by two pointers supplied by the FIFO controller.

### FIFO Controller

The FIFO controller accepts the SI, SO and $\overline{MR}$ inputs and generates the IR, $\overline{OR}$, F0 and F1 outputs and pointers for the store.

### SI and SO

SI and SO are the shift in and shift out signals to the FIFO. These inputs may be synchronous or asynchronous to one another. There are no restrictions on SI and SO with respect to each other. There is no maximum limit on SI or SO high or low periods, the only restriction being minimum SI or SO high or low periods which determine the cycle time. See Section F0 and F1.

The FIFO controller calculates the correct pointer outputs for the store, according to the sequence of SI or SO pulses.

### $\overline{MR}$

When low, the $\overline{MR}$ input to the FIFO controller resets both pointers to zero and sets the EMPTY flag (F0 = 0,F1 = 1) and loads the output register with zeros. Any SI or SO pulses that occur while $\overline{MR}$ is low will not change the state of the FIFO controller; the FIFO will remain empty.

### IR and $\overline{OR}$

Input ready and output ready are generated by the FIFO controller, dependent upon the state of SI, SO and the FULL and EMPTY flags.

While SI is high, IR is held low. IR can only go high if SI is low and the FIFO is ready to receive new inputs.

$\overline{OR}$ can only go low if the FIFO is ready to output new data. It is *not* dependent upon the state of SO. A rising edge on SO will cause $\overline{OR}$ to go high for a period equal to the time required to read new data from the store.

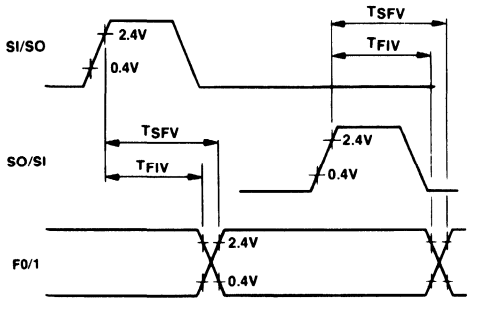



*Fig.3(a) SI and SO isolated*

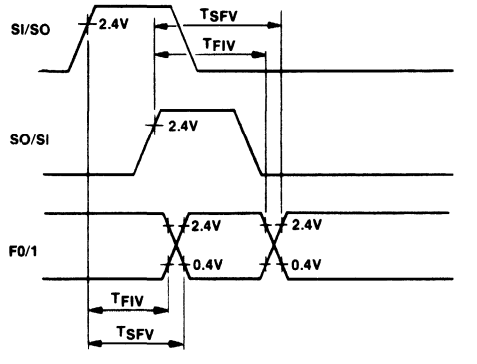



*Fig.3(b) SI and SO overlapping*

*Fig.3 F0/F1 timing for asynchronous SI/SI*

## F0 and F1

The F0 and F1 outputs change according to the state of SI and SO. FULL = (F1 = 1,F0 = 0), EMPTY = (F1 = 0,F0 = 1), DIPSTICK = (F1 = 1,F0 = 1).

The two usual cases for asynchronous (isolated or overlapping) SI and SO pulses are shown in Fig.3, the start of the invalid periods of F0 and F1 being indicated by $t_{FIV}$. In either case, the flags change a period equal to $t_{FIV}$ after the rising edge of SI or SO.

The flexibility of SI and SO timing relationships allows a further relationship for asynchronous SI and SO pulses, as shown in Fig.4, with the invalid F0 and F1 periods indicated.

In this case, either SI or SO is held high, while the remaining input is toggled. The flags change after each rising edge of either input.

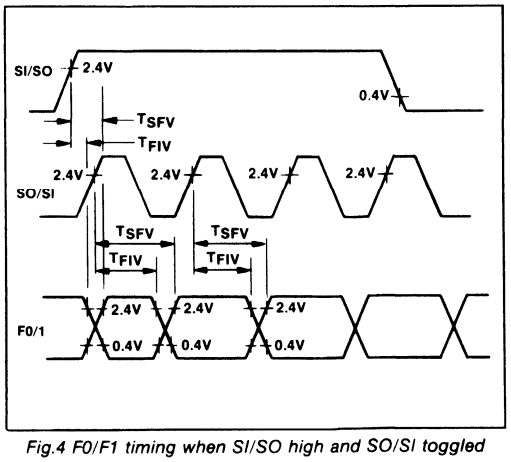



*Fig.4 F0/F1 timing when SI/SO high and SO/SI toggled*

## DIPSTICK Register

The DIPSTICK Register contains a value equal to the number of words in the store at which the DIPSTICK flag will become active.

The DIPSTICK Register defaults to a value of 512 on power up, and if not reprogrammed will continue to become active at this value, fulfilling the function of a 'half-full' flag.

The DIPSTICK Register may be reprogrammed while $\overline{MR}$ is active. A low on $\overline{MR}$ does not change the contents of the DIPSTICK Register, but enables the DIPSTICK Register clock. Any rising edge on SI while $\overline{MR}$ is low will cause a 10-bit word to be loaded into the DIPSTICK Register.

The 10-bit word is derived from two sources: the DI0-8 input and the $\overline{OR}$ output ($\overline{OR}$ acts as an input when MR is low).

The nine inputs derived from the DI0-8 inputs comprise the 9 most significant bits of the DIPSTICK Register, DI8 being the most significant bit. The bit derived from $\overline{OR}$ input forms the least significant bit of the DIPSTICK Register.

The $\overline{OR}$ input may be driven high or low by external logic while $\overline{MR}$ is low. This external logic must adopt a high impedance state whilst $\overline{MR}$ is high (Fig.5(a)) or be CMOS, and be connected to $\overline{OR}$ via a 10kΩ series resistor, see Fig.5(c)).

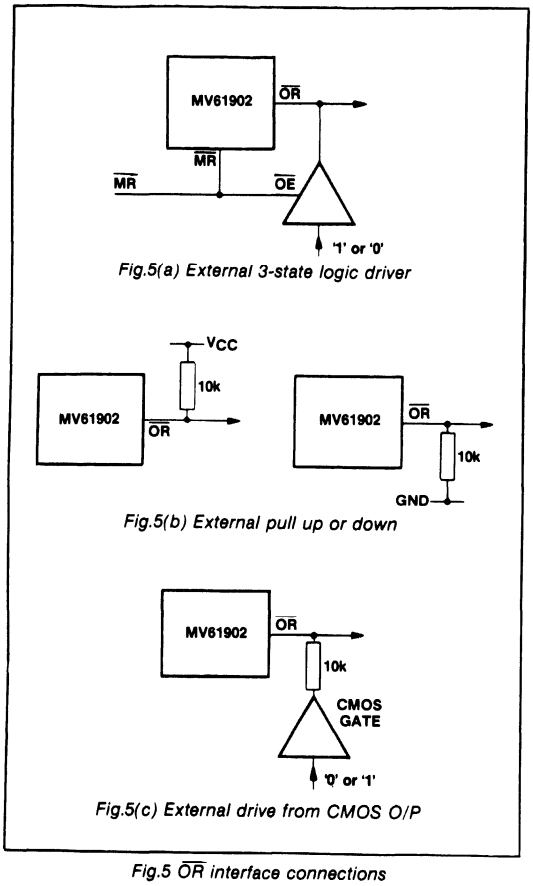



*Fig.5(a) External 3-state logic driver*

*Fig.5(b) External pull up or down*

*Fig.5(c) External drive from CMOS O/P*

*Fig.5 $\overline{OR}$ interface connections*

## CASCADING

The MV61902 DIPSTICK FIFO will cascade in width, depth or speed.

### Width

Multiple MV61902 DIPSTICK FIFOs may be configured as one 1K x (n x 9) FIFO with n independent DIPSTICK flags. See Fig.6 for 1K x 27 example.

### Depth

Multiple MV61902 DIPSTICK FIFOs may be configured as one nK x 9 FIFO, see Fig.7 for 3K x 9 example.

In this configuration, each DIPSTICK flag operates within one of the 1K blocks of the 3K total store. On power up, these flags will default to detect 512 words, 1536 words and 2560 words in the store. The 'full' flags from the second and third stages correspond to 2048 word and 1024 word flags respectively.

These expansion techniques may be combined to allow expansion in width and depth with a corresponding increase in the number of available flags.

### Speed

The MV61902 DIPSTICK FIFO may be cascaded to increase speed and depth at the same time. Fig.8 illustrates a 2K x 9 20MHz FIFO example.

In this example the input data is loaded into alternate FIFOs and clocked out of alternate FIFOs. $\overline{MR}$ selects the top FIFO as the destination of the first word to be written into the store, consequently this FIFO contains the 1st, 3rd, 5th (odd numbered) words written into the store and hence, its DIPSTICK flag can only detect ODD values of store contents. Similarly, the bottom FIFO can only detect the EVEN value of the number of words within the store.

There is a capacity for 2048 words, each DIPSTICK flag has 1024 values, and these are interlaced to cover all 2048 possible values.

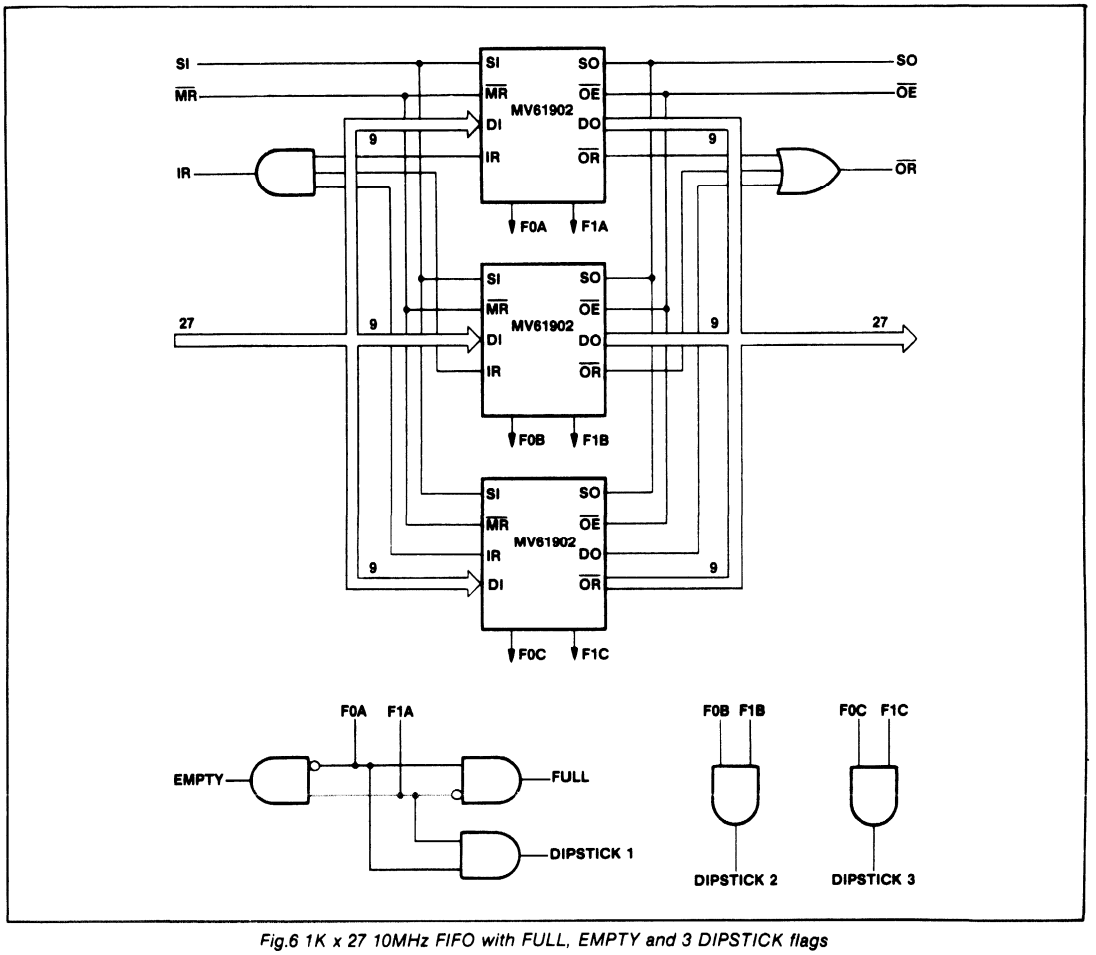



*Fig.6 1K x 27 10MHz FIFO with FULL, EMPTY and 3 DIPSTICK flags*

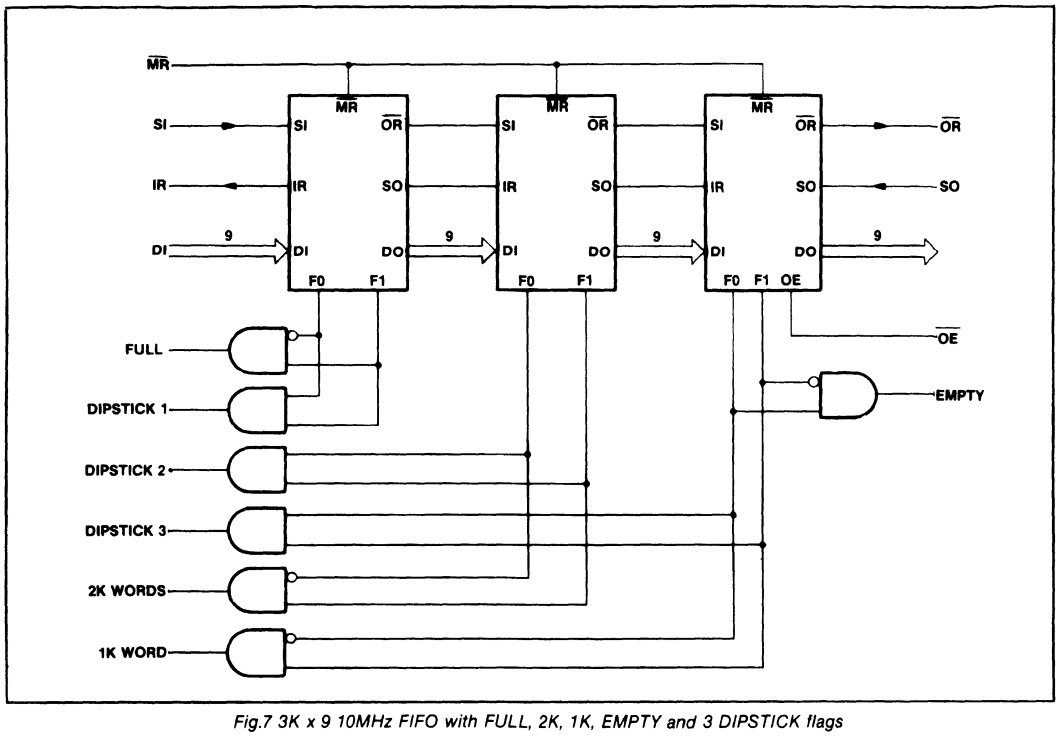



*Fig.7 3K x 9 10MHz FIFO with FULL, 2K, 1K, EMPTY and 3 DIPSTICK flags*

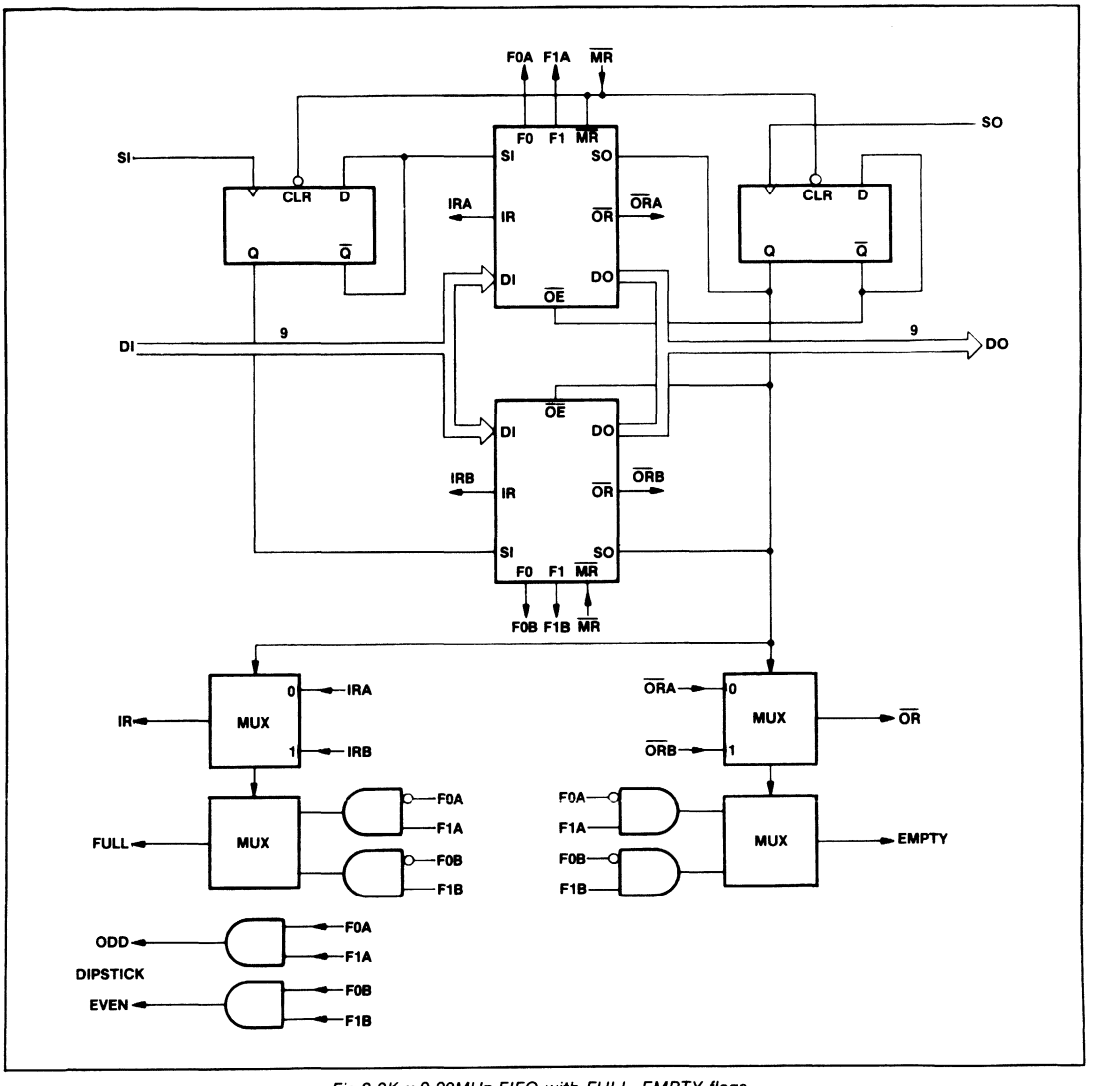



*Fig.8 2K x 9 20MHz FIFO with FULL, EMPTY flags*

## TYPICAL APPLICATIONS

### 10MHz User Programmable Delay Line

The MV61902 DIPSTICK FIFO may be configured as a user programmable delay line.

In this application, SI and SO are toggled synchronously, and the DIPSTICK Register is used to store the desired delay.

To build a 10MHz 1K x 9 delay line requires one MV61902 and one 3-input AND gate (see Fig.9).

An $\overline{MR}$ empties the FIFO and allows the DIPSTICK Register to be programmed with the desired delay. Subsequent clock cycles will load data into the FIFO, but no SO pulses will occur until the DIPSTICK flag becomes active as decoded by the 3-input AND gate.

Once DIPSTICK has become active, every clock pulse will cause an SI and SO to the FIFO, resulting in no net change in the FIFOs contents, and leaving DIPSTICK and hence, SO enabled.

Each CLK cycle will cause a word to be written into and read from the FIFO, implementing the operation of a delay line.

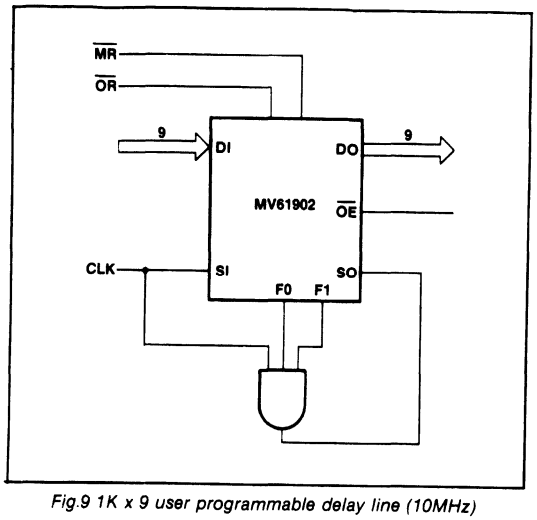



*Fig.9 1K x 9 user programmable delay line (10MHz)*

### 20MHz User Programmable Delay Line

To build a 20MHz 2K word delay line, two MV61902 DIPSTICK FIFOs must be cascaded as illustrated in Fig.10. This example will implement an ODD delay; should an EVEN delay be required, then the Q and Q signals driving the $\overline{OE}$ of the FIFOs should be interchanged as should the Q and Q signals driving the SO AND gates (see points marked X on Fig.10).

The delay (ODD) is programmed as follows.

For a delay of N cycles

$$\frac{(N - 1)}{2}$$

is programmed into the DIPSTICK Register of the lower FIFO and

$$\frac{(N - 1)}{2} + 1$$

is programmed into the DIPSTICK Register of the upper FIFO. If

$$\frac{(N - 1)}{2}$$

happened to be EVEN, then this programming may be achieved in a single cycle by presenting

$$\frac{(N - 1)}{2}$$

to the inputs to both FIFOs and setting $\overline{OR}$ high on the upper FIFO.

The delay operates as follows:

After an $\overline{MR}$, the FIFOs are empty and the DIPSTICK Registers may be programmed. Data may be shifted into the FIFOs, each CLK causing a new word to be shifted into each FIFO alternately, starting with the upper FIFO.

No data will be shifted out until a DIPSTICK flag becomes active and enables the SO input.

Once a FIFOs DIPSTICK flag has become active, after two further cycles of CLK, both an SI and an SO will have occurred, causing no net changes in the FIFOs contents, and hence, leaving the DIPSTICK flag active and the SO enabled. The FIFO structure will continue to operate as a delay line with one word clocked in and one clocked out on each subsequent clock cycle.

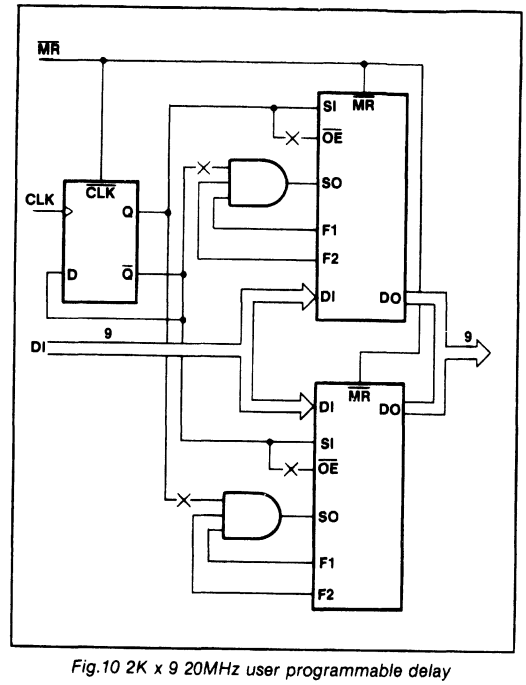



*Fig.10 2K x 9 20MHz user programmable delay*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 10%, GND = 0V

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output high voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = 8mA |
| Output low voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = -8mA |
| Input high voltage | $V_{IH}$ | 2.0 | | | V | |
| Input low voltage | $V_{IL}$ | | | 0.8 | V | |
| Input leakage current | $V_{IL}$ | -10 | | 10 | μA | GND ≤ $V_{IN}$ ≤ $V_{CC}$ |
| Vcc current | Icc | | | 50 | mA | $T_{amb}$ -40°C to +85°C |
| Output leakage current | Ioz | -50 | | 50 | μA | GND ≤ $V_{OUT}$ ≤ $V_{CC}$ = $V_{CC}$ max. |
| Output short CCT current (See Note 2) | Ios | 15 | | 80 | mA | $V_{CC}$ = max. |

**Switching Characteristics**

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| SO or SI low | 50 | | | ns | |
| SO or SI high | 25 | | | ns | |
| Setup DI0-8 to SI ⌐ | 20 | | | ns | |
| Hold DI0-8 to SI ⌐ | | | 0 | ns | |
| SO to DO0-8 valid | | | 25 | ns | 2 x LSTTL + 20pF |
| SI ⌐ to IR ⌙ | | | 20 | ns | 2 x LSTTL + 20pF |
| SI ⌙ to IR ⌐ - min SI pulse | | | 75 | ns | 2 x LSTTL + 20pF |
| SO ⌐ to $\overline{OR}$ ⌐ | | | 50 | ns | 2 x LSTTL + 20pF |
| SO ⌙ to $\overline{OR}$ ⌙ | | 30 | | ns | SO min pulse width |
| $\overline{OR}$ high | | | 50 | ns | 2 x LSTTL + 20pF |
| SO ⌐ or SI ⌐ to $F_0$, $F_1$ invalid $T_{FIV}$ | | 40 | | ns | 2 x LSTTL + 20pF |
| SO ⌐ or SI ⌐ to $F_0$, $F_1$ valid $T_{SFV}$ | | 70 | | ns | 2 x LSTTL + 20pF |
| $\overline{MR}$ low | 300 | | | ns | |
| $\overline{MR}$ ⌙ to SI ⌐ | 250 | | | ns | |
| Setup $\overline{OR}$, to SI ⌐ | 20 | | | ns | $\overline{MR}$ low } |
| Setup DI0-8 to SI ⌐ | 20 | | | ns | $\overline{MR}$ low } Programming |
| Hold $\overline{OR}$, PE to SI ⌐ | | | 0 | ns | $\overline{MR}$ low } mode |
| Hold DI0-8 to SI ⌐ | | | 0 | ns | $\overline{MR}$ low } |
| $\overline{OE}$ ⌐ DO ⌒ z (See Note 3) | | | 20 | ns | 2 x LSTTL + 20pF |
| $\overline{OE}$ ⌐ DO ⌒ z | | | 20 | ns | 2 x LSTTL + 20pF |
| $\overline{OE}$ ⌙ DO z ⌒ | | | 20 | ns | 2 x LSTTL + 20pF |
| $\overline{OE}$ ⌙ DO z ⌒ | | | 20 | ns | 2 x LSTTL + 20pF |
| Power up to $\overline{MR}$ ⌙ | 2 | | | μs | Vcc = 4.25V min. |

## ABSOLUTE MAXIMUM RATINGS (See Note 1)

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5 to 7.0V |
| Input voltage $V_{IN}$ | -0.9 to Vcc +9V |
| Output voltage $V_{OUT}$ | -0.9 to Vcc +0.9V |
| Clamp diode current per pin Ik (See Note 2) | ±18mA |
| Static discharge voltage | |
| Storage temperature Ts | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -40°C to +85°C |
| Package power dissipation | |
| DG | 2200mW |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. 'z' denotes high impedance state.

# MV61903

## 1K x 9 PARITY FIFO

The MV61903 is one of a new generation of RAM-based FIFOs designed for ease of use. The MV61903 features user-programmable even or odd parity generation and checking circuitry, and an unencoded parity error flag.

The MV61903 also has a user-programmable flag (DIPSTICK™) which defaults to a conventional 'half-full' flag on power-up.

The FIFO has input and output registers and a truly asynchronous 3-state output enable to simplify interfacing.

Larger FIFO stores can be constructed by cascading parts in depth or width. In addition the MV61903 can be cascaded in such a way as to increase its speed. Two 10MHz MV61903s can be used to create a 20MHz 2K x 9 PARITY FIFO structure.

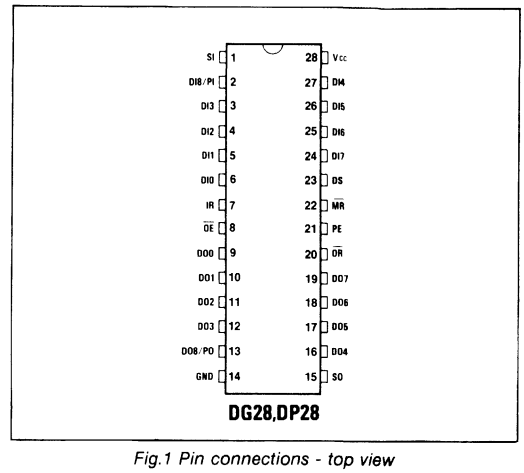



*Fig.1 Pin connections - top view*

### FEATURES

- 10MHz 1K Word x 9-bit FIFO
- On-Chip Parity Generation and Checking Circuitry
- User Programmable Flag (DIPSTICK)
- Parity Error Flag
- Cascadable in Width, Depth and Speed
- Input and Output Registers
- Asynchronous Output Enable
- 2-micron CMOS
- Power Dissipation 250mW
- Operating Temperature Range -40°C to +85°C

### APPLICATIONS

- Parity Protected, Asynchronous, Data Communication
- Disk or Tape Interfaces
- Printer Buffers
- User Programmable Delay Lines

### ASSOCIATED PRODUCTS

**MV61902** 1K x 9 DIPSTICK FIFO
**MV66030** 64 x 9 25MHz FIFO
**MV66401-4** 64 x 4/5 25MHz FIFOs

### ORDERING INFORMATION

**MV61903DG** (Commercial - ceramic DIL package)
**MV61903DP** (Commercial - plastic DIL package)

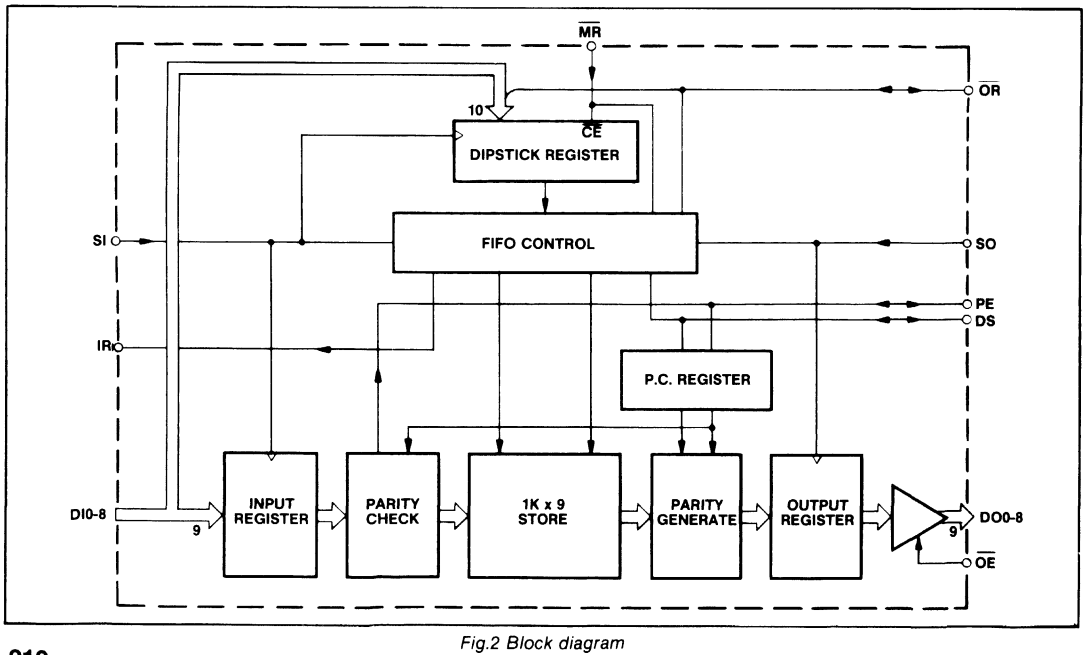



*Fig.2 Block diagram*

## PIN DESCRIPTIONS

| Symbol | Pin No. | Description |
|---|---|---|
| SI | 1 | **Shift in** The SI input is used to load data into the FIFO. On the rising edge of SI, the data present on the DI port is loaded into the input register and the write cycle that places the data within the store is initiated. During programming, the SI input is used to load data into the DIPSTICK Register and Parity Control Register. |
| SO | 15 | **Shift out** The SO input is used to clock data out from the FIFO. On the rising edge of SO, the data currently read from the store is loaded into the output register and the read cycle that reads the next output from the store is initiated. |
| IR | 7 | **Input ready** The IR flag indicates that the FIFO is ready to receive another input. After a rising edge of SI, IR will go low for the period required to write the new data into the store. Should IR remain low for more than the duration of one cycle the FIFO is full. |
| $\overline{OR}$ | 20 | **Output ready** The $\overline{OR}$ flag indicates that the FIFO is ready to output new data. After a rising edge of SO, $\overline{OR}$ will go high for the period required to read new data from the store. Should $\overline{OR}$ remain high for more than the duration of one cycle the FIFO is empty. During programming the $\overline{OR}$ output acts as a one bit input to LSB of the 10-bit DIPSTICK Register. |
| DI | 6,5,4, 3,27,26, 25,24,2 | **Data Input** DI0-8 is the 9-bit data input to the FIFO. This input is internally registered, hence input data may be removed at any time after the rising edge of SI. During programming of DIPSTICK the DI input is the 9 MSBs input to the DIPSTICK Register. When Parity Generation is enabled, the DI0-7 inputs are used as the inputs to the Parity Generator, DI8 is treated as a Parity Input (PI). |
| DO | 9,10,11, 12,16,17, 18,19,13 | **Data output** DO0-8 is the 9-bit data output from the FIFO. This output is internally registered, hence the output data will not change until shortly after the rising edge of SO. When Parity Generation is enabled, the Parity bit replaces the DO8 bit of the output, DO8 is treated as the Parity Output (PO). |
| $\overline{MR}$ | 22 | **Master reset** The $\overline{MR}$ input to the FIFO performs two functions:<br>1. Resetting the FIFO to an empty state;<br>2. Enabling the DIPSTICK Register and the Parity Control Register Clocks and causing $\overline{OR}$, PE and DS to become inputs to the 10th bit of the DIPSTICK Register and the Parity Control Register, respectively. |
| $\overline{OE}$ | 8 | **Output enable** The $\overline{OE}$ input when high forces the DO0-8 outputs into a high impedance state. |
| PE | 21 | **Parity error** The PE output changes after the rising edge of SI. The PE flag indicates, when high, that the data loaded into the FIFO on the most recent rising edge of SI contained a Parity error.<br>During programming the PE output acts as a one-bit input to the Parity Control Register, and when set high selects Odd Parity. |
| DS | 22 | **DIPSTICK** The DS output changes when the last of SI or SO to go high finally goes low - see Section DS in Functional Description. The DS output is active high. During Programming the DS output acts as a one-bit input to the Parity Control Register and when set high enables the Parity Generation Circuitry. |

## FUNCTIONAL DESCRIPTION

The MV61903 contains four main blocks; the 1K x 9 STORE and associated registers, the FIFO controller, the DIPSTICK Register and the Parity circuitry.

### 1K x 9 STORE

The 1K x 9 STORE contains the data written into the FIFO. It accepts data from the input register, sources data to the output register, and is controlled by two pointers supplied by the FIFO controller.

### FIFO Controller

The FIFO controller accepts the SI, SO and MR inputs and generates the IR, OR and DS outputs and pointers for the store.

### SI and SO

SI and SO are the shift in and shift out signals to the FIFO. These inputs may be synchronous or asynchronous to one another. There are no restrictions on SI and SO with respect to each other. There is no maximum limit on SI or SO high or low periods, the only restriction being minimum SI or SO high or low periods which determine the cycle time (see Section DS).

The FIFO controller calculates the correct pointer outputs for the store, according to the sequence of SI or SO pulses.

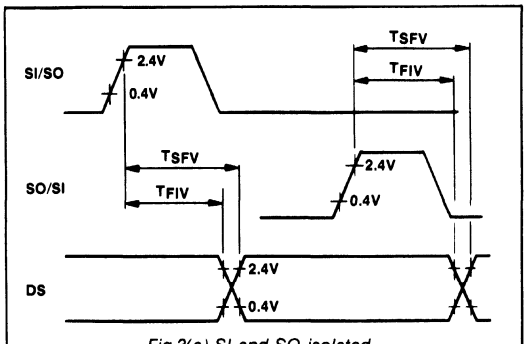



*Fig.3(a) SI and SO isolated*

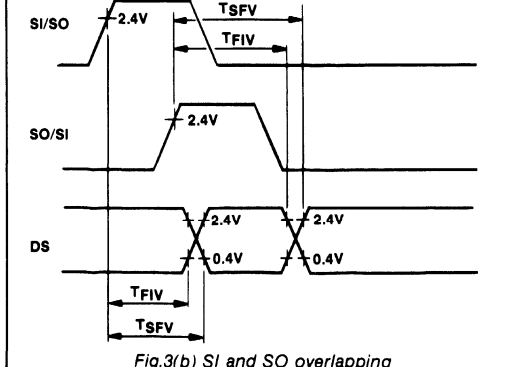



*Fig.3(b) SI and SO overlapping*

*Fig.3 DS timing for asynchronous SI/SO*

### $\overline{MR}$

When low, the $\overline{MR}$ input to the FIFO controller resets both pointers to zero and loads the output register with zeros. Any SI or SO pulses that occur while $\overline{MR}$ is low will not change the state of the FIFO controller, the FIFO will remain empty.

### IR and $\overline{OR}$

Input ready and output ready are generated by the FIFO controller, dependent upon the state of SI and SO.

While SI is high, IR is held low. IR can only go high if SI is low and the FIFO is ready to receive new inputs.

$\overline{OR}$ can only go low if the FIFO is ready to output new data. It is not dependent upon the state of SO. A rising edge on SO will cause $\overline{OR}$ to go high for a period equal to the time required to read new data from the store.

### DS

The DS output changes according to the state of SI and SO.

The two usual cases for asynchronous (isolated or ovelapping) SI and SO pulses are shown in Fig.3, the start of the invalid period DS being indicated by $T_{FIV}$.

In either case, the DS flag changes a period equal to $T_{FIV}$ after the rising edge of SI or SO.

The flexibility of SI and SO timing relationships allows a further relationship for asynchronous SI and SO pulses, as shown in Fig.4 with the invalid DS period indicated.

In this case, either SI or SO is held high, while the remaining input is toggled. The DS flag changes after each rising edge of either input.

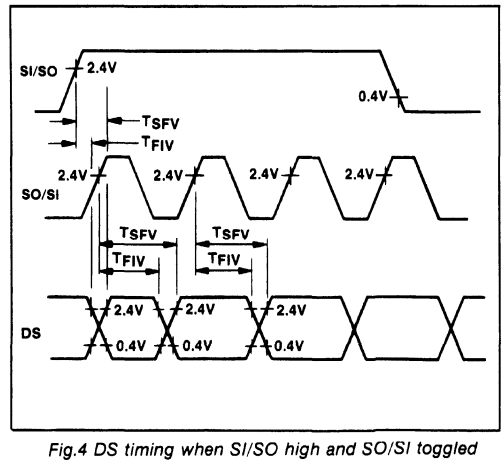



*Fig.4 DS timing when SI/SO high and SO/SI toggled*

## DIPSTICK Register

The DIPSTICK Register contains a value equal to the number of words in the store at which the DIPSTICK flag will become active.

The DIPSTICK Register defaults to a value of 512 on power up, and if not reprogrammed will continue to become active at this value, fulfilling the function of a 'half-full' flag.

The DIPSTICK Register may be reprogrammed while $\overline{MR}$ is active. A low on $\overline{MR}$ does not change the contents of the DIPSTICK Register, but enables the DIPSTICK Register clock. Any rising edge on SI while $\overline{MR}$ is low will cause a 10-bit word to be loaded into the DIPSTICK Register.

The 10-bit word is derived from two sources: the DI0-8 inputs and the $\overline{OR}$ output ($\overline{OR}$ acts as an input when $\overline{MR}$ is low).

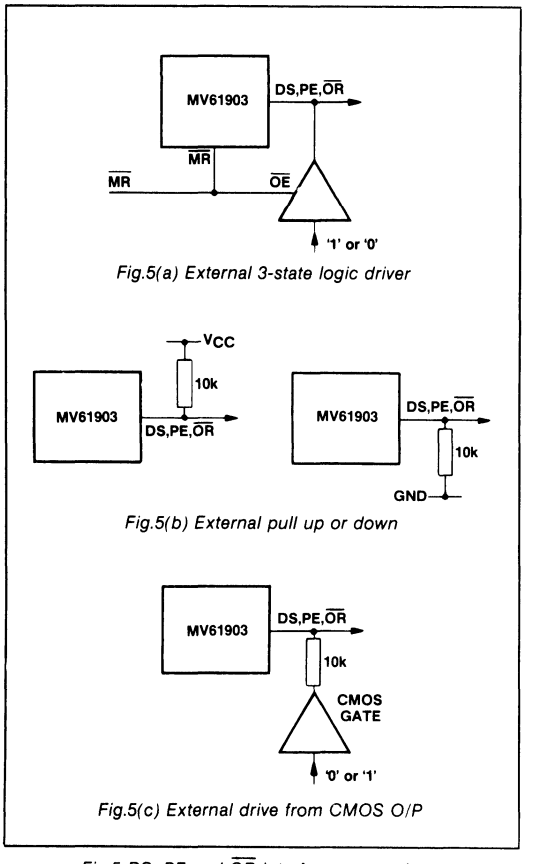



*Fig.5(a) External 3-state logic driver*

*Fig.5(b) External pull up or down*

*Fig.5(c) External drive from CMOS O/P*

*Fig.5 DS, PE and $\overline{OR}$ interface connections*

The nine inputs derived from the DI0-8 inputs comprise the 9 most significant bits of the DIPSTICK Register, DI8 being the most significant bit. The bit derived from $\overline{OR}$ input forms the least significant bit of the DIPSTICK Register.

The $\overline{OR}$ input may be driven high or low by external logic while $\overline{MR}$ is low. This external logic must adopt a high impedance state while $\overline{MR}$ is high (Fig.5(a)) or be CMOS, and be connected to $\overline{OR}$ via a 10kΩ series resistor (see Fig.5(c)).

## PARITY CIRCUITRY

The Parity circuitry consists of three main elements, the Parity Control Register, the Parity Checking Circuit and the Parity Generation Circuit.

### Parity Control Register

The Parity Control Register is a 2-bit register that is programmed at the same time as the DIPSTICK Register via the DS and PE ports.

Both DS and PE outputs become inputs when $\overline{MR}$ is low. The DS input will set the Parity Generation bit of the Parity Control Register when high, and will reset it when low. The PE input will set the Parity sign bit of the Parity Control Register when high and will reset it when low. A low on $\overline{MR}$ does not change the contents of the Parity Control Register, but enables the Parity Control Register Clock. Any rising edge of SI while MR is low will cause a two-bit word to be loaded into the Parity Control Register.

On power-up the Parity Control Register defaults to a setting that disables the Parity Generation circuitry, and selects ODD Parity checking. This corresponds to a low setting of the Parity generation bit of the Parity Control Register, and a high setting of the Parity sign bit as shown in Table 1.

*Table 1 PE and DS settings during programming*

| PE | DS | Function |
|---|---|---|
| 0 | 0 | EVEN Parity Generation Disabled |
| 0 | 1 | EVEN Parity Generation Enabled |
| 1 | 0 | ODD Parity Generation Disabled |
| 1 | 1 | ODD Parity Generation Enabled |

The PE and DS inputs may be driven high or low by external logic while $\overline{MR}$ is low. This external logic must adopt a high impedance state whilst $\overline{MR}$ is high (Fig.5(a)) or be CMOS and be connected to $\overline{OR}$ via a 10kΩ series resistor (see Fig.5(c)).

### Parity Checking Circuit

The Parity Checking Circuit selects the Parity Sign (EVEN, ODD) by the Parity Control Register sign bit setting, and checks all incoming data for Parity errors. Any detected error will cause the PE output to go high shortly after the rising edge of SI that loads the data containing the error into the FIFO.

### Parity Generation Circuit

The Parity Generation Circuit is enabled by the Parity Generation bit of the Parity Control Register, and selects the Parity sign (EVEN, ODD) according to the Parity Control Register sign bit setting.

The Parity Generation Circuit generates the correct bit for the DI0-7 inputs to the FIFO (after they have passed through the store), and if parity generation is enabled, it inserts this correct parity bit into the DO8 bits of the DO0-8 output.

## CASCADING

The MV61903 Parity FIFO will cascade in width, depth or speed.

### Width

Multiple MV61903 Parity FIFOs may be configured as one 1K x (n x 9) FIFO with n independent DIPSTICK flags. See Fig.6 for 1K x 27 example.

### Depth

Multiple MV61903 Parity FIFOs may be configured as one nK x 9 FIFO, see Fig.7 for 3K x 9 example.

In this configuration, each DIPSTICK flag operates within one of the 1K blocks of the 3K total store. On power up, these flags will default to detect 512 words, 1536 words and 2560 words in the store.

When cascading and generating parity, the First FIFO in the chain must be programmed to generate, the remainder to check parity.

These expansion techniques may be combined to allow expansion in width and depth with a corresponding increase in the number of available flags.

### Speed

The MV61903 Parity FIFO may be cascaded to increase speed and depth at the same time. Fig.8 illustrates a 2K x 9 20MHz FIFO example.

In this example the Input data is loaded into alternate FIFOs and clocked out of alternate FIFOs. MR selects the top FIFO as the destination of the first word to be written into the store, consequently this FIFO contains the 1st, 3rd, 5th (odd numbered) words written into the store and hence, its DIPSTICK flag can only detect ODD values of store contents. Similarly, the bottom FIFO can only detect the EVEN value of the number of words within the store.

There is a capacity for 2048 words, each DIPSTICK flag has 1024 values, and these are interlaced to cover all 2048 possible values.

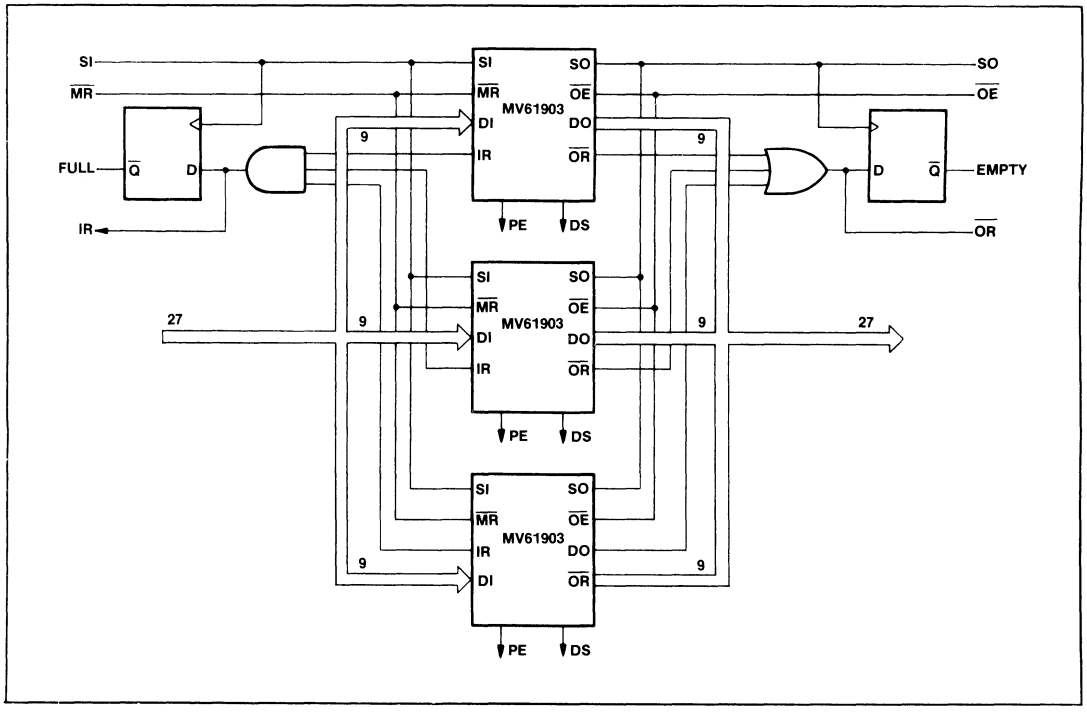



*Fig.6 1K x 27 10MHz FIFO with FULL, EMPTY and 3 DIPSTICK flags*

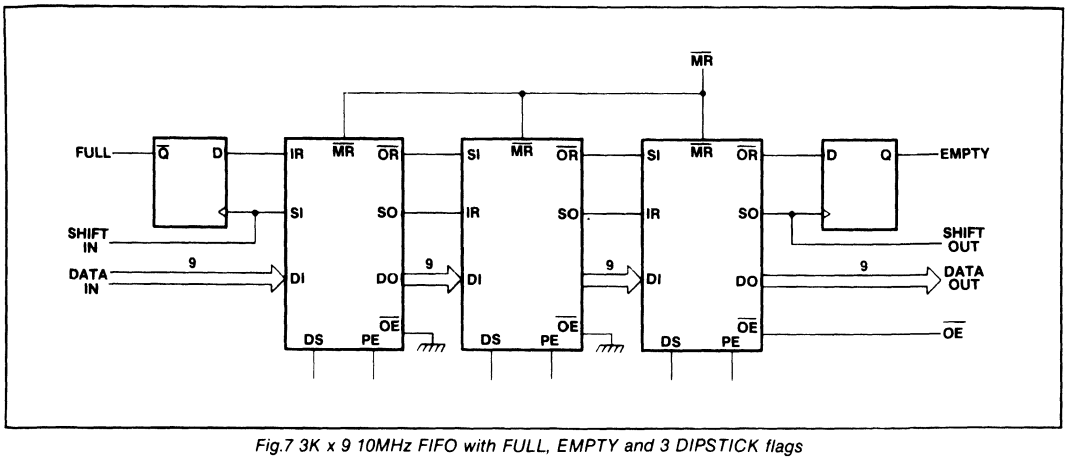



*Fig.7 3K x 9 10MHz FIFO with FULL, EMPTY and 3 DIPSTICK flags*

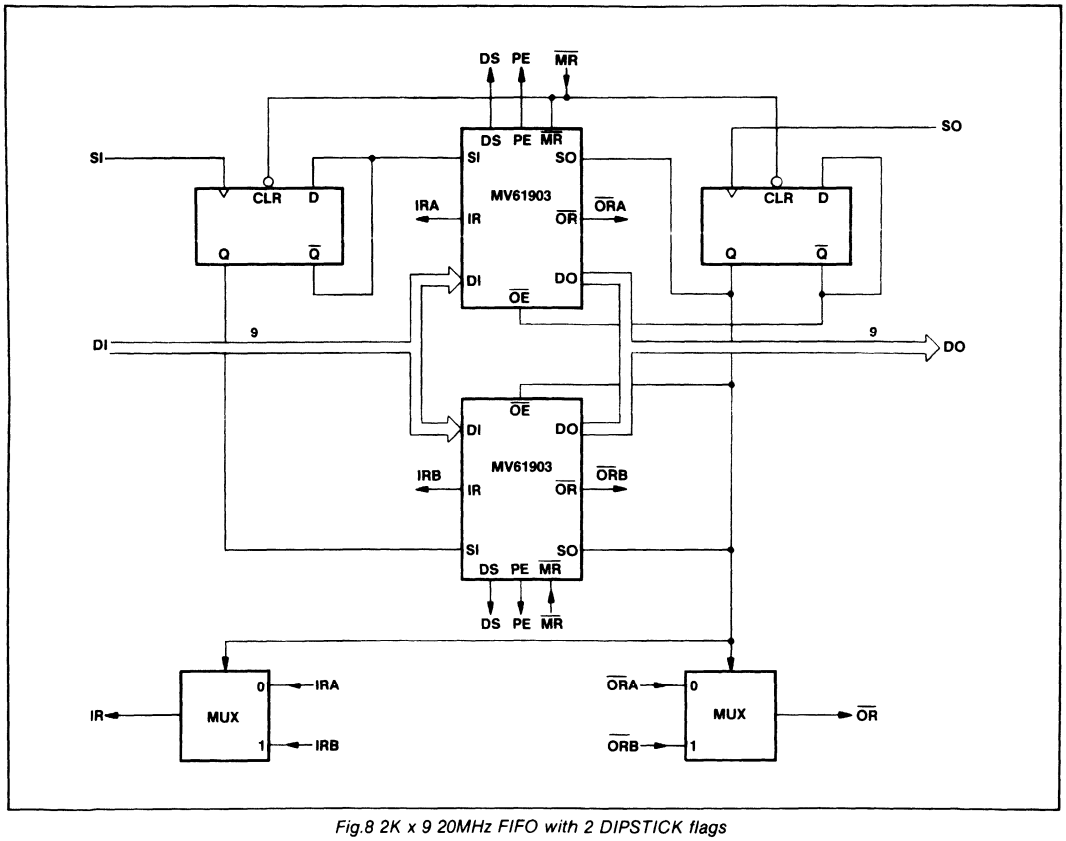



*Fig.8 2K x 9 20MHz FIFO with 2 DIPSTICK flags*

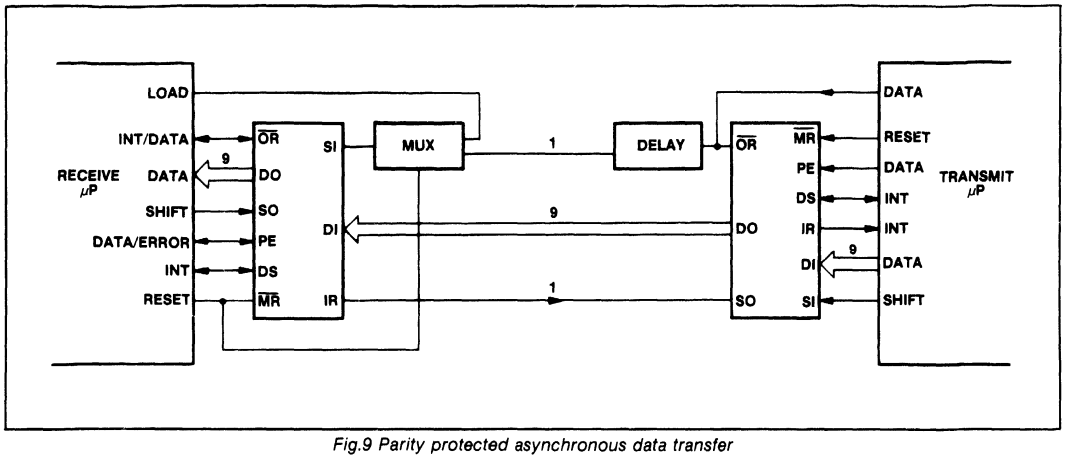



*Fig.9 Parity protected asynchronous data transfer*

## TYPICAL APPLICATIONS

### Parity Protected Asynchronous Data Transfer

Fig.9 illustrates an interconnection of two MV61903 FIFOs configured to form an asynchronous Parity Protected Data Communication link.

The MV61903s are programmed directly from the Transmit and Receive microprocessors to set the Parity sign (EVEN, ODD) and enable Parity Generation on the Transmit side. The PE flag of the receiving FIFO acts as an interrupt to indicate that the FIFO has space for a new block of data, or has received a new block of data respectively. These interrupts may be used to initiate DMA data transfer routines.

The delay element is required to ensure that the set up time on the receiving FIFO is satisfied before SI is taken high. This delay will vary according to the implementation.

During programming, the link between the Transmit FIFO OR and the Receive FIFO SI must be broken to allow the receive microprocessor to program the receive FIFO.

### 10MHz User Programmable Delay Line

The MV61903 may be configured as a user programmable delay line.

In this application, SI and SO are toggled synchronously, and the DIPSTICK Register is used to store the desired delay.

To build a 10MHz 1K x 9 delay line requires one MV61903 and one 2-input AND gate. See Fig.10.

An MR empties the FIFO and allows the DIPSTICK Register to be programmed with the desired delay. Subsequent clock cycles will load data into the FIFO, but no SO pulses will occur until the DIPSTICK flag becomes active as decoded by the 2-input AND gate.

Once DIPSTICK has become active, every clock pulse will cause an SI and SO to the FIFO, resulting in no net change in the FIFOs contents, and leaving DIPSTICK, and hence SO, enabled.

Each CLK cycle will cause a word to be written into and read from the FIFO, implementing the operation of a delay line.

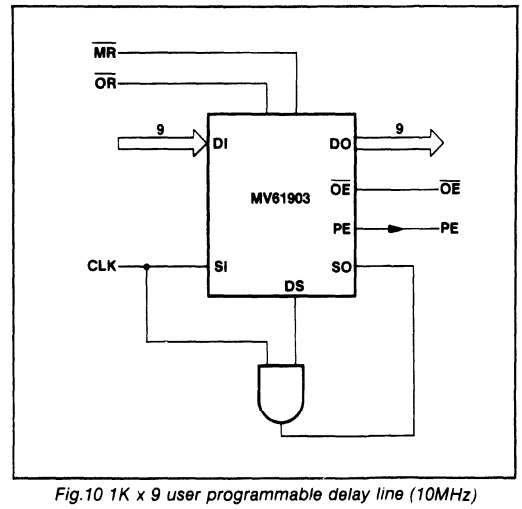



*Fig.10 1K x 9 user programmable delay line (10MHz)*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = -40°C to +85°C, $V_{CC}$ = 5.0V ± 10%, GND = 0V

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output high voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = 8mA |
| Output low voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = -8mA |
| Input high voltage | $V_{IH}$ | 2.0 | | | V | |
| Input low voltage | $V_{IL}$ | | | 0.8 | V | |
| Input leakage current | $V_{IL}$ | -10 | | 10 | μA | GND ≤ $V_{IN}$ ≤ $V_{CC}$ |
| Vcc current | $I_{CC}$ | | | 50 | mA | $T_{amb}$ -40°C to +85°C |
| Output leakage current | $I_{OZ}$ | -50 | | 50 | μA | GND ≤ $V_{OUT}$ ≤ $V_{CC}$ = $V_{CC}$ max. |
| Output short CCT current (See Note 2) | $I_{OS}$ | 15 | | 80 | mA | $V_{CC}$ = max. |

**Switching Characteristics**

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| SO or SI low | 50 | | | ns | |
| SO or SI high | 25 | | | ns | |
| Setup DI0-8 to SI⌐ | 20 | | | ns | |
| Hold DI0-8 to SI ⌐ | | | 0 | ns | |
| SO to DO0-8 valid | | | 25 | ns | 2 x LSTTL + 20pF |
| SI⌐ to IR⌐ | | | 20 | ns | 2 x LSTTL + 20pF |
| SI⌐ to IR⌐ - min SI pulse | | | 75 | ns | 2 x LSTTL + 20pF |
| SO⌐ to $\overline{OR}$ ⌐ | | | 50 | ns | 2 x LSTTL + 20pF |
| SO⌐ to $\overline{OR}$ ⌐ | | 30 | | ns | SO min pulse width |
| $\overline{OR}$ high | | | 50 | ns | 2 x LSTTL + 20pF |
| SO⌐ or SI⌐ to DS invalid $T_{FIV}$ | | 40 | | ns | 2 x LSTTL + 20pF |
| SO⌐ or SI⌐ to DS valid $T_{SFV}$ | | 70 | | ns | 2 x LSTTL + 20pF |
| SI⌐ to PE valid | | | 20 | ns | 2 x LSTTL + 20pF |
| $\overline{MR}$ low | 300 | | | ns | |
| $\overline{MR}$ ⌐ to SI ⌐ | 250 | | | ns | |
| Setup $\overline{OR}$, DS, to SI⌐ | 20 | | | ns | $\overline{MR}$ low |
| Setup DI0-8 to SI⌐ | 20 | | | ns | $\overline{MR}$ low } Programming |
| Hold $\overline{OR}$, DS, PE to SI⌐ | | | 0 | ns | $\overline{MR}$ low } mode |
| Hold DI0-8 to SI⌐ | | | 0 | ns | $\overline{MR}$ low |
| $\overline{OE}$ ⌐ DO ⌐ z (See Note 3) | | | 20 | ns | 2 x LSTTL + 20pF |
| $\overline{OE}$ ⌐ DO ⌐ z | | | 20 | ns | 2 x LSTTL + 20pF |
| $\overline{OE}$ ⌐ DO z ⌐ | | | 20 | ns | 2 x LSTTL + 20pF |
| $\overline{OE}$ ⌐ DO z ⌐ | | | 20 | ns | 2 x LSTTL + 20pF |
| Power up to $\overline{MR}$ ⌐ | 2 | | | μs | $V_{CC}$ = 4.25V min. |

## ABSOLUTE MAXIMUM RATINGS (See Note 1)

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5 to 7.0V |
| Input voltage $V_{IN}$ | -0.9 to $V_{CC}$ +9V |
| Output voltage $V_{OUT}$ | -0.9 to $V_{CC}$ +0.9V |
| Clamp diode current per pin Ik (See Note 2) | ±18mA |
| Static discharge voltage | |
| Storage temperature Ts | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -40°C to +85°C |
| Package power dissipation DG | 2200mW |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. 'z' denotes high impedance state.

# SP9001C

## FOUR CHANNEL MAGNETIC BUBBLE SENSE AMPLIFIER

### GENERAL DESCRIPTION

The SP9001C is an integrated circuit designed to detect low level pulses. The circuit is organised with four differential input amplifiers which are multiplexed to give two latched tristate TTL outputs. A variable threshold input is also provided to vary input sensitivity. Internal AC coupling is used to remove DC offset present at the inputs. Although designed primarily for magnetic bubble memory systems, this device can be used in other applications where the detection of low-level pulses is required.

### FEATURES

- Four Multiplexed Differential Input Channels
- Two Tri-State TTL Outputs
- Adjustable Input Sensitivity 2-10mV
- ±2V Common Mode Range
- Pulse Detection in Presence of ±100mV DC Offset
- TTL Compatible Logic Inputs

### APPLICATIONS

- Sense Amplifiers For Magnetic Bubble Memories
- Low Level Pulse Detection

### ORDERING INFORMATION

**SP9001C DC** (Commercial Ceramic)
**SP9001MC DC** (Military Ceramic)

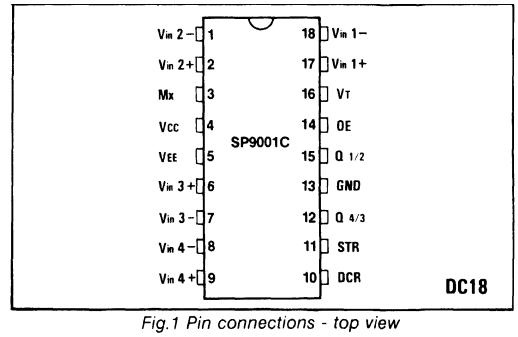



*Fig.1 Pin connections - top view*

### PIN NAMES

| | |
|---|---|
| Mx | Multiplex |
| DCR | DC restore |
| STR | Strobe |
| OE | Output enable |
| $V_T$ | Threshold set |
| $V_{EE}$ | Negative voltage supply |
| $V_{CC}$ | Positive voltage supply |
| $V_{in}$ | Input |
| $Q_{1/2}$ | Output-channels 1 and 2 |
| $Q_{4/3}$ | Output-channels 4 and 3 |

Logic '0' on OE enables tristate outputs
Logic '1' on Mx selects channels 1 and 4

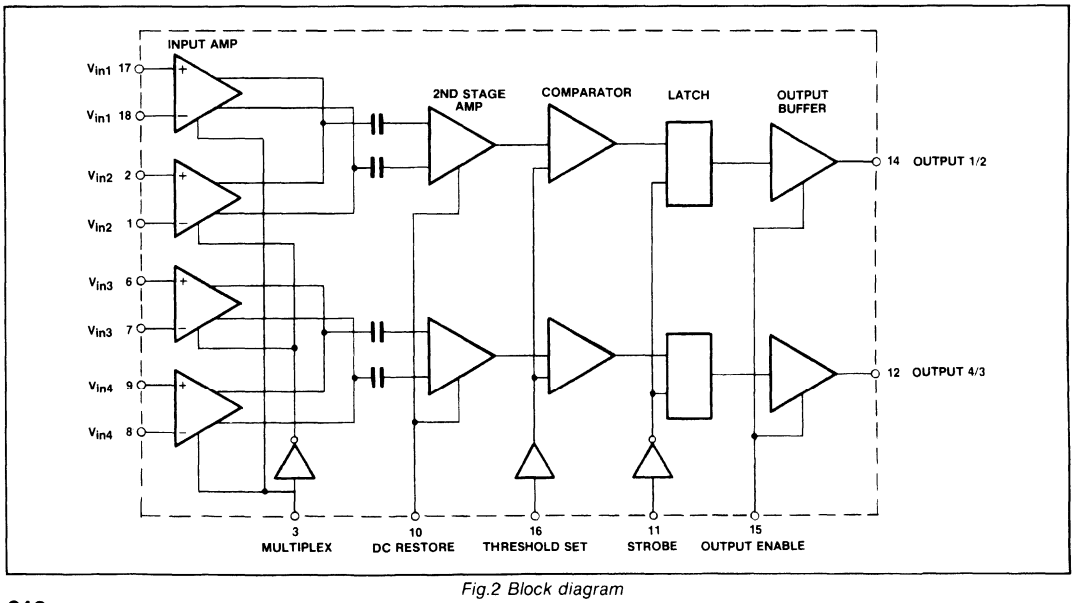



*Fig.2 Block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{CC}$ = +5V $V_{EE}$ = -5V $T_{amb}$ = 25°C

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 40 | 50 | mA | |
| Negative supply current | $I_{EE}$ | | -20 | -30 | mA | |
| Logic input current - low | $I_{IL}$ | | | -1.6 | mA | $V_{IL}$ = 0.4V See Note 1 |
| Logic input current - high | $I_{IH}$ | | | 40 | $\mu$A | $V_{IH}$ = 2.4V See Note 1 |
| Output voltage - low | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 16mA See Note 2 |
| Output voltage - high | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -5mA See Note 2 |
| Offstate output current ($V_O$ = 0.4V, $V_O$ = 2.4) | $I_{OZ}$ | | | 40 | $\mu$A | See Note 2 |
| Threshold set input range | $V_T$ | 1 | | 4.5 | V | |
| Threshold set input current ($V_T$ = 4.5V) | $I_{IT}$ | | | 10 | $\mu$A | |
| Threshold set voltage | $V_T$ | 3.25 | 3.65 | 4.10 | V | I/P sensitivity = 10mV |
| Threshold variation with sensitivity | $\Delta V_T/\Delta V_{in}$ | 0.230 | 0.255 | 0.290 | V/mV | |
| Input common mode range | CMR | | | ±2 | V | See Note 4 |
| Input differential DC offset | $V_{OS}$ | | | ±100 | mV | See Notes 3,4 |
| Input bias current | $I_{in}$ | | | 10 | $\mu$A | See Note 4 |
| Input offset current | $\Delta I_{in}$ | | | 1 | $\mu$A | See Note 4 |
| Input impedance | $R_{in}$ | 10 | | | kΩ | See Note 4 |
| Input threshold range | $V_{in}$ | 2 | | 10 | mV | See Note 4 |
| Channel/channel threshold variation | $\Delta V_{in}$ | | | ±0.5 | mV | |
| Variation threshold with temperature | $\Delta V_{in}/\Delta T$ | | -10 | | $\mu$V/°C | |
| Variation threshold with supply (positive) | $\Delta V_{in}/\Delta V_{CC}$ | | -0.5 | | mV/V | |
| Variation threshold with supply (negative) | $\Delta V_{in}/V_{EE}$ | | -0.8 | -1.1 | mV/V | |
| Input amplifier bandwidth | B | | 7 | | MHz | |
| Multiplex set up time | $t_1$ | 20 | | | ns | See Note 5 |
| DC restore-input set up time | $t_2$ | 50 | | 5000 | ns | See Note 5 |
| input-strobe set up time | $t_3$ | 20 | | | ns | See Note 5 |
| Strobe/output delay (output low) | $t_4$ | | 35 | 65 | ns | Fig.5. See Note 5 |
| Strobe/output delay (output high) | $t_5$ | | 25 | 50 | ns | See Note 5 |
| Output rise time | $t_6$ | | 15 | 25 | ns | See Note 5 |
| Output fall time | $t_7$ | | 15 | 25 | ns | See Note 5 |
| Output enable/output delay (low) | $t_8$ | | 20 | 50 | ns | Fig.6. See Note 5 |
| Output enable/output delay (high) | $t_9$ | | 15 | 25 | ns | Fig.6. See Note 5 |

**NOTES**
1. Each logic input.
2. Each output.
3. The device will detect a small pulse at the input in the presence of a DC differential offset applied at the input (see Fig.12)
4. Each input channel.
5. Timing limits guaranteed but not tested.

## RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply voltage | $V_{CC}$ | 4.5 | 5 | 5.5 | V | |
| Negative supply voltage | $V_{EE}$ | -5.5 | -5 | -4.5 | V | |
| Logic input voltage - low | $V_{IL}$ | | | 0.8 | V | See Note 1 |
| Logic input voltage - high | $V_{IH}$ | 2 | | | V | See Note 1 |
| Output current - low | $I_{OL}$ | | | 16 | mA | See Note 2 |
| Output current - high | $I_{OH}$ | | | -5 | mA | See Note 2 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage temperature | -65° C to 150° C |
| Operating temperature | -55° C to +110° C |
| Positive supply $V_{CC}$ | +7V |
| Negative supply $V_{EE}$ | -7V |
| Analogue input voltage | ±4V |
| Differential input voltage | ±3V |
| Logic input voltage | Min. -1.5V Max. $V_{CC}$ |
| Threshold input voltage | Min. -1.5V Max. $V_{CC}$ |

## CIRCUIT DESCRIPTION

A block diagram of the sense amplifier is shown in Fig.2. The circuit consists of four differential input stages which are multiplexed into two output channels each comprising a second stage amplifier, comparator, D-Type flip-flop and output buffer. AC coupling is employed between first and second stages enabling the device to accept relatively large DC offset voltages at the input. The DC restore input, when driven high, causes the second stage inputs to be clamped to zero volts. When the DC restore input is low the clamp is released and the input signals can pass to the second stage. The overall action of the clamp is to reference the differential input signal to zero whilst the clamp is closed. Hence the effective signal is the change in differential input signal from the time at which the clamp is opened, as shown in Fig.4.

The signal is amplified and then compared with the threshold voltage set by applying an external voltage to Pin 16 ($V_T$). The relationship between the actual threshold and the applied voltage is shown in Fig.8. The comparator decision is strobed into the edge triggered flip-flop on the positive edge of the strobe signal and fed into a TTL compatible tristate output stage.

The complete sequence of waveforms is shown in Figs. 5 and 6. Fig. 7 shows waveforms obtained in a typical magnetic bubble memory system application.

## OPERATING NOTES

The circuit operates with a small number of external components. These are required to set the necessary threshold voltage (which can be arranged, if required, to track the power supply voltage), or to compensate for sensitivity changes with temperature. It is recommended that the power supplies are well decoupled by connecting 0.1μF capacitors to ground, as close to the package as possible.

Since the device has a high sensitivity, care should be taken to avoid routing the inputs close to the DC restore, strobe and other logic signals, which might cause cross coupling and produce an incorrect decision.

The high impedance differential inputs add to the flexibility of the device, allowing a variety of input connections schemes to be used. DC offsets of up to 100mV can be tolerated at the input by virtue of the internal AC coupling, but the inputs should be maintained within the ±2 volts common mode range (see Fig.11). This enables the resistor bridge network, shown in Fig.12(a), to be used for low cost solutions. Larger DC offsets will require the inputs to be AC coupled, in which case external bias must be provided. The high input impedance will not unduly load the circuit to which it is connected.

The flexibility of the design of the input stage also allows the use of current sources or baluns as a bridge network (see Figs.12(b) and 12(c)).

If the multiplex facility is not required the multiplex input should be connected to either the positive supply or ground and the appropriate input channels used as convenient. Unused amplifier inputs should be connected to ground.

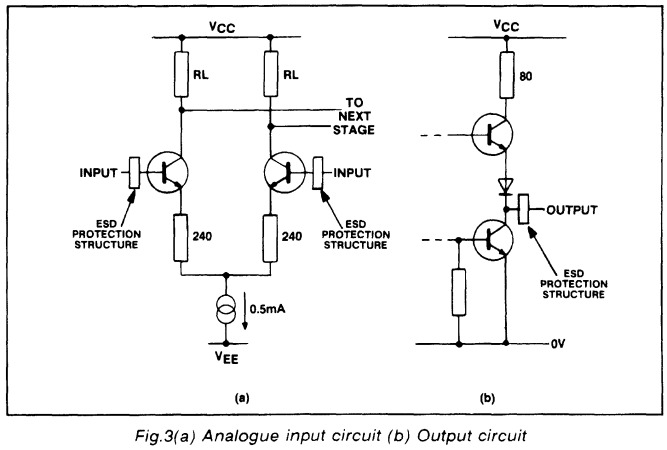



*Fig.3(a) Analogue input circuit (b) Output circuit*

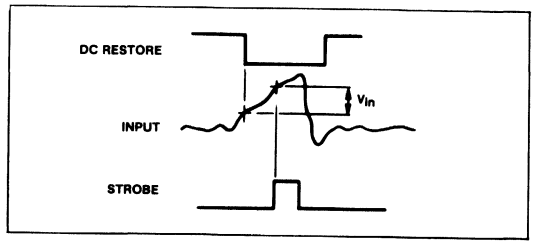



*Fig.4 DC restore timing*

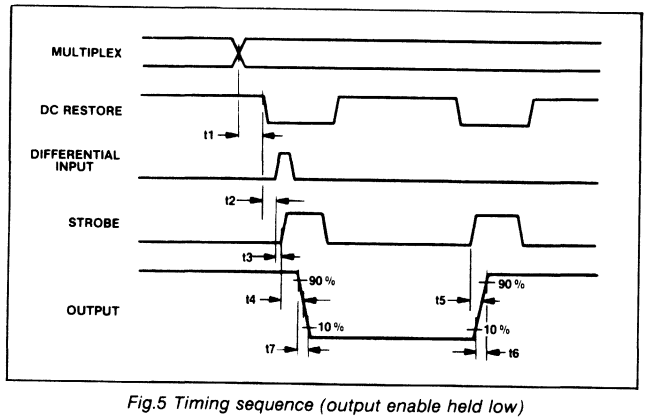



*Fig.5 Timing sequence (output enable held low)*

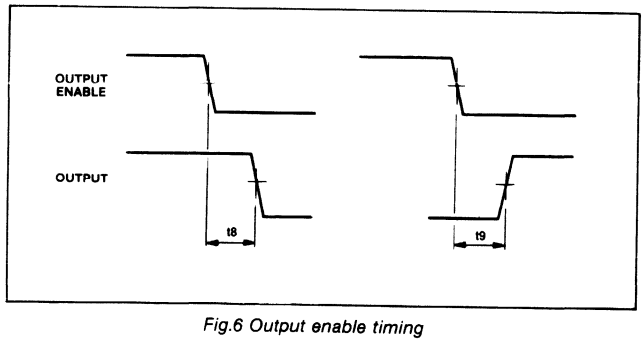



*Fig.6 Output enable timing*

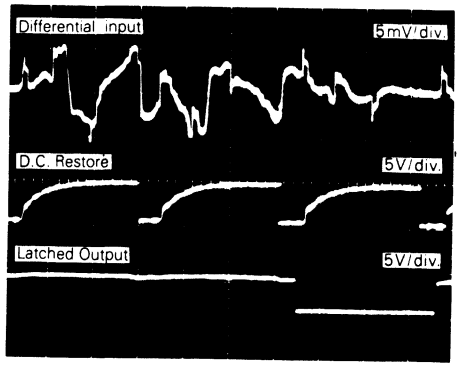



*Fig.7 Typical waveforms in Magnetic Bubble Memory System*

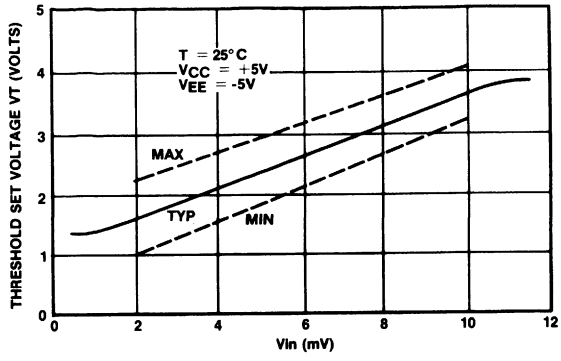



*Fig.8 Minimum threshold set voltage ($V_T$) vs input signal ($V_{in}$)*

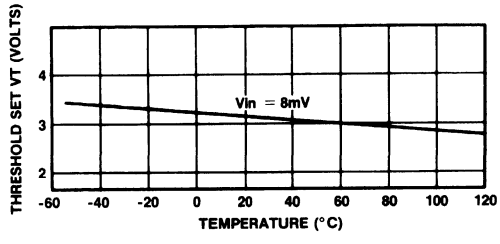



*Fig.9 Threshold set voltage vs temperature*

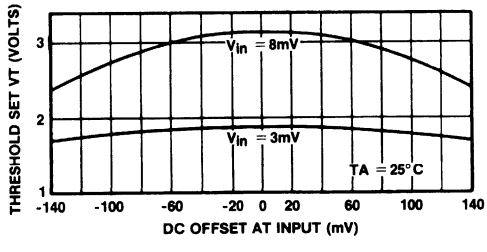



*Fig.10 Threshold set vs differential DC offset at input*

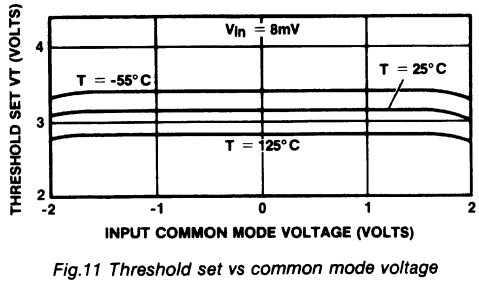



*Fig.11 Threshold set vs common mode voltage*

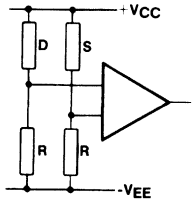



Fig.12(a)

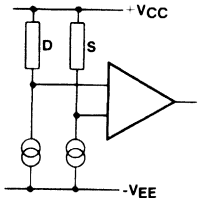



Fig.12(b)

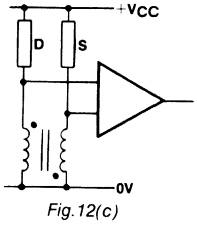



Fig.12(c)

**D = BUBBLE MEMORY DUMMY RESISTOR**
**S = BUBBLE MEMORY SENSE RESISTOR**

*Fig.12 Input stage configurations*

# Technical Data

## 4. High speed logic

# SP9131

## 520MHz ECL DUAL D FLIP-FLOP

The SP9131 Dual D type flip-flop is pin compatible with 10131, but has improved dynamic performance.

### FEATURES

- Guaranteed Operation at 520MHz
- Separate or Common Clock
- Independent Set and Reset Inputs
- Master Slave Operation
- -5.2V Supply
- Operating Temperature Range:
  -30°C to +85°C - Industrial
  -55°C to +125°C - Military
- ECL 10K Compatible
- Pin Compatible with MC10131/102131/105131/10H131 — But Faster

### ORDERING INFORMATION

**SP9131DG** (Industrial - Ceramic DIL package)
**SP9131BB DG** (Plessey High Reliability Ceramic DIL package)
**SP9131LC** (Industrial - LCC package)
**SP9131AC DG** (Military - Ceramic DIL package)

NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

### R-S TRUTH TABLE

| R | S | Qn + 1 |
|---|---|---|
| L | L | Qn |
| L | H | H |
| H | L | L |
| H | H | ND |

### CLOCKED TRUTH TABLE

| C | D | Qn + 1 |
|---|---|---|
| L | X | Qn |
| H | L | L |
| H | H | H |

X = Don't care
C = CE + CC
A clock H is a clock transition from a low to a high state.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\lvert V_{CC} - V_{EE} \rvert$ 8V |
| Input voltages | 0V to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

### THERMAL CHARACTERISTICS

| | |
|---|---|
| DG16 | $\theta_{JA}$ = 110°C/W |
| | $\theta_{JC}$ = 33°C/W |
| LC20 | $\theta_{JA}$ = 73°C/W |
| | $\theta_{JC}$ = 22°C/W |

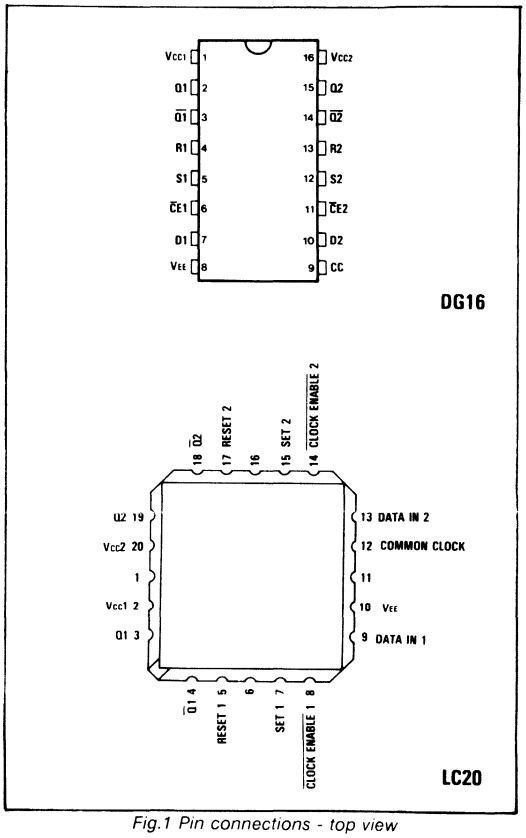



*Fig.1 Pin connections - top view*

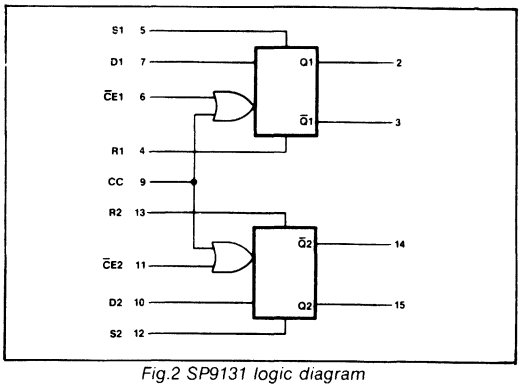



*Fig.2 SP9131 logic diagram*

## ELECTRICAL CHARACTERISTICS

The SP9131 circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

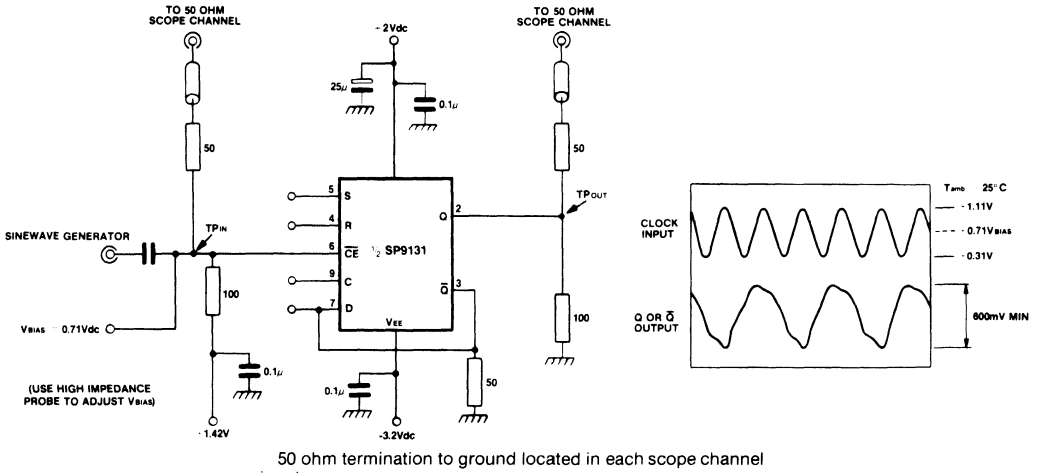
| Test temp. | TEST VOLTAGES (V) $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ |
|---|---|---|---|---|---|
| -30° C | -0.89 | -1.89 | -1.205 | -1.500 | -5.2 |
| +25° C | -0.81 | -1.85 | -1.105 | -1.475 | -5.2 |
| +85° C | -0.70 | -1.825 | -1.035 | -1.440 | -5.2 |

| Characteristic | Symbol | Pin under test | Test limits -30° C Min. | -30° C Max. | +25° C Min. | +25° C Typ. | +25° C Max. | +85° C Min. | +85° C Max. | Unit | VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ | $V_{CC}$ (GND) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power supply current | $I_E$ | 8 | - | 95 | - | 70 | 87 | - | 95 | mA | - | - | - | - | 8 | 1.16 |
| Input current | $I_{inH}$ | 4 | - | - | - | - | 600 | - | - | μA | 4 | - | - | - | 8 | 1.16 |
| | | 5 | - | - | - | - | 600 | - | - | | 5 | - | - | - | | |
| | | 6 | - | - | - | | 300 | - | - | | 6 | - | - | - | | |
| | | 7 | - | - | - | - | 300 | - | - | | 7 | - | - | - | | |
| | | 9 | - | - | - | - | 420 | - | - | | 9 | - | - | - | | |
| Input leakage current | $I_{inL}$ | 4,5 (Note 1) | - | - | 0.5 | - | - | - | - | μA | - | - | - | - | 8 | 1.16 |
| | | 6,7,9 (Note 1) | - | - | 0.5 | - | - | - | - | μA | - | - | - | - | 8 | 1.16 |
| Logic '1' output voltage | $V_{OH}$ | 2 | -1.06 | -0.89 | -0.96 | - | -0.81 | -0.89 | -0.70 | V | 5 | - | - | - | 8 | 1.16 |
| | | 2 (Note 2) | -1.06 | -0.89 | -0.96 | - | 0.81 | -0.89 | -0.70 | V | 7 | - | - | - | 8 | 1.16 |
| Logic '0' output voltage | $V_{OL}$ | 3 | -1.89 | -1.675 | -1.85 | - | -1.65 | -1.825 | -1.615 | V | 5 | - | - | - | 8 | 1.16 |
| | | 3 (Note 2) | -1.89 | -1.675 | -1.85 | - | -1.65 | -1.825 | -1.615 | V | 7 | - | - | - | 8 | 1.16 |
| Logic '1' threshold voltage | $V_{OHA}$ | 2 | -1.08 | - | -0.98 | - | - | -0.91 | - | V | - | - | 5 | - | 8 | 1.16 |
| | | 2 (Note 2) | -1.08 | - | -0.98 | - | - | -0.91 | - | V | - | - | 7 | 9 | 8 | 1.16 |
| Logic '0' threshold voltage | $V_{OLA}$ | 3 | - | -1.655 | - | - | -1.63 | - | -1.595 | V | - | - | 5 | - | 8 | 1.16 |
| | | 3 (Note 2) | - | -1.655 | - | - | -1.63 | - | -1.595 | V | - | - | 7 | 9 | 8 | 1.16 |
| **SWITCHING TIMES** | | | | | | | | | | | +1.11V | | Pulse in | Pulse out | -3.2V | +2.0V |
| Clock input propagation delay | $t_{9\,+2-}$ | 2 | 0.5 | 1.8 | 0.5 | 1.0 | 1.8 | 0.6 | 2.1 | ns | - | - | 9 | 2 | 8 | 1.16 |
| | $t_{9\,+2+}$ | 2 | - | - | | | | - | - | | 7 | - | 9 | 2 | | |
| | $t_{6\,+2+}$ | 2 | - | - | | | | - | - | | 7 | - | 6 | 2 | | |
| | $t_{6\,+2-}$ | 2 | - | - | | | | - | - | | - | - | 6 | 2 | | |
| Rise time (20 to 80 %) | $t_{2\,+}$ | 2 | 0.5 | 1.5 | 0.5 | 1.0 | 1.5 | 0.5 | 1.6 | | 7 | - | 9 | 2 | | |
| Fall time (20 to 80 %) | $t_{2-}$ | 2 | 0.4 | 1.4 | 0.4 | | 1.4 | 0.5 | 1.5 | | - | - | 9 | 2 | | |
| Set input propagation delay | $t_{5\,+2+}$ | 2 | 0.5 | 2.0 | 0.5 | 1.0 | 2.0 | 0.6 | 2.3 | ns | - | - | 5 | 2 | 8 | 1.16 |
| | $t_{12\,+15+}$ | 15 | - | - | | | | - | - | | 6 | - | 12 | 15 | | |
| | $t_{5\,+3-}$ | 3 | - | - | | | | - | - | | - | - | 5 | 3 | | |
| | $t_{12\,+14-}$ | 14 | - | - | | | | - | - | | 9 | - | 12 | 14 | | |
| Reset input propagation delay | $t_{4\,+2-}$ | 2 | - | - | | 1.0 | | - | - | ns | - | - | 4 | 2 | 8 | 1.16 |
| | $t_{13\,+15-}$ | 15 | - | - | | | | - | - | | 6 | - | 13 | 15 | | |
| | $t_{4\,+3-}$ | 3 | - | - | | | | - | - | | - | - | 4 | 3 | | |
| | $t_{13\,+14+}$ | 14 | - | - | | | | - | - | | 9 | - | 13 | 14 | | |
| Setup time | $t_{setup}$ | 7 | 1.0 | - | 1.0 | - | | 1.0 | - | ns | - | - | 6.7 | 2 | 8 | 1.16 |
| Hold time | $t_{hold}$ | 7 | 0.2 | - | 0.2 | - | | 0.2 | - | ns | - | - | 6.7 | 2 | 8 | 1.16 |
| Toggle frequency (max.) | $f_{Tog}$ | 2 | 520 | - | 520 | 600 | - | 500 | - | MHz | - | - | 6 | 2 | 8 | 1.16 |

NOTES
1. Individually test each input, apply $V_{IL}$ min to pin under test.
2. Output level to be measured after a clock pulse has been applied to the CE input (pin 6).

$V_{IH}$ max.
$V_{IL}$ min.

## TEST CIRCUIT DETAILS

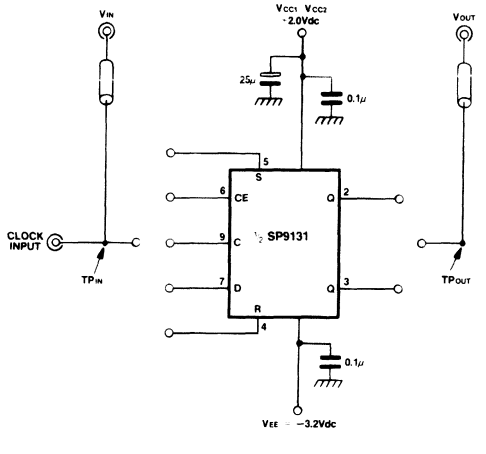


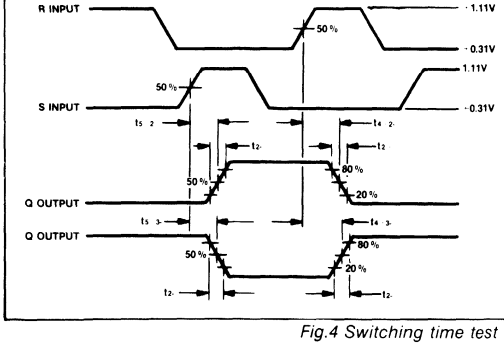

50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $< 1/4$ inch from $TP_{IN}$ to input pin and $TP_{OUT}$ to output pin.

The +2V and -3.2V supplies allow the output load to be connected to ground.

*Fig.3 Toggle frequency test circuit*

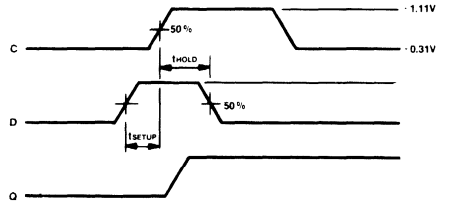



50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $< 1/4$ inch from $TP_{IN}$ to input pin and $TP_{OUT}$ to output pin.

INPUT PULSE
$t+ = t- = 1.0nsec \pm 0.2nsec$ (20 to 80%).




NOTE

$t_{setup}$ is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

$t_{hold}$ is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

*Fig.4 Switching time test circuit and waveforms at 25° C*

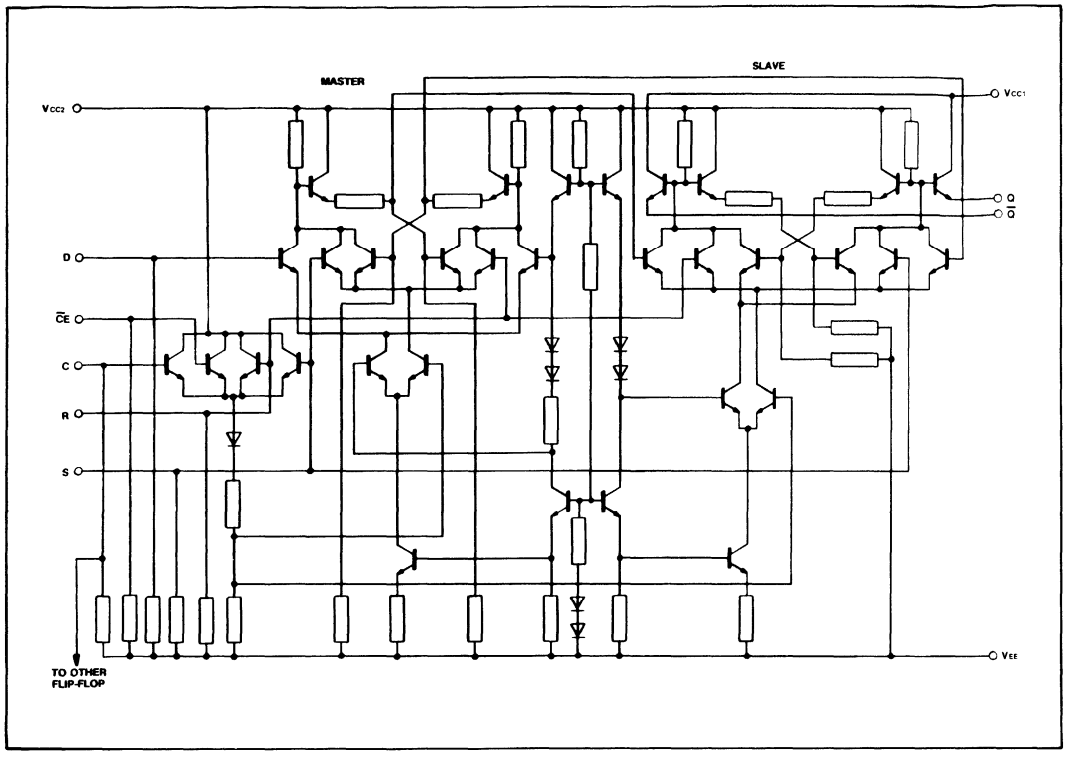



*Fig.5 Circuit schematic (½ of circuit shown)*

PLESSEY
Semiconductors

ADVANCE INFORMATION

# SP9210

## 200MHz DUAL 4-BIT LATCH

The SP9210 is a dual 4-bit master/slave D-type flip-flop with asynchronous set and reset which override the clock input.

Data is entered into the master when the clock is low and is transferred to the slave on the positive transition of the clock, the device being edge-sensitive.

On-chip pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

### FEATURES

- Dual 4-Bit Master/Slave D-Type Flip-Flop
- Clock Rate in Excess of 200MHz
- -5.2V Supply
- Current Consumption Typically 145mA
- Input Current Less Than 330μA
- Operating Temperature Range -30°C to +85°C
- Set and Reset Inputs Provided
- ECL 10K Compatible
- Dual Clock Inputs

### ORDERING INFORMATION

**SP9210DG** (Industrial - Ceramic DIL package)
**SP9210BB DG** (Plessey High Reliability Ceramic DIL package)

### PIN NAMES

| | |
|---|---|
| S1-4 | Set input for 1-4 |
| S5-8 | Set input for 5-8 |
| $V_{EE}$ | Supply voltage (-VE) |
| D1-8 | Data inputs 1-8 |
| CLK1-4 | Clock latch for 1-4 |
| CLK5-8 | Clock latch for 5-8 |
| Q1-8 | Outputs latches 1-8 |
| R1-4 | Reset input latch for 1-4 |
| R5-8 | Reset input latch for 5-8 |

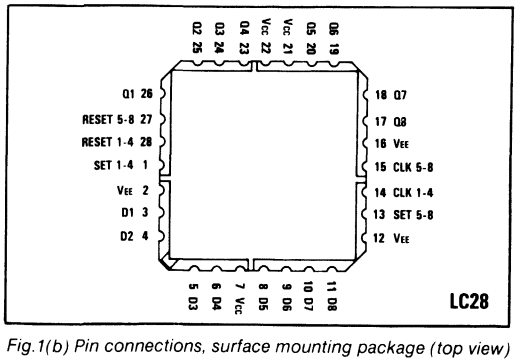



*Fig.1(b) Pin connections, surface mounting package (top view)*

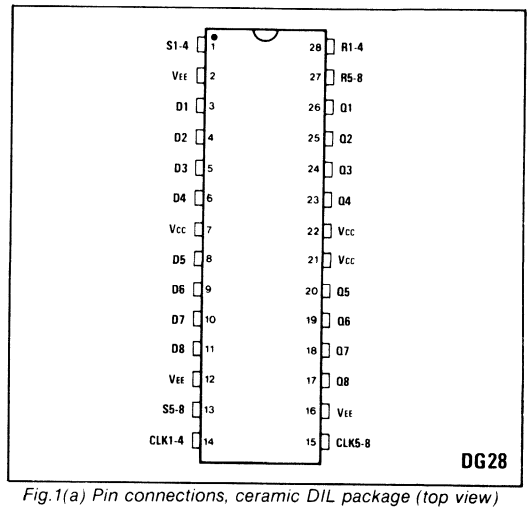



*Fig.1(a) Pin connections, ceramic DIL package (top view)*

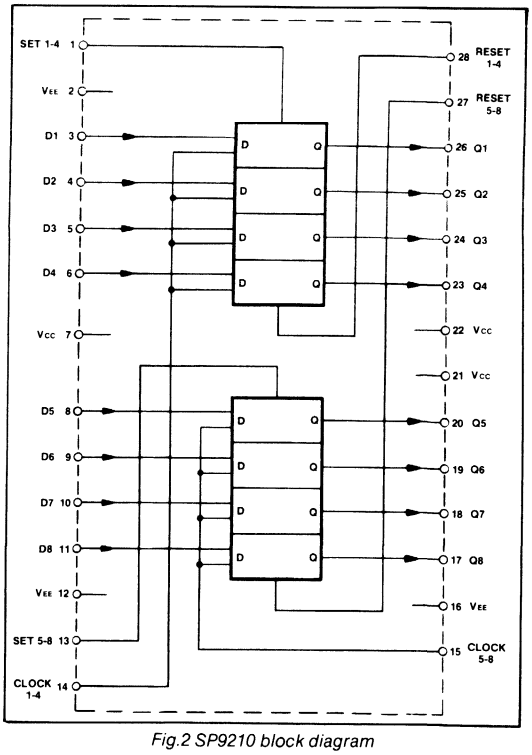



*Fig.2 SP9210 block diagram*

## ELECTRICAL CHARACTERISTICS

Each circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

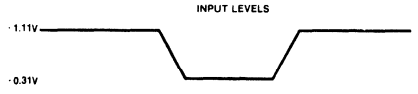
| Test temp. | TEST VOLTAGES (V) $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ |
|---|---|---|---|---|---|
| -30° C | -0.89 | -1.89 | -1.205 | -1.500 | -5.2 |
| +25° C | -0.810 | -1.850 | -1.105 | -1.475 | -5.2 |
| +85° C | -0.70 | -1.825 | -1.035 | -1.440 | -5.2 |

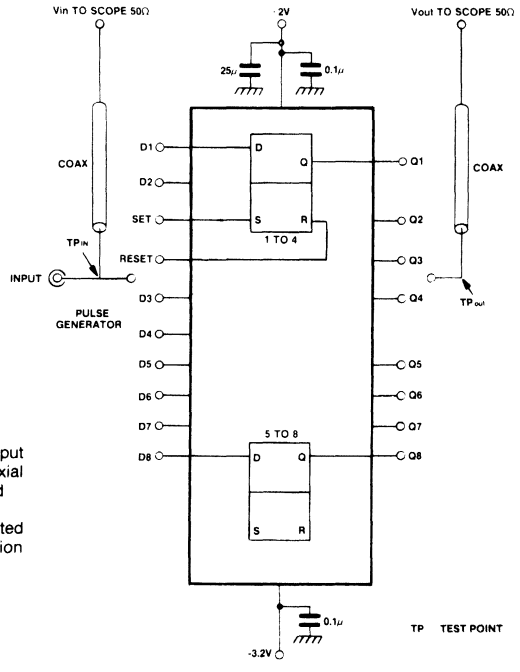
| Characteristic | Symbol | Pin under test | -30° C Min. | -30° C Max. | +25° C Min. | +25° C Typ. | +25° C Max. | +85° C Min. | +85° C Max. | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH}$ MAX. | $V_{IL}$ MIN. | $V_{IHA}$ MIN. | $V_{ILA}$ MAX. | $V_{EE}$ | $V_{CC}$ (GND) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | | | | | | | | | |
| Drain current | $I_{EE}$ | 2,12,16 | - | 200 | - | 145 | 180 | - | 200 | mA | - | - | - | - | 2,12,16 | 7,21,22 |
| Input current | $I_{INH}$ | Set/Reset | - | - | - | - | 330 | - | - | µA | Note 1 | - | - | - | 2,12,16 | 7,21,22 |
| | | Clock | - | - | - | - | 310 | - | - | µA | Note 1 | - | - | - | 2,12,16 | 7,21,22 |
| | | Data | - | - | - | - | 310 | - | - | µA | Note 1 | - | - | - | 2,12,16 | 7,21,22 |
| Input leakage current | $I_{INL}$ | All inputs | - | - | 0.5 | - | - | - | - | µA | - | Note 1 | - | - | 2,12,16 | 7,21,22 |
| Logic '1' output voltage | $V_{OH}$ | All outputs (Note 2) | -1.06 | -0.89 | -0.96 | - | -0.81 | -0.89 | -0.70 | V | Data inputs | - | - | - | 2,12,16 | 7,21,22 |
| Logic '0' output voltage | $V_{OL}$ | All outputs (Note 2) | -1.89 | -1.675 | -1.85 | - | -1.65 | -1.825 | -1.615 | V | - | Data inputs | - | - | 2,12,16 | 7,21,22 |
| Logic '1' threshold voltage | $V_{OHA}$ | All outputs (Note 2) | -1.08 | - | -0.98 | - | - | -0.91 | - | V | - | - | Data inputs | - | 2,12,16 | 7,21,22 |
| Logic '0' threshold voltage | $V_{OLA}$ | All outputs (Note 2) | - | -1.655 | - | - | -1.63 | - | -1.595 | V | - | - | - | Data inputs | | |
| **SWITCHING TIMES** | | | | | | | | | | | **+1.11V** | **+0.3V** | **Pulse in** | **Pulse out** | **-3.2V** | **+2.0V** |
| Clock input propagation delay | $t_{d+}$ | All outputs | 1.0 | 3.0 | 1.0 | 2.0 | 3.0 | 1.1 | 3.4 | ns | Data inputs | - | Clock inputs | Outputs | 2,12,16 | 7,21,22 |
| | $t_{d-}$ | All outputs | 1.0 | 3.0 | 1.0 | 2.0 | 3.0 | 1.1 | 3.4 | ns | - | Data inputs | Clock inputs | Outputs | 2,12,16 | 7,21,22 |
| Rise time (20 % - 80 %) | $t_r$ | All outputs | 1.0 | 3.0 | 1.0 | 2.0 | 3.0 | 1.1 | 3.3 | ns | Data inputs | - | Clock inputs | Outputs | 2,12,16 | 7,21,22 |
| Fall time (20 % - 80 %) | $t_f$ | All outputs | 1.0 | 3.0 | 1.0 | 2.0 | 3.0 | 1.1 | 3.3 | ns | - | Data inputs | Clock inputs | Outputs | 2,12,16 | 7,21,22 |
| Set propagation delay | $t_{set}$ | All outputs | 1.5 | 4.0 | 1.5 | 2.5 | 4.0 | 1.4 | 4.5 | ns | - | - | Set inputs | Outputs | 2,12,16 | 7,21,22 |
| Reset propagation delay | $t_{rset}$ | All outputs | 1.5 | 4.0 | 1.5 | 2.5 | 4.0 | 1.4 | 4.5 | ns | - | - | Reset inputs | Outputs | 2,12,16 | 7,21,22 |
| Set up time | $t_s$ | Data inputs | 1.5 | - | 1.5 | - | - | 1.5 | - | ns | - | - | Data,Clock | Outputs | 2,12,16 | 7,21,22 |
| Hold time | $t_h$ | Data inputs | 1.0 | - | 1.0 | - | - | 1.0 | - | ns | - | - | Data,Clock | Outputs | 2,12,16 | 7,21,22 |
| Max.clock frequency | $f_{CLK}$ | All outputs | - | - | 200 | - | - | - | - | MHz | Data inputs | - | Clock inputs | Outputs | 2,12,16 | 7,21,22 |

NOTES
1. Each input pin tested individually.
2. Output level to be measured after a clock pulse has been applied.


Thermal characteristics

| | |
|---|---|
| DG28 | $\theta_{JA}$ = 40°C/W |
| | $\theta_{JC}$ = 15°C/W |
| LC28 | $\theta_{JA}$ = 70°C/W |
| | $\theta_{JC}$ = 16°C/W |

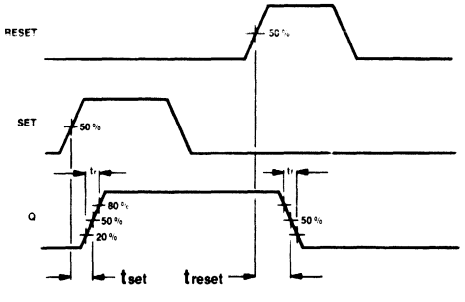


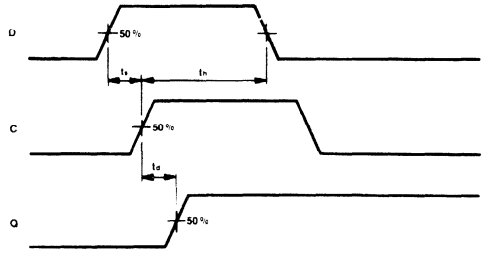

50 ohm to ground located in each scope channel input. All input and output cables to the scope are equal length of 50 ohm coaxial cable. Wire length should be ¼ inch from $TP_{IN}$ to input pin and $TP_{OUT}$ to output pin.

With supply voltages at 2V and -3.2V outputs should be terminated with 50 ohms to ground; this results in an output level translation giving $V_{OH}$ = 1.11V and $V_{OL}$ = +0.31V.

**SET AND RESET TIMING DIAGRAM**




**CLOCK AND DATA TIMING DIAGRAM**




NOTE

$t_{setup}$ is the minimum time before the positive transition of the clock pulse (C) that information must be present at data input (D).

$t_{hold}$ is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at data input (D).

*Fig.3 Test circuit details for dynamic test*

## R - S TRUTH TABLE

| R | S | Qn + 1 |
|---|---|---|
| L | L | Qn |
| L | H | H |
| H | L | L |
| H | H | ND |

R = Reset, S = Set,
ND = Not defined

## CLOCKED TRUTH TABLE

| C | D | Qn + 1 |
|---|---|---|
| L | X | Qn |
| ↓ | L | L |
| ↑ | H | H |

C = Clock, D = Data,
↑ = Rising edge,
X = Don't care

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\|V_{CC} - V_{EE}\|$ 7V |
| Input voltages | $V_{CC}$ to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

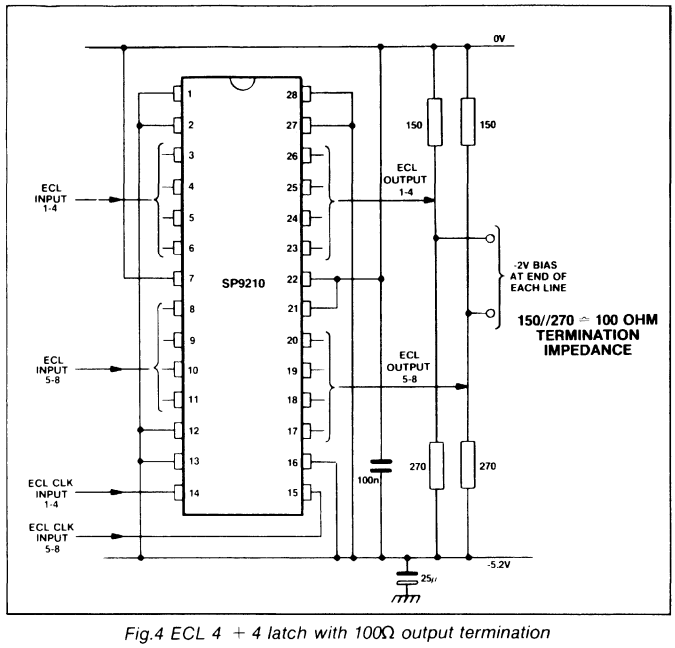



*Fig.4 ECL 4 + 4 latch with 100Ω output termination*

PLESSEY
Semiconductors

# SP16F60

## DUAL 4-INPUT OR/NOR GATE

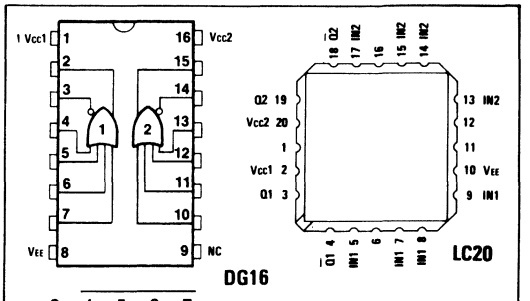
SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (—30° C to +85° C). Input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

### FEATURES

- Operating Temperature Range -30°C to +85°C
- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible With SP1660

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics




DC Input Loading Factor = 1
DC Output Loading Factor = 70
$t_{pd}$ = 0.9ns typ (510-ohm load)
= 1.1ns typ (50-ohm load)
$P_D$ = 120mW typ/pkg (No load)
Full Load Current, $I_L$ = -25mA dc max.

*Fig.1(a) Logic and pin connections (top view) DG package*
*Fig.1(b) Pin connections LC package*

### ORDERING INFORMATION

**SP16F60DG** (Industrial - Ceramic DIL package)
**SP16F60BB DG** (Plessey High Reliability Ceramic DIL package)
**SP16F60LC** (Industrial - LCC package)
**SP16F60BC DG** (Military - Ceramic DIL package)

NOTE:
The BC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510. Please consult your nearest Plessey sales office for availability of separately published data.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\lvert V_{CC} - V_{EE} \rvert$ 8V |
| Input voltages | 0V to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

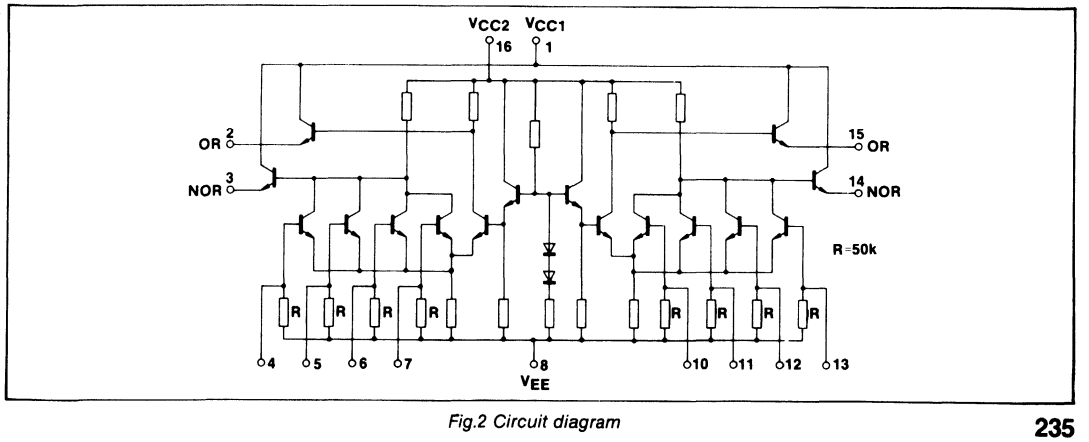



*Fig.2 Circuit diagram*

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

Thermal characterstics

| | |
|---|---|
| DG16 | $\theta_{JA}$ = 120°C/W |
| | $\theta_{JC}$ = 40°C/W |
| LC20 | $\theta_{JA}$ = 73°C/W |
| | $\theta_{JC}$ = 22°C/W |

| @ Test Temperature | TEST VOLTAGE VALUES (V) $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ |
|---|---|---|---|---|---|
| -30°C | -0.875 | -1.890 | -1.180 | -1.515 | -5.2 |
| +25°C | -0.810 | -1.850 | -1.095 | -1.485 | -5.2 |
| +85°C | -0.700 | -1.830 | -1.025 | -1.440 | -5.2 |

| Characteristic | Symbol | Pin Under Test | SP16F60 Test Limits -30°C Min | -30°C Max | +25°C Min | +25°C Max | +85°C Min | +85°C Max | Units | TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ | $V_{CC}$ (Gnd) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Drain Current | $I_E$ | 8 | – | – | – | 28 | – | – | mA | – | – | – | – | 8 | 1,16 |
| Input Current | $I_{in\ H}$ | * | – | – | – | 350 | – | – | μA | * | – | – | – | 8 | 1,16 |
| | $I_{in\ L}$ | * | – | – | 0.5 | – | – | – | μA | – | * | – | – | 8 | 1,16 |
| NOR Logic 1 Output Voltage | $V_{OH}$ | 3 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | – | 4 | – | – | 8 | 1,16 |
| | | | | | | | | | | – | 5 | – | – | | |
| | | | | | | | | | | – | 6 | – | – | | |
| | | | | | | | | | | – | 7 | – | – | | |
| NOR Logic 0 Output Voltage | $V_{OL}$ | 3 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | 4 | – | – | – | 8 | 1,16 |
| | | | | | | | | | | 5 | – | – | – | | |
| | | | | | | | | | | 6 | – | – | – | | |
| | | | | | | | | | | 7 | – | – | – | | |
| OR Logic 1 Output Voltage | $V_{OH}$ | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | 4 | – | – | – | 8 | 1,16 |
| | | | | | | | | | | 5 | – | – | – | | |
| | | | | | | | | | | 6 | – | – | – | | |
| | | | | | | | | | | 7 | – | – | – | | |
| OR Logic 0 Output Voltage | $V_{OL}$ | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | – | 4 | – | – | 8 | 1,16 |
| | | | | | | | | | | – | 5 | – | – | | |
| | | | | | | | | | | – | 6 | – | – | | |
| | | | | | | | | | | – | 7 | – | – | | |
| NOR Logic 1 Threshold Voltage | $V_{OHA}$ | 3 | -1.065 | – | -0.980 | – | -0.910 | – | V | – | – | – | 4 | 8 | 1,16 |
| | | | | – | | – | | – | | – | – | – | 5 | | |
| | | | | – | | – | | – | | – | – | – | 6 | | |
| | | | | – | | – | | – | | – | – | – | 7 | | |
| NOR Logic 0 Threshold Voltage | $V_{OLA}$ | 3 | – | -1.630 | – | -1.600 | – | -1.555 | V | – | – | 4 | – | 8 | 1,16 |
| | | | – | | – | | – | | | – | – | 5 | – | | |
| | | | – | | – | | – | | | – | – | 6 | – | | |
| | | | – | | – | | – | | | – | – | 7 | – | | |
| OR Logic 1 Threshold Voltage | $V_{OHA}$ | 2 | -1.065 | – | -0.980 | – | -0.910 | – | V | – | – | 4 | – | 8 | 1,16 |
| | | | | – | | – | | – | | – | – | 5 | – | | |
| | | | | – | | – | | – | | – | – | 6 | – | | |
| | | | | – | | – | | – | | – | – | 7 | – | | |
| OR Logic 0 Threshold Voltage | $V_{OLA}$ | 2 | – | -1.630 | – | -1.600 | – | -1.555 | V | – | – | – | 4 | 8 | 1,16 |
| | | | – | | – | | – | | | – | – | – | 5 | | |
| | | | – | | – | | – | | | – | – | – | 6 | | |
| | | | – | | – | | – | | | – | – | – | 7 | | |
| Switching Times (50Ω Load) | | | Typ | Max | Typ | Max | Typ | Max | | Pulse In | Pulse Out | | | -3.2V | +2.0V |
| Propagation Delay | $t_{4+3-}$ | 3 | – | – | 0.55 | 0.8 | – | – | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{4-2-}$ | 2 | – | – | | | – | – | | | 2 | – | – | | |
| | $t_{4+2+}$ | 2 | – | – | | | – | – | | | 2 | – | – | | |
| | $t_{4-3+}$ | 3 | – | – | | | – | – | | | 3 | – | – | | |
| Rise Time 20% to 80% | $t_{3+}$ | 3 | | | 0.4 | 0.6 | – | – | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{2+}$ | 2 | | | 0.35 | 0.6 | – | – | ns | 4 | 2 | – | – | 8 | 1,16 |
| Fall Time 20% to 80% | $t_{3-}$ | 3 | | | 0.4 | 0.6 | – | – | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{2-}$ | 2 | | | 0.35 | 0.6 | – | – | ns | 4 | 2 | – | – | 8 | 1,16 |

* Individually test each input applying $V_{IH}$ or $V_{IL}$ to the input under test.

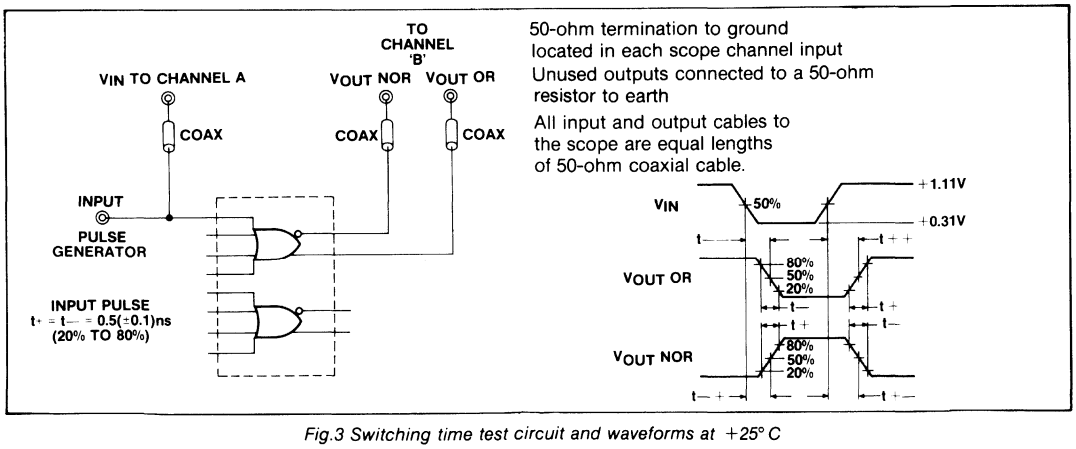



*Fig.3 Switching time test circuit and waveforms at +25° C*

PLESSEY
Semiconductors

# SP1648

## ECL OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of an inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0V dc supply or a -5.2V dc supply, depending upon system requirements.

**Operating temperature range:**
-30° C to +85° C (Ceramic)
0° C to +75° C (Plastic)

| SUPPLY VOLTAGE | GND PINS | SUPPLY PINS |
|---|---|---|
| +5.0V dc | 7,8 | 1,14 |
| -5.2V dc | 1,14 | 7,8 |

### ORDERING INFORMATION

**SP1648DP** (Industrial - Plastic DIL package)
**SP1648DG** (Industrial - Ceramic DIL package)
**SP1648BB DG** (Plessey High Reliability Ceramic DIL package)
**SP1648 LC** (Industrial - LCC package)
**SP1648 MP** (Industrial - Miniature Plastic package)

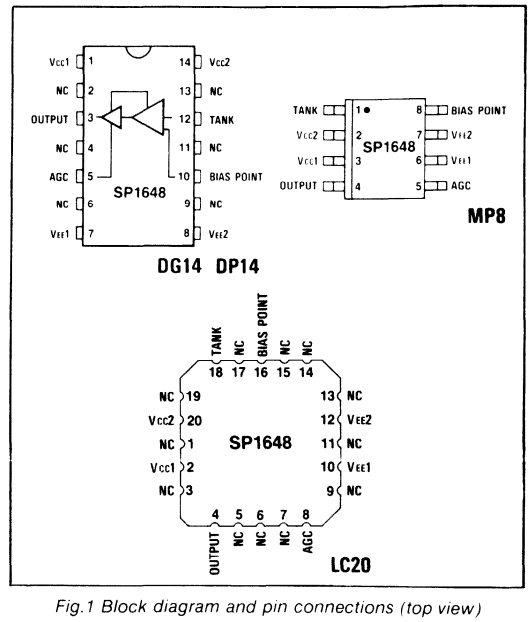



*Fig.1 Block diagram and pin connections (top view)*

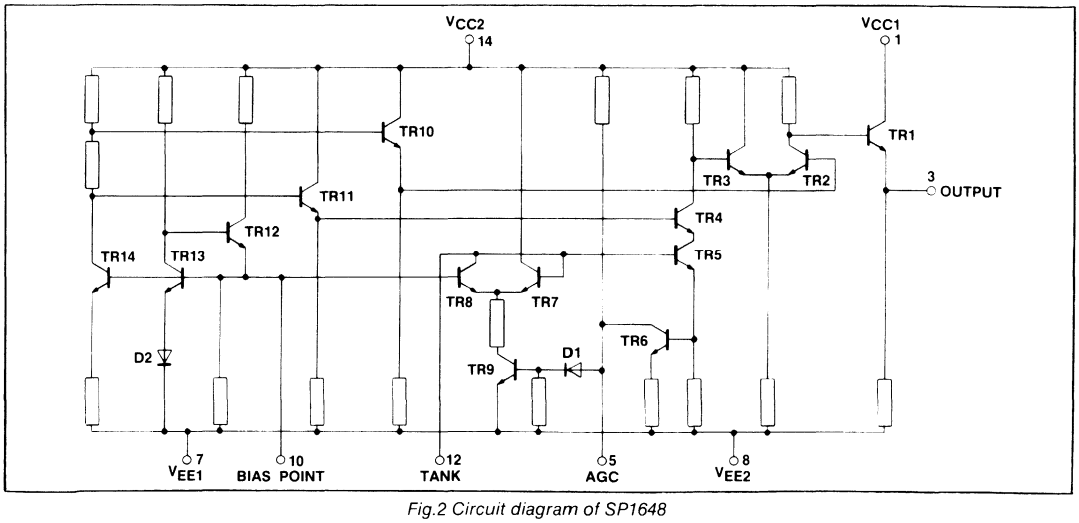



*Fig.2 Circuit diagram of SP1648*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | \| $V_{CC}$ - $V_{EE}$ \| 8V |
| Output source current | <40mA |
| AGC input | $V_{CC}$ to $V_{EE}$ |
| Storage temperature range | -65°C to +150°C (Ceramic) |
| | -55°C to +150°C (Plastic) |
| Operating junction temperature DG | <175°C |
| Operating junction temperature DP | <150°C |

## ELECTRICAL CHARACTERISTICS

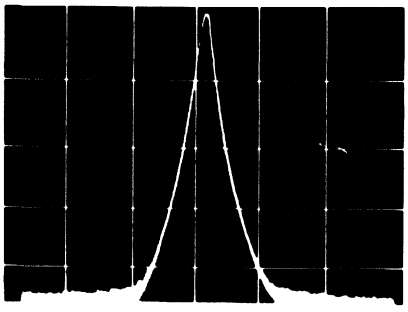
**Supply Voltage = +5.0V**

| Characteristic | Symbol | Pin under test | SP1648 Test Limits | | | | | | | | | | TEST VOLTAGE/CURRENT | | | | | | $V_{EE}$ (Gnd) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -30° C | | | +25° C | | | +85° C | | | Unit | Volts | | | mAdc | | | |
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | Test temp. | $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{CC}$ | $I_L$ | | |
| Power supply drain current | $I_E$ | 8 | - | | - | - | | 40 | - | | - | mAdc | -30° C | - | - | 5.0 | 5.0 | | 7,8 |
| Logic '1' output voltage | $V_{OH}$ | 3 | 3.94 | | 4.18 | 4.04 | | 4.25 | 4.11 | | 4.36 | Vdc | +25° C | - | 12 | 5.0 | 5.0 | | 7,8 |
| Logic '0' output voltage | $V_{OL}$ | 3 | 3.16 | | 3.40 | 3.20 | | 3.43 | 3.23 | | 3.46 | Vdc | +85° C | 12 | - | 5.0 | 5.0 | | 7,8 |
| Bias voltage | $V_{bias}$* | 10 | 1.51 | | 1.86 | 1.40 | | 1.70 | 1.28 | | 1.58 | Vdc | TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW | | | | | | |
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | $V_{IH}$ Max. | $V_{IL}$ Max. | $V_{CC}$ | $I_L$ | | | |
| Peak-to-peak tank voltage | $V_{P-P}$ | 12 | - | - | - | - | 500 | - | - | - | - | mV | See Fig.4 | - | 1.14 | 3 | | | 7,8 |
| Output duty cycle | $V_{DC}$ | 3 | - | - | - | - | 50 | - | - | - | - | % | See Fig.4 | - | 1.14 | 3 | | | 7,8 |
| Oscillation frequency | $f_{max}$ | - | - | - | - | 200 | 225 | - | - | - | - | MHz | See Fig.4 | - | 1.14 | 3 | | | 7,8 |

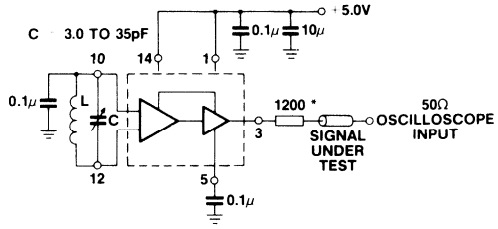
Thermal characteristics
DG14 $\theta_{JA} = 125°C/W$
$\theta_{JC} = 40°C/W$
DP14 $\theta_{JA} = 107°C/W$
$\theta_{JC} = 52°C/W$

**Supply Voltage = -5.2V**

| Characteristic | Symbol | Pin under test | SP1648 Test Limits | | | | | | | | | | TEST VOLTAGE/CURRENT | | | | | | $V_{EE}$ (Gnd) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -30° C | | | +25° C | | | +85° C | | | Unit | Volts | | | mAdc | | | |
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | Test temp. | $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{CC}$ | $I_L$ | | |
| Power supply drain current | $I_E$ | 8 | - | | - | - | | 41 | - | | - | mAdc | -30° C | - | - | 7.8 | - | | 1,14 |
| Logic '1' output voltage | $V_{OH}$ | 3 | 1.045 | | -0.815 | -0.960 | | -0.750 | -0.890 | | -0.650 | Vdc | +25° C | - | 12 | 7.8 | 3 | | 1,14 |
| Logic '0' output voltage | $V_{OL}$ | 3 | -1.890 | | -1.650 | -1.850 | | -1.620 | -1.830 | | -1.575 | Vdc | +85° C | 12 | - | 7.8 | 3 | | 1,14 |
| Bias voltage | $V_{bias}$* | 10 | -3.690 | | -3.340 | -3.800 | | -3.500 | -3.920 | | -3.620 | Vdc | TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW | | | | | | |
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | $V_{IH}$ Max. | $V_{IL}$ Max. | $V_{CC}$ | $I_L$ | | | |
| Peak-to-peak tank voltage | $V_{P-P}$ | 12 | - | - | - | - | 500 | - | - | - | - | mV | See Fig.4 | - | 7.8 | 3 | | | 1,14 |
| Output duty cycle | $V_{DC}$ | 3 | - | - | - | - | 50 | - | - | - | - | % | See Fig.4 | - | 7.8 | 3 | | | 1,14 |
| Oscillation frequency | $f_{max}$ | - | - | - | - | 200 | 225 | - | - | - | - | MHz | See Fig.4 | - | 7.8 | 3 | | | 1,14 |

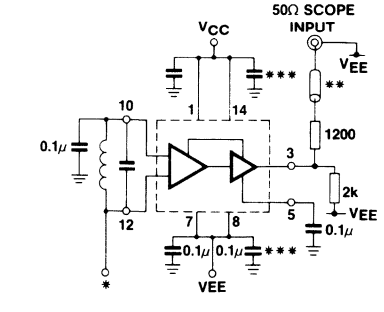


B.W. = 10kHz
Center Frequency = 100MHz
Scan Width = 50kHz/div
Vertical Scale = 10dB/div




*The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

*Fig.3 Spectral purity of signal at output (DIL pin numbers)*




*Use high impedance probe (>1.0MΩ must be used).

**The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

***Bypass only that supply opposite ground.

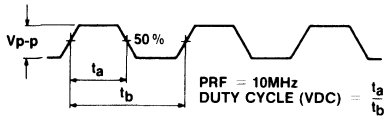



*Fig.4 Test circuit and waveforms (DIL pin numbers)*

## OPERATING CHARACTERISTICS

Fig.1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 through TR14 provide this bias drive for the oscillator and output buffer. Fig.3 indicates the high spectral purity of the oscillator output.

When operating the oscillator in the voltage controlled mode (Fig.5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 $V_{BE}$ above $V_{EE}$ (≈1.4V for positive supply operation).

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Fig.6.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figs.7,8 and 9. Figs.7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6pF typical). Fig.8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1kΩ resistor in Figs.7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51kΩ) in Fig.9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

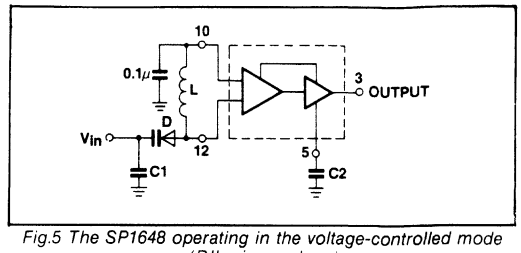



*Fig.5 The SP1648 operating in the voltage-controlled mode (DIL pin numbers)*

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\,(max) + C_S}}{\sqrt{C_D\,(min) + C_S}}$$

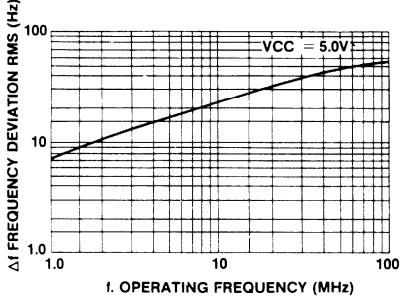
where $f_{min} = \dfrac{1}{2\pi\sqrt{L\,(C_D\,(max) + C_S)}}$

$C_S$ = shunt capacitance (input plus external capacitance).
$C_D$ = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Fig.3).

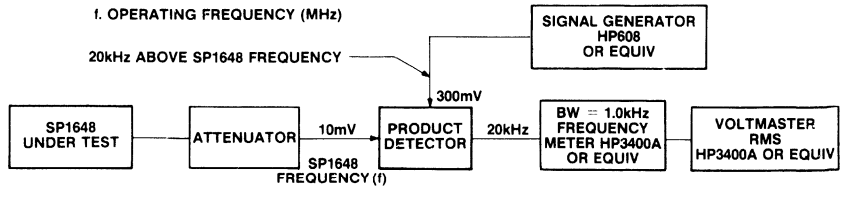
Capacitors (C1 and C2 of Fig.5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1MHz and 50MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly




**OSCILLATOR TANK COMPONENTS (CIRCUIT OF FIGURE 5)**

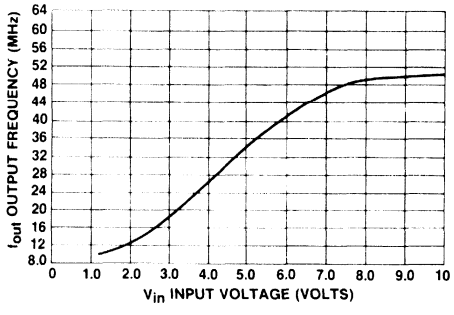
| f MHz | D | L μH |
|---|---|---|
| 1.0-10 | MV2115 | 100 |
| 10-60 | MV2115 | 2.3 |
| 60-100 | MV2106 | 0.15 |




$$\text{FREQUENCY DEVIATION} = \frac{\text{(HP5210A OUTPUT VOLTAGE) (FULL SCALE FREQUENCY)}}{\text{1.0VOLT}}$$

Note: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimised prior to testing.

*Fig.6 Frequency deviation test circuit*



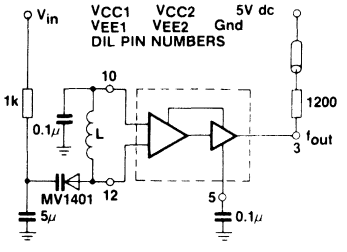
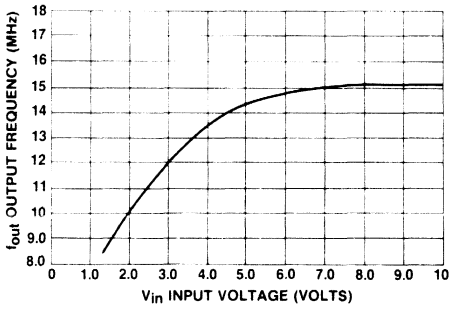




*Fig.7*



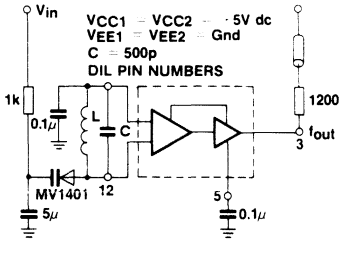
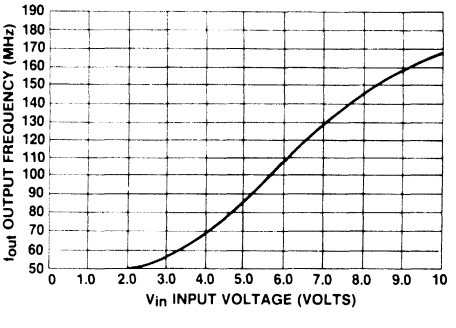




*Fig.8*



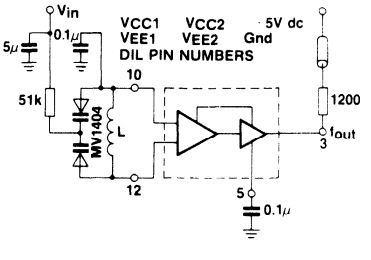




*Fig.9*

upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimise unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0V supply is used, -5.2V if a negative supply is used).

At frequencies above 100MHz typ. it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by attaching a series resistor (1kΩ minimum) from the AGC to the most positive power potential (+5.0V if a +5.0V supply is used, ground if a -5.2V supply is used).

PLESSEY
Semiconductors

# SP1650

## DUAL A/D COMPARATOR

The SP1650 is a very high speed comparator utilising differential amplifier inputs to sense analogue signals above or below a reference level. An output latch provides a unique sample-hold feature.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock iinputs ($\overline{C}_a$ and $\overline{C}_b$) operate from ECL III or ECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, $Q_a$ will be at a logic high level provided that $V_1 > V_2$ ($V_1$ is more positive than $V_2$). $\overline{Q}_a$ is the logic complement of $Q_a$. When the clock in to a low logic level, the outputs are latched in their present state.

### FEATURES

- $P_D$ = 330mW typ/pkg (No Load)
- $t_{pd}$ = 3.5ns typ.
- Input Slew Rate = 350V/us
- Differential Input Voltage: -5.0V to +5.0V (-30°C to +85°C)
- Common Mode Range: -2.5V to +3.0V (-30°C to +85°C)
- Resolution: ≤20mV (-30°C to +85°C)
- Drives 50 ohm lines

### TRUTH TABLE

| $\overline{C}$ | $V_1$ $V_2$ | Qn + 1 | $\overline{Qn}$ + 1 |
|---|---|---|---|
| H | $V_1 > V_2$ | H | L |
| H | $V_1 < V_2$ | L | H |
| L | $\phi$ $\phi$ | $Q_n$ | $\overline{Q_n}$ |

$\phi$ = Don't Care

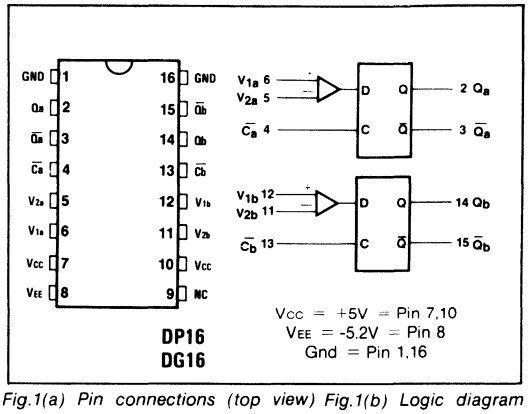



*Fig.1(a) Pin connections (top view) Fig.1(b) Logic diagram*

**Operating temperature range:**
-30°C to +85°C (Ceramic)
0°C to +75°C (Plastic)

### ORDERING INFORMATION

**SP1650DG** (Industrial - Ceramic DIL package)
**SP1650BB DG** (Plessey High Reliability Ceramic DIL package)
**SP1650 DP** (Industrial - Plastic DIL package)
**SP1650 BC DG** (Military - Ceramic DIL package)

NOTE:
The BC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

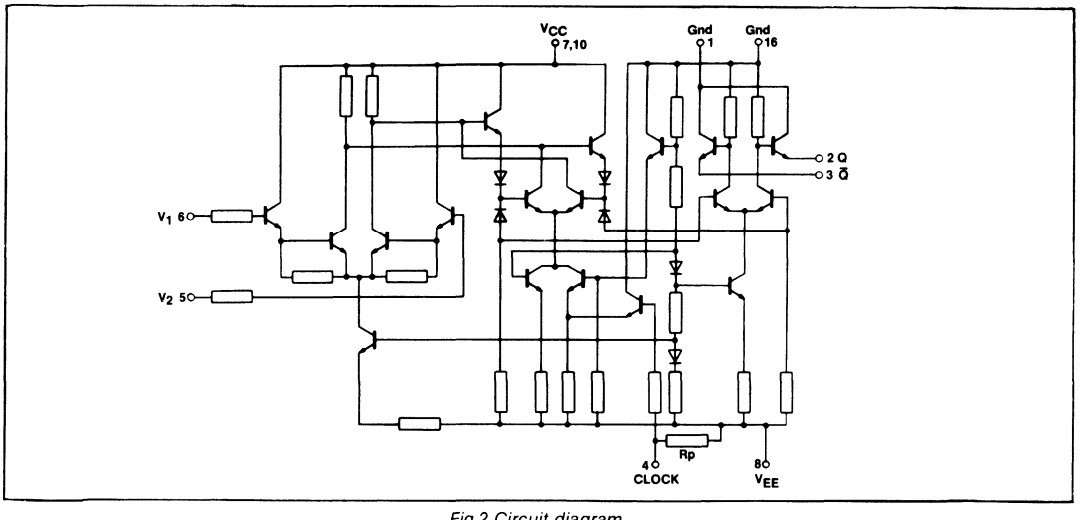



*Fig.2 Circuit diagram*

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

| Test temp. | TEST VOLTAGE (V) $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{A1}$ | $V_{A2}$ | $V_{A3}$ | $V_{A4}$ | $V_{A5}$ | $V_{A6}$ | $V_{CC}$ (3) | $V_{EE}$ (3) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| -30°C | -0.875 | -1.890 | -1.180 | -1.515 | +0.020 | -0.020 | See Note (4) | | | | +5.0 | -5.2 |
| +25°C | -0.810 | -1.850 | -1.095 | -1.485 | +0.020 | -0.020 | | | | | +5.0 | -5.2 |
| +85°C | -0.700 | -1.830 | -1.025 | -1.440 | +0.020 | -0.020 | | | | | +5.0 | -5.2 |

| Characteristic | Symbol | Pin under test | SP1650 Test Limits (1) -30°C Min. | -30°C Max. | +25°C Min. | +25°C Max. | +85°C Min. | +85°C Max. | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{A1}$ | $V_{A2}$ | $V_{A3}$ | $V_{A4}$ | $V_{A5}$ | $V_{A6}$ | $V_{CC}$ (3) | $V_{EE}$ (3) | Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | | | | | | | | | | | | | | | |
| Drain current | | | | | | | | | | | | | | | | | | | | | | |
| Positive | $I_{CC}$ | 7,10 | - | - | - | 25* | - | - | mAdc | - | 4,13 | - | - | 6,12 | - | - | - | - | - | 7,10 | 8 | 1,5,11,16 |
| Negative | $I_E$ | 8 | - | - | - | 55* | - | - | mAdc | 4,13 | - | - | - | 6,12 | - | - | - | - | - | 7,10 | 8 | 1,5,11,16 |
| Input current | $I_{IN}$ | 6 | - | - | - | 10 | - | - | μAdc | 4 | 13 | - | - | 12 | - | 6 | - | - | - | 7,10 | 8 | 1,5,11,16 |
| Input leakage current | $I_R$ | 6 | - | - | - | 7 | - | - | μAdc | 4 | 13 | - | - | 12 | - | - | - | 5 | - | 7,10 | 8 | 1,5,11,16 |
| Input clock current | $I_{INH}$ | 4 | - | - | - | 350 | - | - | μAdc | 4 | 13 | - | - | 6,12 | - | - | - | - | - | 7,10 | 8 | 1,5,11,16 |
| | $I_{INL}$ | 4 | - | - | 0.5 | - | - | - | μAdc | - | 13 | - | - | 6,12 | - | - | - | - | - | 7,10 | 4,8 | 1,5,11,16 |
| Logic '1' output voltage | $V_{OH}$ | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | Vdc | 4,13 | - | - | - | 6,12 | - | - | - | - | - | 7,10 | 8 | 1,5,11,16 |
| | 2 | | | | | | | | | | - | - | - | - | 5,11 | - | - | - | - | | | 1,6,12,16 |
| | 2 | | | | | | | | | | - | - | - | - | - | 6,12 | 5,11 | - | - | | | 1,16 |
| | 2 | | | | | | | | | | - | - | - | - | - | - | - | 5,11 | 6,12 | | | 1,16 |
| | 3 | | | | | | | | | | - | - | - | - | 6,12 | - | - | - | - | | | 1,5,11,16 |
| | 3 | | | | | | | | | | - | - | - | 5,11 | - | - | - | - | - | | | 1,6,12,16 |
| | 3 | | | | | | | | | | - | - | - | - | - | 5,11 | 6,12 | - | - | | | 1,16 |
| | 3 | | | | | | | | | | - | - | - | - | - | - | - | 6,12 | 5,11 | | | 1,16 |
| Logic '0' output voltage | $V_{OL}$ | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | Vdc | 4,13 | - | - | - | - | 6,12 | - | - | - | - | 7,10 | 8 | 1,5,11,16 |
| | 2 | | | | | | | | | | - | - | - | 5,11 | - | - | - | - | - | | | 1,6,12,16 |
| | 2 | | | | | | | | | | - | - | - | - | - | 5,11 | 6,12 | - | - | | | 1,16 |
| | 2 | | | | | | | | | | - | - | - | - | - | - | - | 6,12 | 5,11 | | | 1,16 |
| | 3 | | | | | | | | | | - | - | - | 6,12 | - | - | - | - | - | | | 1,5,11,16 |
| | 3 | | | | | | | | | | - | - | - | - | 5,11 | - | - | - | - | | | 1,16,12,16 |
| | 3 | | | | | | | | | | - | - | - | - | - | 6,12 | 5,11 | - | - | | | 1,16 |
| | 3 | | | | | | | | | | - | - | - | - | - | - | - | 5,11 | 6,12 | | | 1,16 |
| Logic '0' threshold voltage (2) | 1 | $V_{OHA}$ | 2 | -1.065 | - | -0.980 | - | -0.910 | - | Vdc | - | 13 | 4 | - | 6 | - | - | - | - | 7,10 | 8 | 1,5,16 |
| | 2 | | 2 | - | - | - | - | - | - | | - | | - | 4 | - | 6 | - | - | - | | | |
| | 3 | | 3 | - | - | - | - | - | - | | - | | 4 | - | - | 6 | - | - | - | | | |
| | 4 | | 3 | - | - | - | - | - | - | | - | | - | 4 | 6 | - | - | - | - | | | |
| Logic '0' threshold voltage (2) | 1 | $V_{OLA}$ | 3 | - | -1.630 | - | -1.600 | - | -1.555 | Vdc | - | 13 | 4 | - | 6 | - | - | - | - | 7,10 | 8 | 1,5,16 |
| | 2 | | 3 | - | - | - | - | - | - | | - | | - | 4 | - | 6 | - | - | - | | | |
| | 3 | | 2 | - | - | - | - | - | - | | - | | 4 | - | - | 6 | - | - | - | | | |
| | 4 | | 2 | - | - | - | - | - | - | | - | | - | 4 | 6 | - | - | - | - | | | |

NOTES
1. All data is for ½ SP1650 except data marked ( *) which refers to the entire package.
2. These tests done in order indicated. See Figure 6.
3. Maximum Power Supply Voltages (beyond which device life may be impaired):
   $|V_{EE}| + |V_{CC}| < 12V$ dc.
4. At all temperatures, $V_{A3} = +3.000V$, $V_{A4} = +2.980V$, $V_{A5} = -2.500V$ and $V_{A6} = -2.480V$.

| Test temp. | TEST VOLTAGE (V) $V_{R1}$ | $V_{R2}$ | $V_{R3}$ | $V_X$ | $V_{XX}$ | $V_{CC}$ (1) | $V_{EE}$ (1) |
|---|---|---|---|---|---|---|---|
| -30°C | +2.000 | See Note (4) | | +1.040 | +2.00 | +7.00 | -3.20 |
| +25°C | +2.000 | | | +1.110 | +2.00 | +7.00 | -3.20 |
| +85°C | +2.000 | | | +1.190 | +2.00 | +7.00 | -3.20 |

See Figure 4

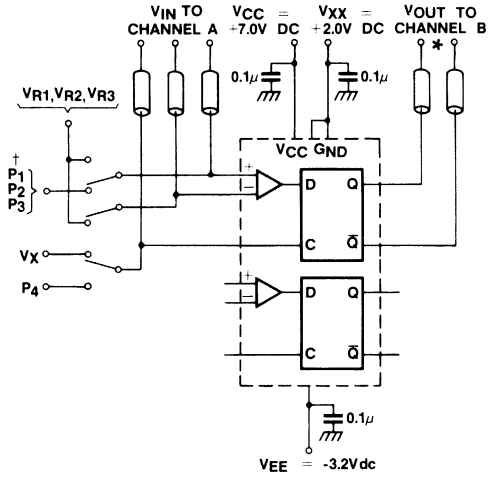
| Characteristic | Symbol | Pin under test | SP1650 Test Limits -30°C Min. | -30°C Max. | +25°C Min. | +25°C Max. | +85°C Min. | +85°C Max. | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{R1}$ | $V_{R2}$ | $V_{R3}$ | $V_X$ | $V_{XX}$ | $V_{CC}$ (1) | $V_{EE}$ (1) | P1 | P2 | P3 | P4 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **SWITCHING TIMES** | $t_{6\text{-}2\downarrow}$ | 2 | 2.0 | 5.0 | 2.0 | 5.0 | 2.0 | 5.7 | ns | 5 | - | - | 4 | 1,11,16 | 7,10 | 8 | 6 | - | - | - |
| Propagation delay | $t_{6\text{-}2\uparrow}$ | 2 | | | | | | | | - | 5 | - | | | | | - | 6 | - | - |
| (50% to 50%) | $t_{6\text{-}2\downarrow}$ | 2 | | | | | | | | - | - | 5 | | | | | - | - | 6 | - |
| V-input to output | $t_{6\text{-}3\uparrow}$ | 3 | | | | | | | | 5 | - | - | | | | | 6 | - | - | - |
| | $t_{6\text{-}3\downarrow}$ | 3 | | | | | | | | - | 5 | - | | | | | - | 6 | - | - |
| | $t_{6\text{-}3\uparrow}$ | 3 | | | | | | | | - | - | 5 | | | | | - | - | 6 | - |
| | $t_{6\text{-}2\uparrow}$ | 2 | | | | | | | | 5 | - | - | | | | | 6 | - | - | - |
| | $t_{6\text{-}2\downarrow}$ | 2 | | | | | | | | - | 5 | - | | | | | - | 6 | - | - |
| | $t_{6\text{-}2\uparrow}$ | 2 | | | | | | | | - | - | 5 | | | | | - | - | 6 | - |
| | $t_{6\text{-}3\downarrow}$ | 3 | | | | | | | | 5 | - | - | | | | | 6 | - | - | - |
| | $t_{6\text{-}3\uparrow}$ | 3 | | | | | | | | - | 5 | - | | | | | - | 6 | - | - |
| | $t_{6\text{-}3\downarrow}$ | 3 | | | | | | | | - | - | 5 | | | | | - | - | 6 | - |
| Clock to output (2) | $t_{4\text{-}2\downarrow}$ | 2 | 2.0 | 4.7 | 2.0 | 4.7 | 2.0 | 5.2 | ns | 5 | - | - | - | 1,11,16 | 7,10 | 8 | 6 | - | - | 4 |
| | $t_{4\text{-}2\uparrow}$ | 2 | | | | | | | | 6 | - | - | - | | | | 5 | - | - | |
| | $t_{4\text{-}3\downarrow}$ | 3 | | | | | | | | 6 | - | - | - | | | | 5 | - | - | |
| | $t_{4\text{-}3\uparrow}$ | 3 | | | | | | | | 5 | - | - | - | | | | 6 | - | - | |
| Clock enable time (3) | $t_{setup}$ | 6 | - | - | 2.5 | - | - | - | ns | 5 | - | - | - | 1,11,16 | 7,10 | 8 | 6 | - | - | 4 |
| Clock aperture time (3) | $t_{ap}$ | 6 | - | - | 1.5 | - | - | - | ns | 5 | - | - | - | 1,11,16 | 7,10 | 8 | 6 | - | - | 4 |
| Rise time | $t_{2\uparrow}$ | 2 | 1.0 | 3.5 | 1.0 | 3.5 | 1.0 | 3.8 | ns | 5 | - | - | 4 | 1,11,16 | 7,10 | 8 | 6 | - | - | - |
| (10% to 90%) | $t_{3\uparrow}$ | 3 | 1.0 | 3.5 | 1.0 | 3.5 | 1.0 | 3.8 | ns | 5 | - | - | 4 | 1,11,16 | 7,10 | 8 | 6 | - | - | - |
| Fall time | $t_{2\downarrow}$ | 2 | 1.0 | 3.0 | 1.0 | 3.0 | 1.0 | 3.3 | ns | 5 | - | - | 4 | 1,11,16 | 7,10 | 8 | 6 | - | - | - |
| (10% to 90%) | $t_{3\downarrow}$ | 3 | 1.0 | 3.0 | 1.0 | 3.0 | 1.0 | 3.3 | ns | 5 | - | - | 4 | 1,11,16 | 7,10 | 8 | 6 | - | - | - |

## NOTES AND MAXIMUM RATINGS

1. Maximum power supply voltages (beyond which device life may be impaired): $|V_{CC}| + |V_{EE}| = 12VDC$
2. Unused clock inputs may be tied to ground.
3. See Fig. 10.
4. At all temperatures, $V_{R2} = +4.9000V$ and $V_{R3} = -0.400V$.
5. Storage temperature: -65°C to +150°C
6. Operating junction temperature <175°C

Thermal characteristics

$\theta_{JA} = 110°$ C/W
$\theta_{JC} = 33°$ C/W




50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

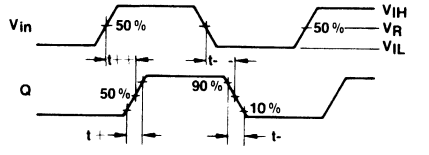
†Refer to Fig.4 for input pulse definitions.

*Complement of output under test should always be loaded with 50-ohms to ground.

*Fig.3 Switching time test circuit at +25°C*

The pulse levels shown are used to check ac parameters over the full common-mode range.

V - INPUT TO OUTPUT

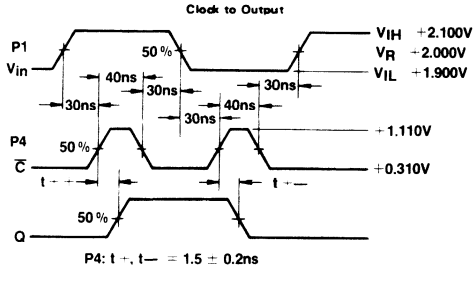



Test Pulses:
t+, t- = 1.5 ± 0.2ns (10% to 90%)
f = 5.0MHz
50% DUTY CYCLE
VIH IS APPLIED TO $\overline{C}$ DURING TESTS

**TEST PULSE LEVELS**

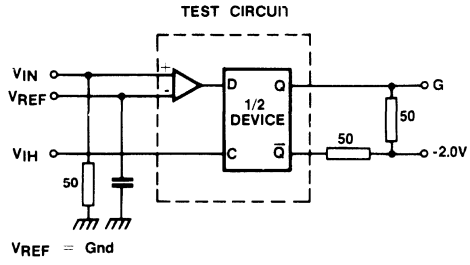
| | Pulse 1 | Pulse 2 | Pulse 3 |
|---|---|---|---|
| $V_{IH}$ | +2.100V | +5.000V | -0.300V |
| $V_R$ | +2.000V | +4.900V | -0.400V |
| $V_{IL}$ | +1.900V | +4.800V | -0.500V |

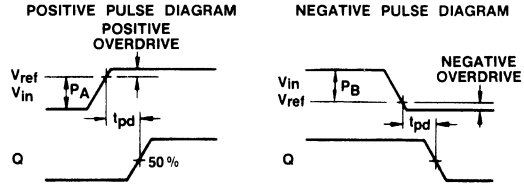
Clock to Output



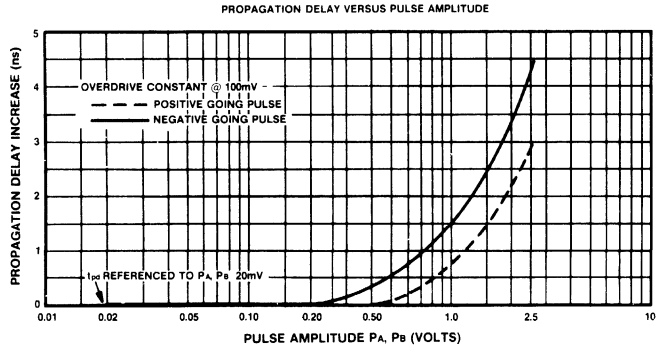

P4: t+, t— = 1.5 ± 0.2ns

*Fig.4 Switching and propagation waveforms @ 25° C*




INPUT SWITCH TIME IS CONSTANT
AT 1.5ns (10% TO 90%).



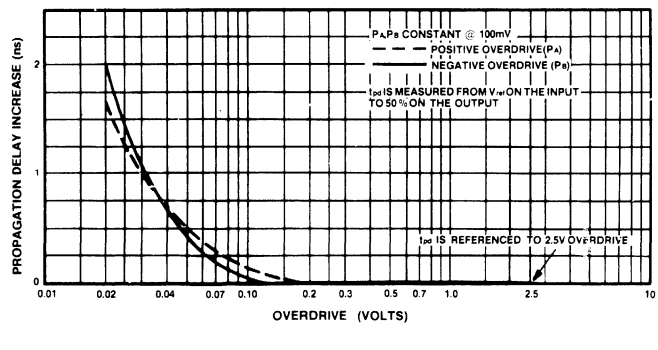




*Fig.5 Propagation delay (tpd) v. input pulse amplitude and constant overdrive*

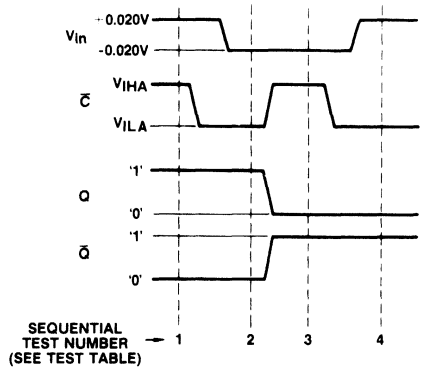



*Fig.6 Logic threshold tests (waveform sequence diagram)*

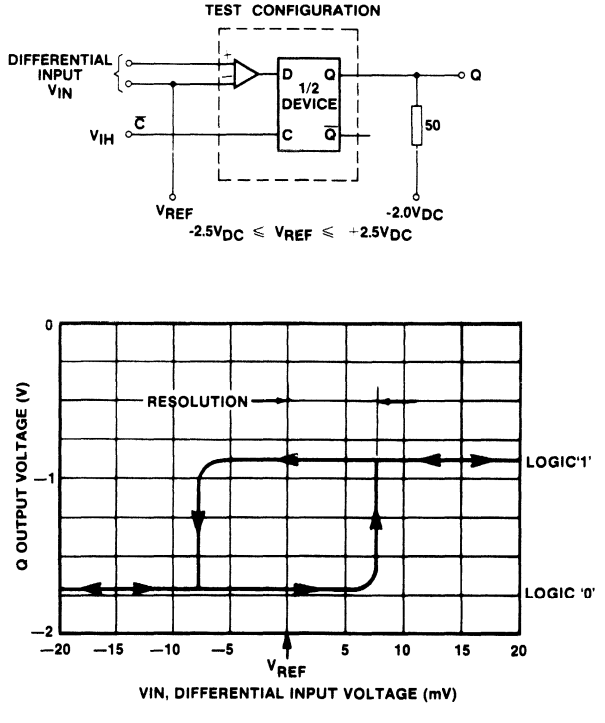



*Fig.7 Transfer characteristics (Q v. $V_{in}$)*

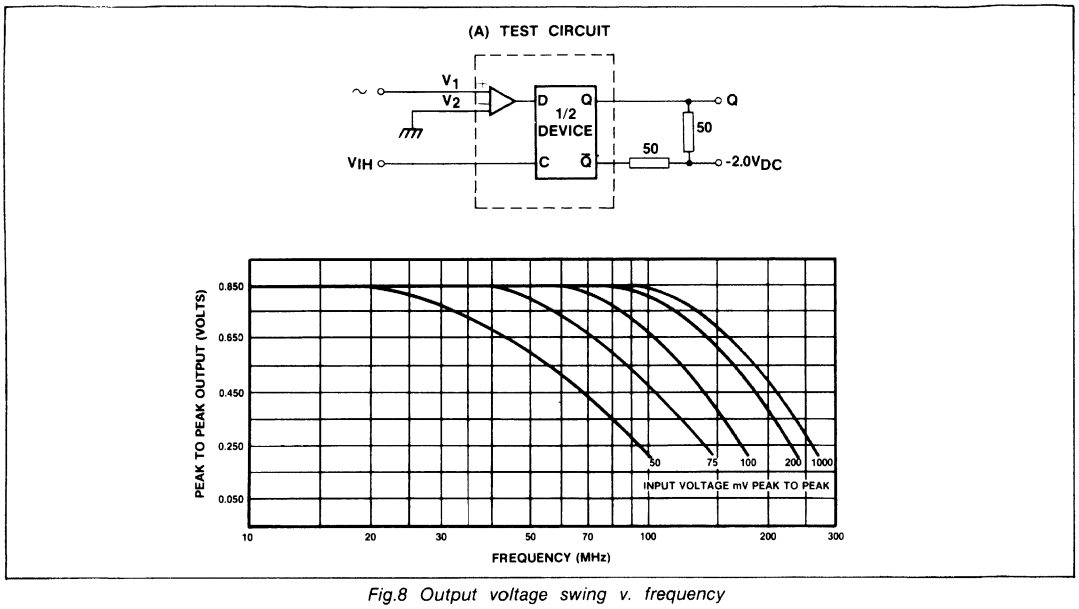



*Fig.8 Output voltage swing v. frequency*

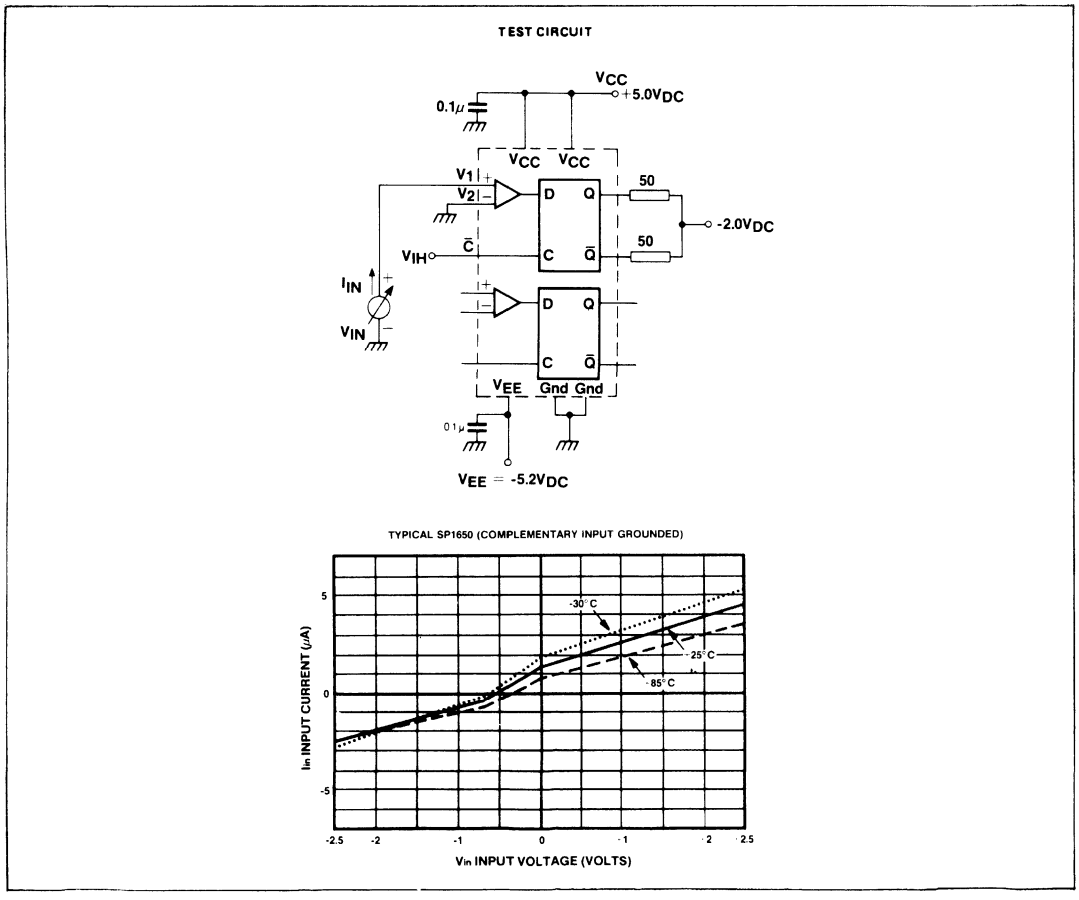
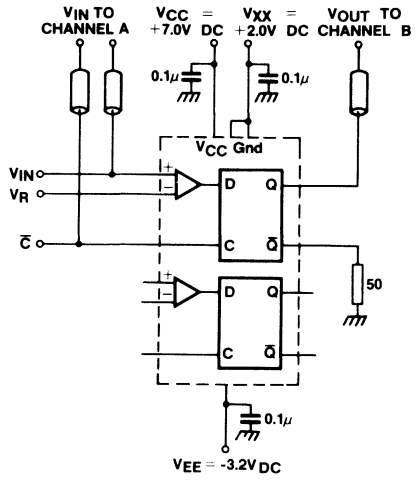


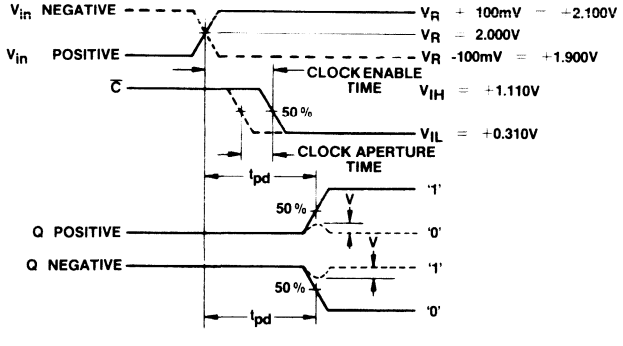

*Fig.9 Input current v. input voltage*




50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

**ANALOG SIGNAL POSITIVE AND NEGATIVE SLEW CASE**




—— Clock enable time = minimum time between analog and clock signal such that output switches, and $t_{pd}$ (analog to Q) is not degraded by more than 200ps.

---- Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150mV.

*Fig.10 Clock enable and aperture time test circuit and waveforms @ 25° C*

# SP1658

## VOLTAGE-CONTROLLED MULTIVIBRATOR

The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with ECL III and ECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The SP1658 is useful in frequency modulation, phase-locked loops, frequency synthesiser and clock signal generation applications for instrumentation, communication and computer systems.

### ORDERING INFORMATION

**SP1658DP** (Industrial - Plastic DIL package)
**SP1658DG** (Industrial - Ceramic DIL package)
**SP1658BB DG** (Plessey High Reliability Ceramic DIL package)
**SP1658LC** (Industrial - LCC package)
**SP1658MP** (Industrial - Miniature Plastic package)
**SP1658BC DG** (Military - Ceramic DIL package)

NOTE:
The BC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

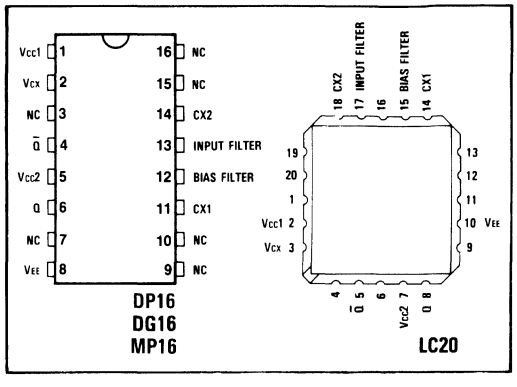



*Fig.1 Pin connections(top view)and block diagram*

### FEATURES

- Operating Temperature Range:
  -30°C to +85°C (Ceramic)
  0°C to +75°C (Plastic)
- Supply Voltages -5.2V, 0V
- Oscillator Frequency Max. 190MHz
- Voltage Controlled

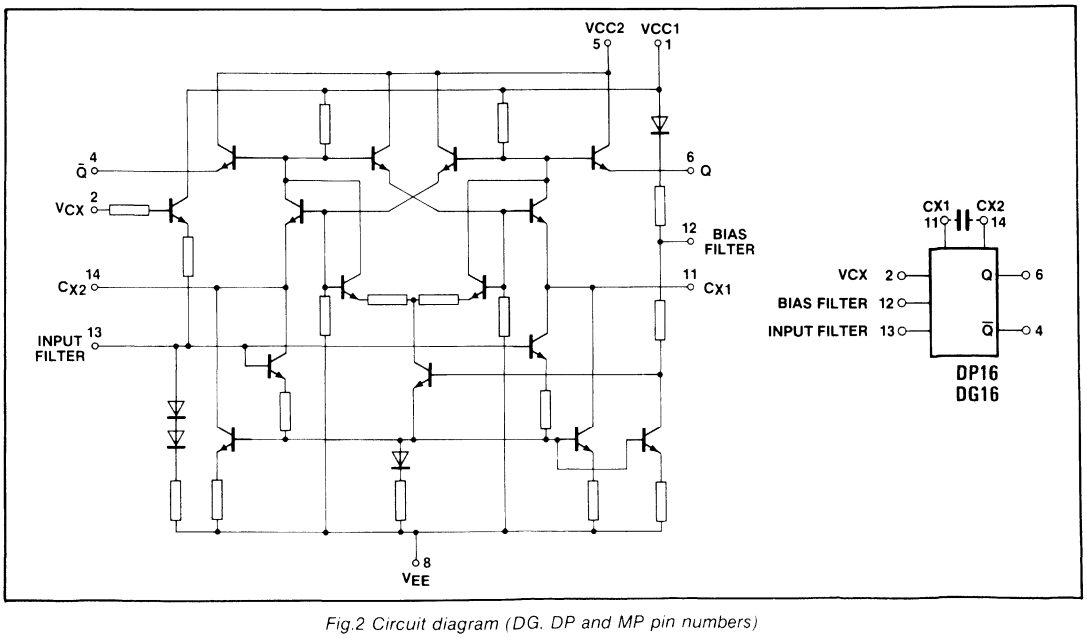



*Fig.2 Circuit diagram (DG, DP and MP pin numbers)*

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0V.

| Test temp. | TEST VOLTAGE (V) $V_{CX1}$ | $V_{CX2}$ | $V_{CX3}$ | $V_{EE}$ |
|---|---|---|---|---|
| -30°C | 0.0 | -2.0 | -1.0 | -5.2 |
| +25°C | -0.0 | -2.0 | -1.0 | -5.2 |
| +85°C | -0.0 | -2.0 | -1.0 | -5.2 |

| Characteristic | Symbol | Pin under test | SP1658 Test Limits -30°C Min. | -30°C Max. | +25°C Min. | +25°C Typ. | +25°C Max. | +85°C Min. | +85°C Max. | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{CX1}$ | $V_{CX2}$ | $V_{CX3}$ | $V_{EE}$ | $V_{CC}$ (GND) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | | | | | | | | |
| Drain current | $I_E$ | 8* | - | - | - | - | 32 | - | - | mAdc | 2 | - | - | 8 | 1,5 |
| | | 8** | - | - | - | - | 32 | - | - | mAdc | 2 | - | - | 8 | 1,5 |
| Input current | $I_{INH}$ | 2* | - | - | - | - | 350 | - | - | μAdc | 2 | - | - | 8 | 1,5 |
| Input leakage current | $I_{INL}$ | 2* | - | - | -0.5 | - | - | - | - | μAdc | - | 2 | - | 8 | 1,5 |
| High output voltage $\overline{Q}$ | $V_{OH}$ | 4* | -1.045 | -0.875 | -0.960 | - | -0.810 | -0.890 | -0.700 | Vdc | - | - | 2 | 8 | 1,5 |
| Q | | 6** | -1.045 | -0.875 | -0.960 | - | -0.810 | -0.890 | -0.700 | Vdc | - | - | 2 | 8 | 1,5 |
| Low output voltage $\overline{Q}$ | $V_{OL}$ | 4** | -1.890 | -1.650 | -1.850 | - | -1.620 | -1.830 | -1.575 | Vdc | - | - | 2 | 8 | 1,5 |
| Q | | 6* | -1.890 | -1.650 | -1.850 | - | -1.620 | -1.830 | -1.575 | Vdc | - | - | 2 | 8 | 1,5 |
| AC characteristics (Fig.3) Tests shown for one output, but checked on both | | | | | | | | | | | $C_{X1}$ | $C_{X2}$ | $V_{CX}$ +2.0V | $V_{EE}$ -3.2V | $V_{CC}$ +2.0V |
| Rise time (10 % to 90 %) | $t_+$ | 6 | - | 3.6 | - | - | 3.5 | - | 3.8 | ns | - | 11,14 | 2 | 8 | 1,5 |
| Fall time (10 % to 90 %) | $t_-$ | 6 | - | 3.1 | - | - | 3.0 | - | 3.3 | ns | - | 11,14 | 2 | 8 | 1,5 |
| Oscillator frequency | $f_{osc1}$ | - | 130 | - | 130 | 155 | 190 | 110 | - | MHz | - | 11,14 | 2 | 8 | 1,5 |
| | $f_{osc2}$ | - | - | - | 78 | 90 | 120 | - | - | MHz | 11,14 | - | 2 | 8 | 1,5 |
| Tuning ratio test † | TR | - | - | - | 3.1 | 4.5 | - | - | - | - | 11,14 | - | - | 8 | 1,5 |

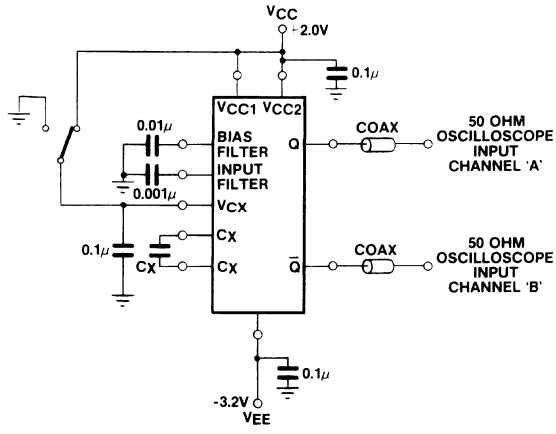
* Germanium diode (0.4 drop) forward biased from 11 to 14 (11 ——▶—— 14)

** Germanium diode (0.4 drop) forward biased from 14 to 11 (11 ——◀—— 14)

† $TR = \frac{\text{Output frequency at } V_{CX} = +2.0V}{\text{Output frequency at } V_{CX} = \text{Gnd}}$

CX1 = 10pF connected from pin 11 to pin 14

CX2 = 5pF connected from pin 11 to pin 14




The +2 and -3.2V supplies enable the output load to be connected to ground.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1 inch from $TP_{in}$ to input pin and $TP_{out}$ to output pin.

Chip capacitors are advised for the input bias filters and supply decoupling.

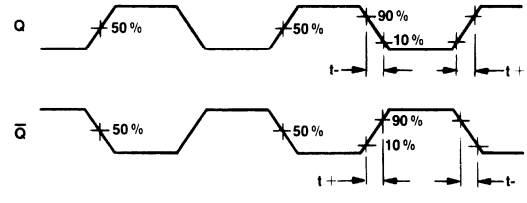



*Fig.3 Switching time test circuit and waveforms*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply | \| $V_{CC}$ - $V_{CC}$\| 8V |
| Output source current | <40mA |
| $V_{CX}$ input | -2.5 to $V_{CC}$ |
| Storage temperature range | -65°C to +150°C |
| | (Ceramic and LC) |
| | -55°C to +150°C (Plastic) |
| Operating junction temperature DG | <175°C |
| Operating junction temperature DP | <150°C |

| Thermal characteristics | |
|---|---|
| DG16 | $\theta_{JA}$ = 120°C/W |
| | $\theta_{JC}$ = 40°C/W |
| LC20 | $\theta_{JA}$ = 73°C/W |
| | $\theta_{JC}$ = 22°C/W |
| DP16 | $\theta_{JA}$ = 180°C/W |
| | $\theta_{JC}$ = 47°C/W |

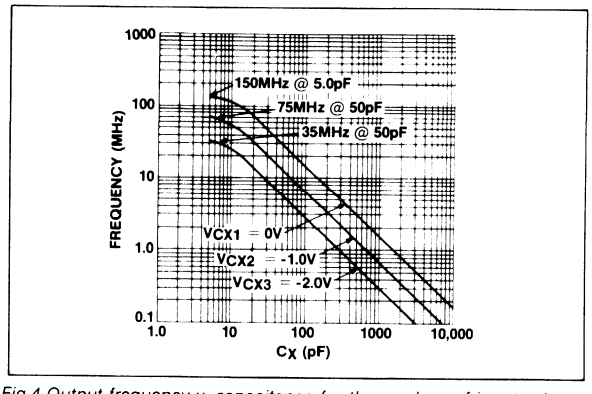



*Fig.4 Output frequency v. capacitance for three values of input voltage*

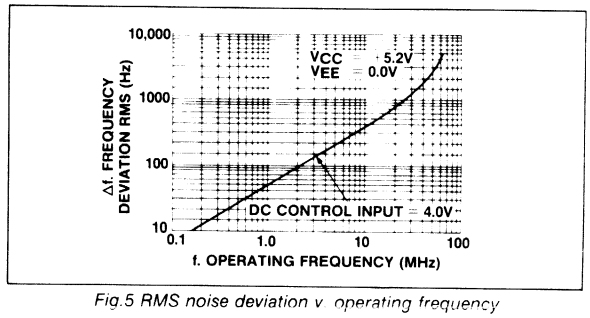



*Fig.5 RMS noise deviation v. operating frequency*

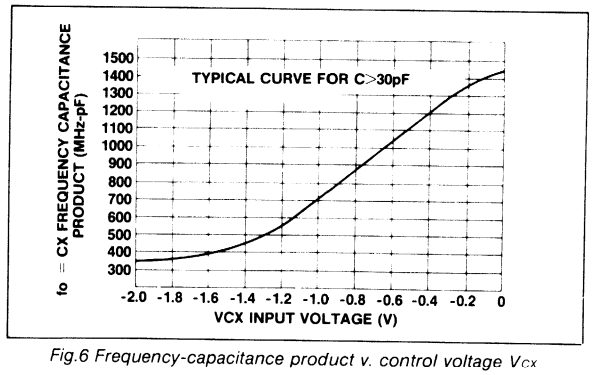



*Fig.6 Frequency-capacitance product v. control voltage $V_{CX}$*

# SP1660

## DUAL 4-INPUT OR/NOR GATE

SP1660 provides simultaneous OR-NOR output functions with the capability of driving 50 Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (-30°C to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

### FEATURES

- Operating Temperature Range -30°C to +85°C
- Gate Switching Speed 1ns Typ.
  (For higher performance see SP16F60 on page)
- ECL 10000-Compatible
- 50 ohm Line Driving Capability
- Operation with Unused I/Ps Open Circuit
- Low Supply Noise Generation

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

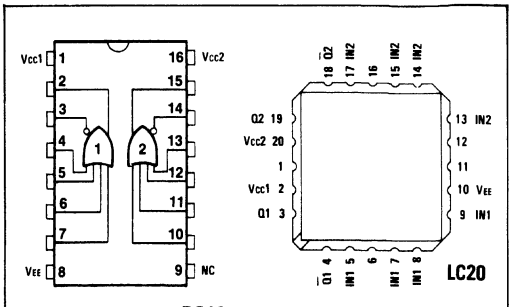



*Fig.1 Logic and pin connections (top view)*

### ORDERING INFORMATION

**SP1660DG** (Industrial - Ceramic DIL package)
**SP1660BB DG** (Plessey High Reliability Ceramic DIL package)
**SP1660LC** (Industrial - LCC package)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\|V_{CC} - V_{EE}\|$ 8V |
| Input voltages | 0V to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

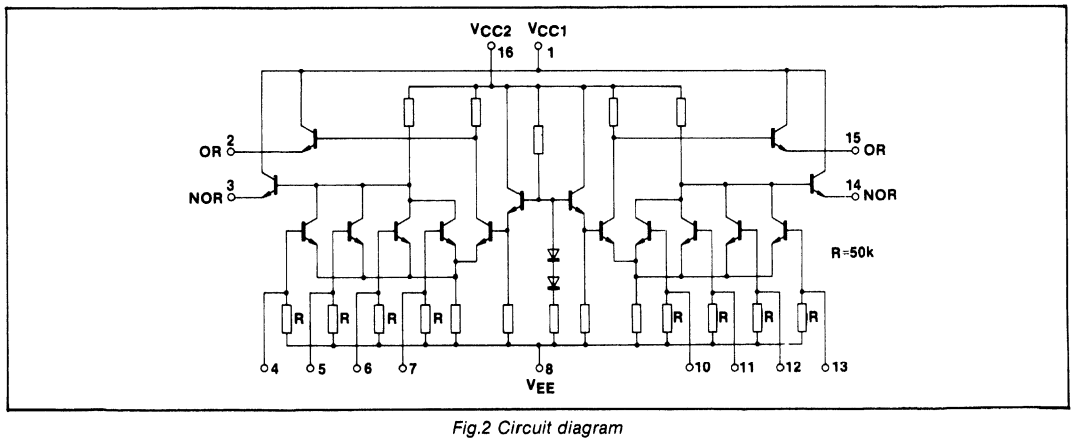



*Fig.2 Circuit diagram*

Thermal characteristics

| | |
|---|---|
| DG16 | $\theta_{JA}$ = 120°C/W |
| | $\theta_{JC}$ = 40°C/W |
| LC20 | $\theta_{JA}$ = 73°C/W |
| | $\theta_{JC}$ = 22°C/W |

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

| @ Test Temperature | TEST VOLTAGE VALUES (V) $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ |
|---|---|---|---|---|---|
| -30°C | -0.875 | -1.890 | -1.180 | -1.515 | -5.2 |
| +25°C | -0.810 | -1.850 | -1.095 | -1.485 | -5.2 |
| +85°C | -0.700 | -1.830 | -1.025 | -1.440 | -5.2 |

| Characteristic | Symbol | Pin Under Test | SP1660 Test Limits -30°C Min | -30°C Max | +25°C Min | +25°C Max | +85°C Min | +85°C Max | Units | TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ | $V_{CC}$ (Gnd) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Drain Current | $I_E$ | 8 | – | – | – | 28 | – | – | mA | – | – | – | – | 8 | 1,16 |
| Input Current | $I_{in\ H}$ | * | – | – | – | 350 | – | – | μA | * | – | – | – | 8 | 1,16 |
| | $I_{in\ L}$ | * | – | – | 0.5 | – | – | – | μA | – | * | – | – | 8 | 1,16 |
| NOR Logic 1 Output Voltage | $V_{OH}$ | 3 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | – | 4 | – | – | 8 | 1,16 |
| | | | | | | | | | | – | 5 | – | – | | |
| | | | | | | | | | | – | 6 | – | – | | |
| | | | | | | | | | | – | 7 | – | – | | |
| NOR Logic 0 Output Voltage | $V_{OL}$ | 3 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | 4 | – | – | – | 8 | 1,16 |
| | | | | | | | | | | 5 | – | – | – | | |
| | | | | | | | | | | 6 | – | – | – | | |
| | | | | | | | | | | 7 | – | – | – | | |
| OR Logic 1 Output Voltage | $V_{OH}$ | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | 4 | – | – | – | 8 | 1,16 |
| | | | | | | | | | | 5 | – | – | – | | |
| | | | | | | | | | | 6 | – | – | – | | |
| | | | | | | | | | | 7 | – | – | – | | |
| OR Logic 0 Output Voltage | $V_{OL}$ | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | – | 4 | – | – | 8 | 1,16 |
| | | | | | | | | | | – | 5 | – | – | | |
| | | | | | | | | | | – | 6 | – | – | | |
| | | | | | | | | | | – | 7 | – | – | | |
| NOR Logic 1 Threshold Voltage | $V_{OHA}$ | 3 | -1.065 | – | -0.980 | – | -0.910 | – | V | – | – | – | 4 | 8 | 1,16 |
| | | | | – | | – | | – | | – | – | – | 5 | | |
| | | | | – | | – | | – | | – | – | – | 6 | | |
| | | | | – | | – | | – | | – | – | – | 7 | | |
| NOR Logic 0 Threshold Voltage | $V_{OLA}$ | 3 | – | -1.630 | – | -1.600 | – | -1.555 | V | – | – | 4 | – | 8 | 1,16 |
| | | | – | | – | | – | | | – | – | 5 | – | | |
| | | | – | | – | | – | | | – | – | 6 | – | | |
| | | | – | | – | | – | | | – | – | 7 | – | | |
| OR Logic 1 Threshold Voltage | $V_{OHA}$ | 2 | -1.065 | – | -0.980 | – | -0.910 | – | V | – | – | 4 | – | 8 | 1,16 |
| | | | | – | | – | | – | | | | 5 | | | |
| | | | | – | | – | | – | | – | – | 6 | – | | |
| | | | | – | | – | | – | | – | – | 7 | – | | |
| OR Logic 0 Threshold Voltage | $V_{OLA}$ | 2 | – | -1.630 | – | -1.600 | – | -1.555 | V | – | – | – | 4 | 8 | 1,16 |
| | | | – | | – | | – | | | – | – | – | 5 | | |
| | | | – | | – | | – | | | – | – | – | 6 | | |
| | | | – | | – | | – | | | – | – | – | 7 | | |
| Switching Times (50Ω Load) | | | | | | | | | | Pulse In | Pulse Out | | | -3.2V | +2.0V |
| Propagation Delay | $t_{4+3-}$ | 3 | – | 1.8 | – | 1.7 | – | 1.9 | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{4-2-}$ | 2 | – | 1.8 | – | 1.7 | – | 1.9 | | | 2 | – | – | | |
| | $t_{4+2+}$ | 2 | – | 1.6 | – | 1.5 | – | 1.7 | | | 2 | – | – | | |
| | $t_{4-3+}$ | 3 | – | 1.6 | – | 1.5 | – | 1.7 | | | 3 | – | – | | |
| Rise Time | $t_{3+}$ | 3 | – | 2.2 | – | 2.1 | – | 2.3 | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{2+}$ | 2 | – | 2.2 | – | 2.1 | – | 2.3 | ns | 4 | 2 | – | – | 8 | 1,16 |
| Fall Time | $t_{3-}$ | 3 | – | 2.2 | – | 2.1 | – | 2.3 | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{2-}$ | 2 | – | 2.2 | – | 2.1 | – | 2.3 | ns | 4 | 2 | – | – | 8 | 1,16 |

* Individually test each input applying $V_{IH}$ or $V_{IL}$ to the input under test

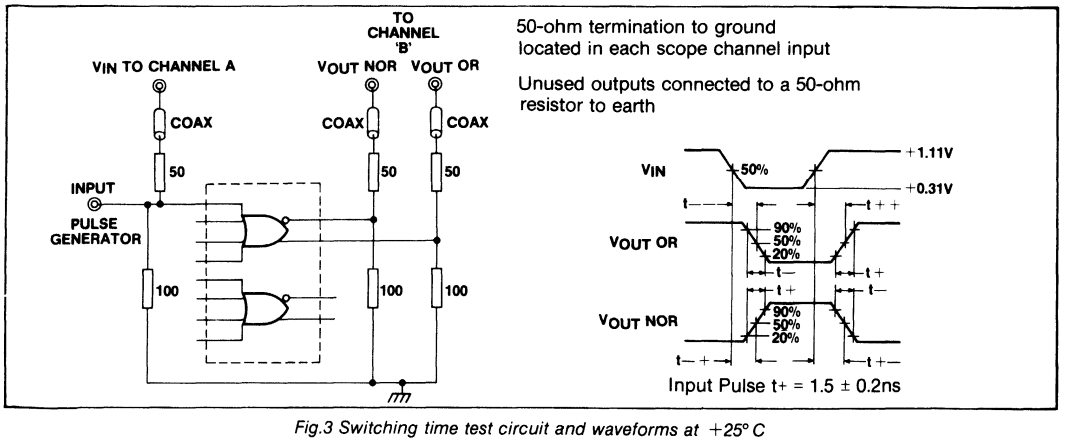



*Fig.3 Switching time test circuit and waveforms at +25° C*

# SP1662

## QUAD 2-INPUT NOR GATE

The SP1662 comprises four 2-input OR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to VEE.

### FEATURES

- Gate Switching Speed 1ns Typ.
- ECL II and ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

### ORDERING INFORMATION

**SP1662DG** (Industrial - Ceramic DIL package)

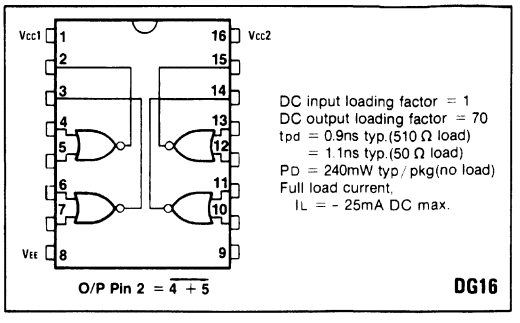



*Fig.1 Logic diagram*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | \|VCC - VEE\| 8V |
| Input voltages | 0V to VEE |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

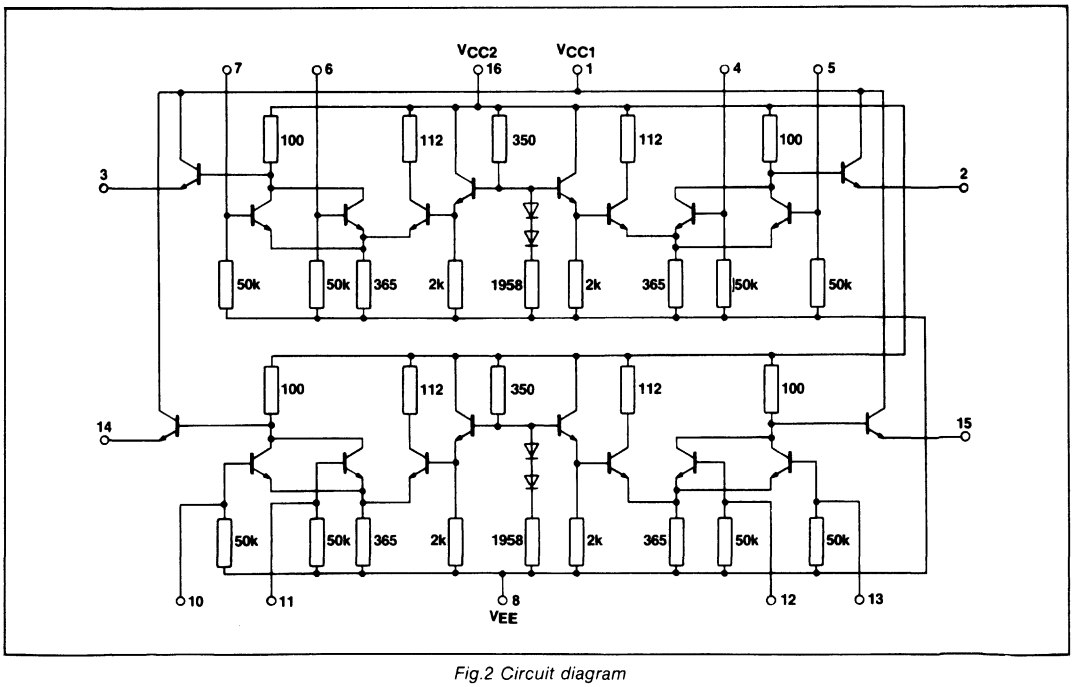



*Fig.2 Circuit diagram*

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

| TEST VOLTAGE (V) | | | | | |
|---|---|---|---|---|---|
| Test temp. | $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ |
| -30° C | -0.875 | -1.890 | -1.180 | -1.515 | -5.2 |
| +25° C | -0.810 | -1.850 | -1.095 | -1.485 | -5.2 |
| +85° C | -0.700 | -1.830 | -1.025 | -1.440 | -5.2 |

| SP1662 Test Limits | | | | | | | | | | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Characteristic | Symbol | Pin under test | -30° C | | +25° C | | +85° C | | Unit | $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ | GND |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | | | | | | |
| **POWER SUPPLY** | | | | | | | | | | | | | | | |
| Drain current | $I_E$ | 8 | - | - | - | 56 | - | - | mA | - | - | - | - | 8 | 1,16 |
| Input current | $I_{INH}$ | * | - | - | - | 350 | - | - | μA | * | - | - | - | 8 | 1,16 |
| | $I_{INL}$ | * | - | - | 0.5 | - | - | - | μA | - | * | - | - | 8 | 1,16 |
| Logic '1' output voltage | $V_{OH}$ | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | - | 4 | - | - | 8 | 1,16 |
| | | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | - | 5 | - | - | 8 | 1,16 |
| Logic '0' output voltage | $V_{OL}$ | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | 4 | - | - | - | 8 | 1,16 |
| | | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | 5 | - | - | - | 8 | 1,16 |
| Logic '0' threshold voltage | $V_{OHA}$ | 2 | -1.065 | - | -0.980 | - | -0.910 | - | V | - | - | - | 4 | 8 | 1,16 |
| | | 2 | -1.065 | - | -0.980 | - | -0.910 | - | V | - | - | - | 5 | 8 | 1,16 |
| Logic '0' threshold voltage | $V_{OLA}$ | 2 | - | -1.630 | - | -1.600 | - | -1.555 | V | - | - | 4 | - | 8 | 1,16 |
| | | 2 | - | -1.630 | - | -1.600 | - | -1.555 | V | - | - | 5 | - | 8 | 1,16 |
| **SWITCHING TIME (50 ohm load)** | | | | | | | | | | **Pulse in** | **Pulse out** | | | **-3.2V** | **+2.0V** |
| Propagation delay | $t_{4+2+}$ | 2 | - | 1.6 | - | 1.5 | - | 1.7 | ns | 4 | 2 | - | - | 8 | 1,16 |
| | $t_{4-2-}$ | 2 | - | 1.8 | - | 1.7 | - | 1.9 | ns | 4 | 2 | - | - | 8 | 1,16 |
| Rise time | $t_{2+}$ | 2 | - | 2.2 | - | 2.1 | - | 2.3 | ns | 4 | 2 | - | - | 8 | 1,16 |
| Fall time | $t_{2-}$ | 2 | - | 2.2 | - | 2.1 | - | 2.3 | ns | 4 | 2 | - | - | 8 | 1,16 |

* Individually test each input applying $V_{IH}$ or $V_{IL}$ to input under test.

Thermal characteristics $\theta_{JA} = 120°$ C/W
$\theta_{JC} = 40°$ C/W

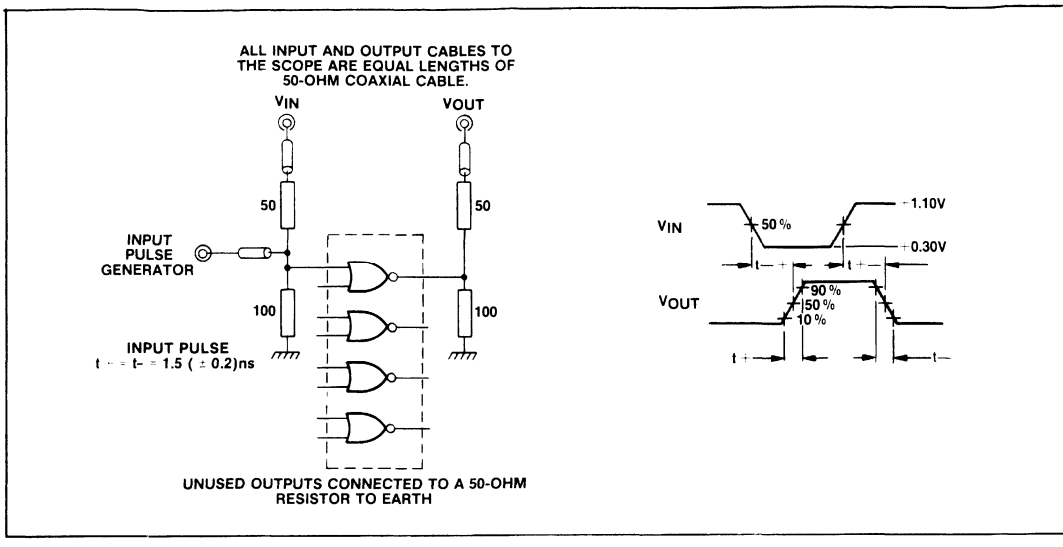



*Fig.3 Switching time test circuit and waveforms at + 25 °C*

PLESSEY
Semiconductors

# SP1664

## QUAD 2-INPUT OR GATE

The SP1664 comprises four 2-input OR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

### FEATURES

- Gate Switching Speed 1ns Typ.
- ECL II and ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation with Unused I/Ps Open Circuit
- Low Supply Noise Generation

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

### ORDERING INFORMATION

**SP1664DG** (Industrial - Ceramic DIL package)

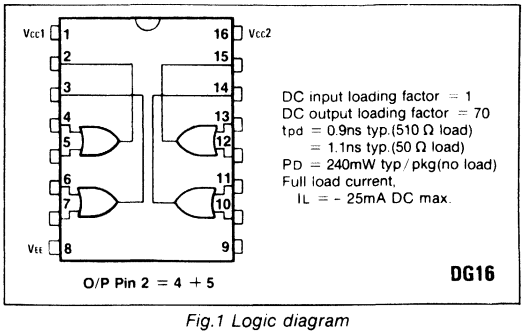



*Fig.1 Logic diagram*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\lvert V_{CC} - V_{EE} \rvert$ 8V |
| Input voltages | 0V to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

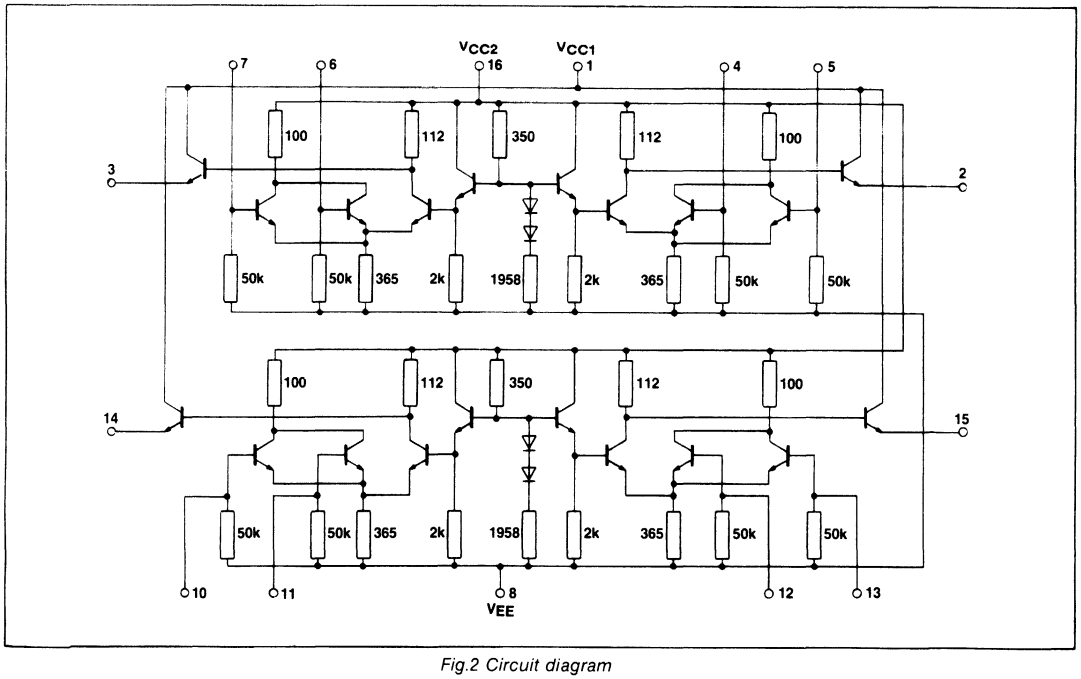



*Fig.2 Circuit diagram*

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

| TEST VOLTAGE (V) | | | | | |
|---|---|---|---|---|---|
| Test temp. | $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ |
| -30° C | -0.875 | -1.890 | -1.180 | -1.515 | -5.2 |
| +25° C | -0.810 | -1.850 | -1.095 | -1.485 | -5.2 |
| +85° C | -0.700 | -1.830 | -1.025 | -1.440 | -5.2 |

| SP1664 Test Limits | | | | | | | | | | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Characteristic | Symbol | Pin under test | -30° C | | +25° C | | +85° C | | Unit | $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ | GND |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | | | | | | |
| **POWER SUPPLY** | | | | | | | | | | | | | | | |
| Drain current | $I_E$ | 8 | - | - | - | 56 | - | - | mA | - | - | - | - | 8 | 1,16 |
| Input current | $I_{INH}$ | * | - | - | - | 350 | - | - | μA | * | - | - | - | 8 | 1,16 |
| | $I_{INL}$ | * | - | - | 0.5 | - | - | - | μA | - | * | - | - | 8 | 1,16 |
| Logic '1' output voltage | $V_{OH}$ | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | 4 | - | - | - | 8 | 1,16 |
| | | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | 5 | - | - | - | 8 | 1,16 |
| Logic '0' output voltage | $V_{OL}$ | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | - | 4 | - | - | 8 | 1,16 |
| | | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | - | 5 | - | - | 8 | 1,16 |
| Logic '0' threshold voltage | $V_{OHA}$ | 2 | -1.065 | - | -0.980 | - | -0.910 | - | V | - | - | 4 | - | 8 | 1,16 |
| | | 2 | -1.065 | - | -0.980 | - | -0.910 | - | V | - | - | 5 | - | 8 | 1,16 |
| Logic '0' threshold voltage | $V_{OLA}$ | 2 | - | -1.630 | - | -1.600 | - | -1.555 | V | - | - | - | 4 | 8 | 1,16 |
| | | 2 | - | -1.630 | - | -1.600 | - | -1.555 | V | - | - | - | 5 | 8 | 1,16 |
| **SWITCHING TIME (50 ohm load)** | | | | | | | | | | **Pulse in** | **Pulse out** | | | **-3.2V** | **+2.0V** |
| Propagation delay | $t_{4+2+}$ | 2 | - | 1.6 | - | 1.5 | - | 1.7 | ns | 4 | 2 | - | - | 8 | 1,16 |
| | $t_{4-2-}$ | 2 | - | 1.8 | - | 1.7 | - | 1.9 | ns | 4 | 2 | - | - | 8 | 1,16 |
| Rise time | $t_{2+}$ | 2 | - | 2.2 | - | 2.1 | - | 2.3 | ns | 4 | 2 | - | - | 8 | 1,16 |
| Fall time | $t_{2-}$ | 2 | - | 2.2 | - | 2.1 | - | 2.3 | ns | 4 | 2 | - | - | 8 | 1,16 |

* Individually test each input applying $V_{IH}$ or $V_{IL}$ to input under test.

Thermal characteristics $\theta_{JA} = 120°$ C/W
$\theta_{JC} = 40°$ C/W

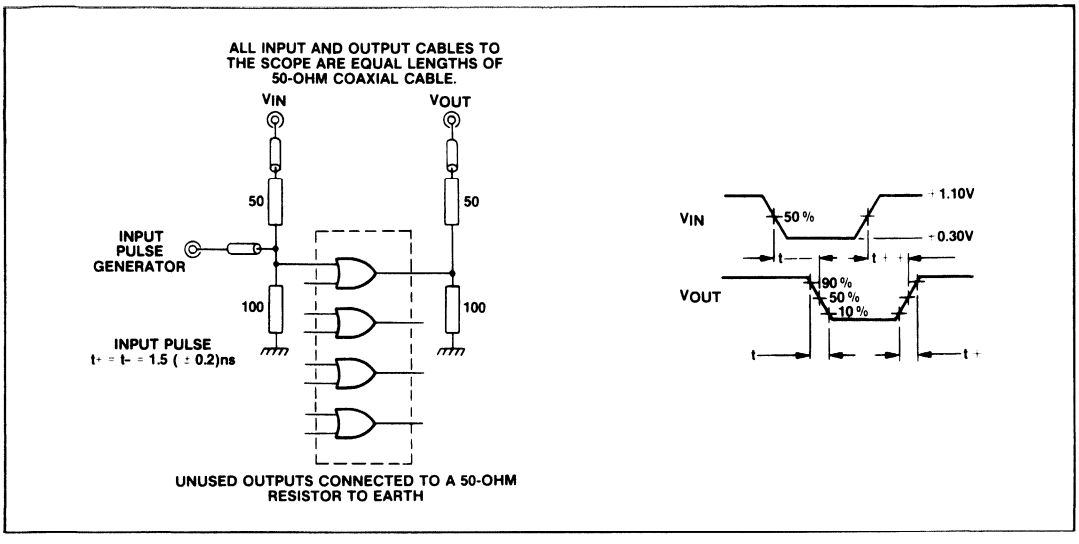



*Fig.3 Switching time test circuit and waveforms at + 25 °C*

# SP1670

## MASTER/SLAVE TYPE D FLIP-FLOP

The SP1670 is a D-type Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

### FEATURES

- Operating Temperature Range -30°C to +85°C
- Toggle Frequency 300MHz
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

### ORDERING INFORMATION

**SP1670DG** (Industrial - Ceramic DIL package)
**SP1670LC** (Industrial - LCC package)
**SP1670 BB DG** (Plessey High Reliability Ceramic DIL package)
**SP16F70BC DG** (Military - Ceramic DIL package)

NOTE:
The BC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510. Please consult your nearest Plessey sales office for availability of separately published data.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\lvert V_{CC} - V_{EE} \rvert$ 8V |
| Input voltages | $V_{CC}$ to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

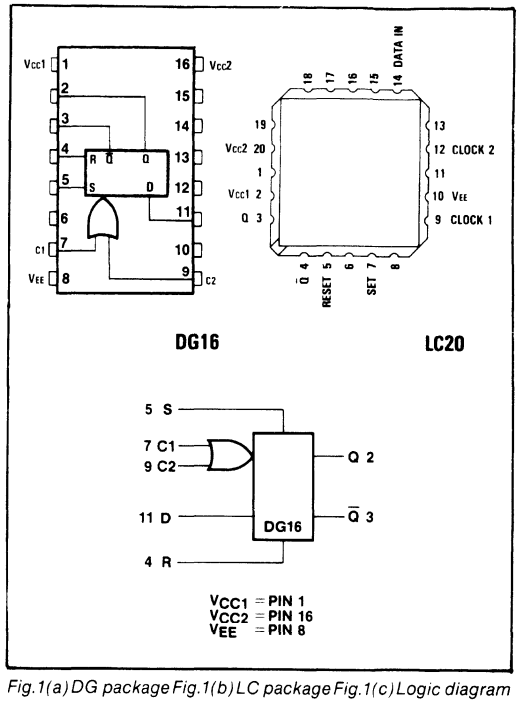



*Fig.1(a) DG package Fig.1(b) LC package Fig.1(c) Logic diagram*

**TRUTH TABLE**

| R | S | D | C | $Q_{n+1}$ |
|---|---|---|---|---|
| L | H | Φ | Φ | H |
| H | L | Φ | Φ | L |
| H | H | Φ | Φ | ND |
| L | L | L | L | $Q_n$ |
| L | L | L | | L |
| L | L | L | H | $Q_n$ |
| L | L | H | L | $Q_n$ |
| L | L | H | | H |
| L | L | H | H | $Q_n$ |

Φ = Don't Care
ND = Not Defined
C = C1 + C2

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifictions shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0V.

| Test temp. | TEST VOLTAGE (V) $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Max. | $V_{ILA}$ Max. | $V_{EE}$ |
|---|---|---|---|---|---|
| -30° C | -0.875 | -1.890 | -1.180 | -1.515 | -5.2 |
| +25° C | -0.810 | -1.850 | -1.095 | -1.485 | -5.2 |
| +85° C | -0.700 | -1.830 | -1.025 | -1.440 | -5.2 |

| Characteristic | Symbol | Pin under test | SP1670 Test Limits -30° C Min. | -30° C Max. | +25° C Min. | +25° C Max. | +85° C Min. | +85° C Max. | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ | $P_1$ | $P_2$ | $P_3$ | $V_{CC}$ Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | | | | | | | | | | | |
| Drain current | $I_E$ | 8 | - | - | - | 48 | - | - | mAdc | 7.9 | - | - | - | 8 | - | - | - | 1.16 |
| Input current | $I_{INH}$ | 4 | - | - | - | 550 | - | - | μAdc | 4 | - | - | - | 8 | - | - | - | 1.16 |
| | | 5 | - | - | - | 550 | - | - | | 5 | - | - | - | | - | - | - | |
| | | 9 | - | - | - | 250 | - | - | | 9 | - | - | - | | - | - | - | |
| | | 7 | - | - | - | 250 | - | - | | 7 | - | - | - | | - | - | - | |
| | | 11 | - | - | - | 270 | - | - | | 11 | - | - | - | | - | - | - | |
| | $I_{INL}$ | 4 | - | - | 0.5 | - | - | - | μAdc | 9 | 4 | - | - | 8 | - | - | - | 1.16 |
| | | 5 | - | - | | - | - | - | | 9 | 5 | - | - | | - | - | - | |
| | | 9 | - | - | | - | - | - | | 7 | 9 | - | - | | - | - | - | |
| | | 7 | - | - | | - | - | - | | 9 | 7 | - | - | | - | - | - | |
| | | 11 | - | - | | - | - | - | | 9 | 11 | - | - | | - | - | - | |
| Logic 1 output voltage | $V_{OH}$ | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | Vdc | - | 4,7,11 | - | - | 8 | 9 | 5 | - | 1.16 |
| | | 3 | | | | | | | | 11 | 5,9 | - | - | | 7 | 4 | - | |
| | | 2 | | | | | | | | 11 | 5,7 | - | - | | 4 | 9 | - | |
| | | 3 | | | | | | | | - | 4,9,11 | - | - | | 5 | 7 | - | |
| Logic 0 output voltage | $V_{OL}$ | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | Vdc | 11 | 5,7 | - | - | 8 | 9 | 4 | - | 1.16 |
| | | 3 | | | | | | | | - | 4,9,11 | - | - | | 7 | 5 | - | |
| | | 2 | | | | | | | | - | 4,7,11 | - | - | | 5 | 9 | - | |
| | | 3 | | | | | | | | 11 | 5,9 | - | - | | 4 | 7 | - | |
| Logic 1 threshold voltage | $V_{IHA}$ | 2 | -1.065 | - | -0.980 | - | -0.910 | - | Vdc | 4,7,11 | - | - | 8 | 9 | - | 5 | 1.16 | |
| | | 3 | | - | | - | | - | | 11 | 5,9 | - | - | | 7 | - | 4 | |
| | | 2 | | - | | - | | - | | 11 | 5,7 | - | - | | 4 | - | 9 | |
| | | 3 | | - | | - | | - | | - | 4,9,11 | - | - | | 5 | - | 7 | |
| | | 2 | | - | | - | | - | | - | 5,7 | 11 | - | | 4 | 9 | - | |
| | | 3 | | - | | - | | - | | - | 4,9 | - | 11 | | 5 | 7 | - | |
| Logic 0 threshold voltage | $V_{ILA}$ | 2 | - | -1.630 | - | 1.600 | - | 1.555 | Vdc | 11 | 5,7 | - | - | 8 | 9 | - | 4 | 1.16 |
| | | 3 | - | | - | | - | | | - | 4,9,11 | - | - | | 7 | - | 5 | |
| | | 2 | - | | - | | - | | | - | 4,7,11 | - | - | | 5 | - | 9 | |
| | | 3 | - | | - | | - | | | 11 | 5,9 | - | - | | 4 | - | 7 | |
| | | 2 | - | | - | | - | | | - | 4,7 | - | 11 | | 5 | 9 | - | |
| | | 3 | - | | - | | - | | | - | 5,9 | 11 | - | | 4 | 7 | - | |
| Switching parameters | | | | | | | | | | | | | | -3.2 Vdc | | | | -2.0 Vdc |
| Clock to output delay | $t_{9,2}$ | 9,2 | 1.0 | 2.7 | 1.1 | 2.5 | 1.1 | 2.9 | ns | - | - | - | - | 8 | - | - | - | 1.16 |
| (See Fig.1) | $t_{9,2}$ | 9,2 | | | | | | | | - | - | - | - | | - | - | - | |
| | $t_{9,3}$ | 9,3 | | | | | | | | - | - | - | - | | - | - | - | |
| | $t_{9,3}$ | 9,3 | | | | | | | | - | - | - | - | | - | - | - | |
| Set to output delay | $t_{5,2}$ | 5,2 | | | | | | | | - | - | - | - | | - | - | - | |
| (See Fig.2) | $t_{5,3}$ | 5,3 | | | | | | | | - | - | - | - | | - | - | - | |
| Reset to output delay | $t_{4,2}$ | 4,2 | | | | | | | | - | - | - | - | | - | - | - | |
| (See Fig.2) | $t_{4,3}$ | 4,3 | | | | | | | | - | - | - | - | | - | - | - | |
| Output | | | | | | | | | | | | | | | | | | |
| Rise time | $t_{2-,t3}$ | 2,3 | 0.9 | 2.7 | 1.0 | 2.5 | 1.0 | 2.9 | | - | - | - | - | | - | - | - | |
| Fall time (See Fig.2) | $t_{2-,t3}$ | 2,3 | 0.5 | 2.1 | 0.6 | 1.9 | 0.6 | 2.3 | | - | - | - | - | | - | - | - | |
| Set up time | $t_{s'1'}$ | 2 | - | - | - | 0.4 | - | - | | - | - | - | - | | - | - | - | |
| (See Fig.3) | $t_{s'0'}$ | 2 | - | - | - | 0.5 | - | - | | - | - | - | - | | - | - | - | |
| Hold time | $t_{H'1'}$ | 2 | - | - | - | 0.3 | - | - | | - | - | - | - | | - | - | - | |
| (See Fig.3) | $t_{H'0'}$ | 2 | - | - | - | 0.5 | - | - | | - | - | - | - | | - | - | - | |
| Toggle frequency (See Fig.4) | $f_{TOG}$ | 2 | 270 | - | 300 | - | 270 | - | MHz | - | - | - | - | | - | - | - | - |

Thermal characteristics

DG16 $\theta_{JA} = 110°C/W$
$\theta_{JC} = 33°C/W$

LC20 $\theta_{JA} = 72°C/W$
$\theta_{JC} = 22°C/W$

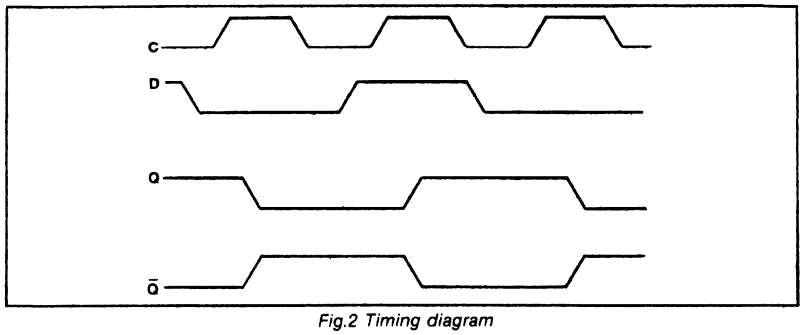



*Fig.2 Timing diagram*

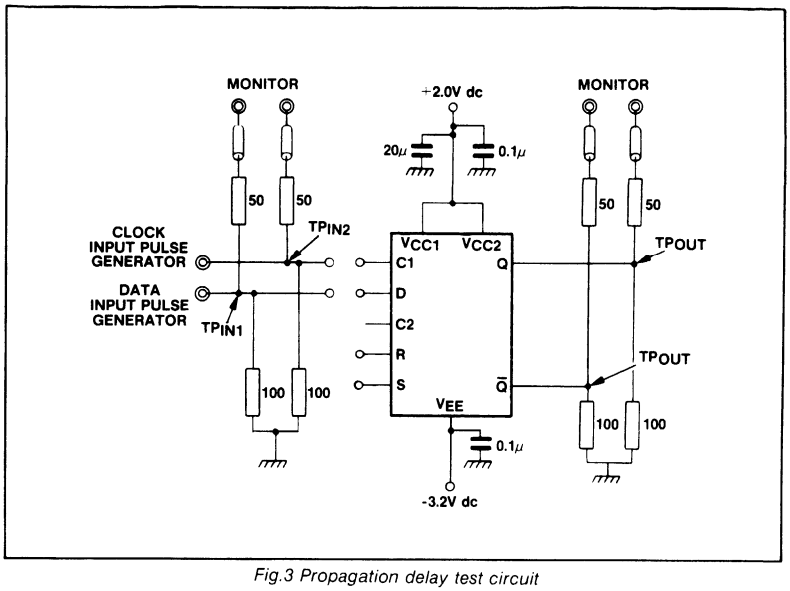



*Fig.3 Propagation delay test circuit*

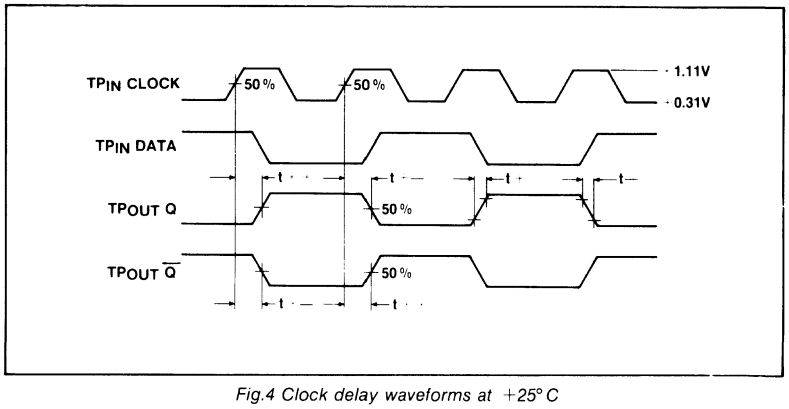



*Fig.4 Clock delay waveforms at +25° C*

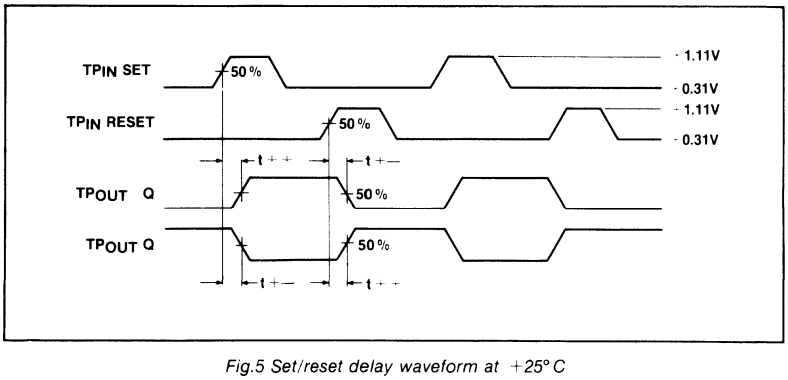



*Fig.5 Set/reset delay waveform at +25° C*

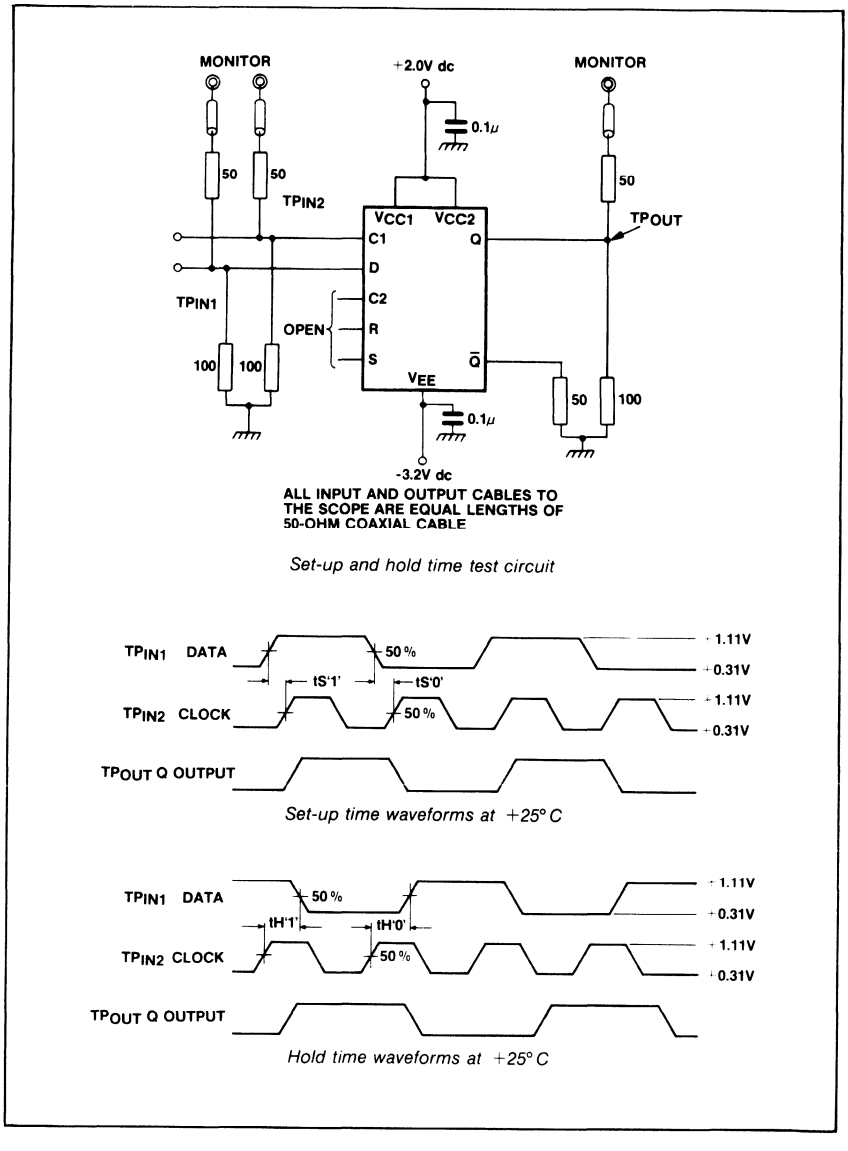



*Fig.6 Set-up and hold time test circuit*

Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock (C) that information must remain unchanged at the data (D) input.

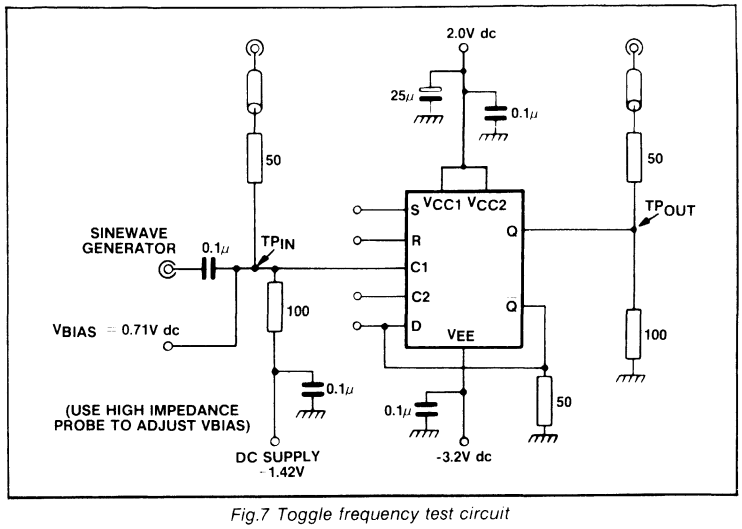



*Fig.7 Toggle frequency test circuit*

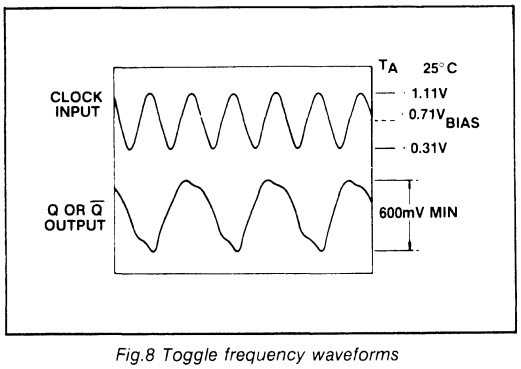



*Fig.8 Toggle frequency waveforms*

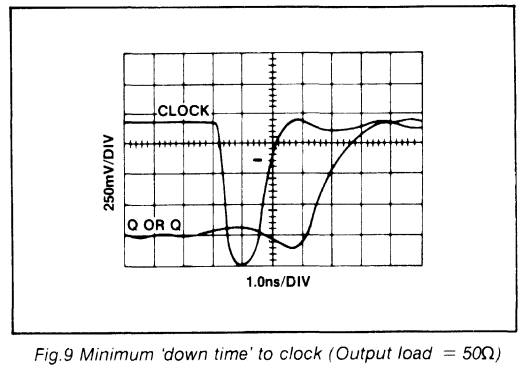



*Fig.9 Minimum 'down time' to clock (Output load = 50Ω)*

The maximum toggle frequency of the SP1670 has been exceed when either:

1. The output peak-to-peak voltage swing falls below 600mV OR
2. The device ceases to toggle (divide by two). $V_{Bias}$ is defined by the test circuit Fig.7 and by the waveform in Fig.8.

Figs.9 and 10 illustrate minimum clock pulse width recommended for reliable operation of the SP1670.

| Temperature | -30°C | +25°C | +85°C |
|---|---|---|---|
| $V_{Bias}$ | +0.660V | +0.710V | +0.765V |

*Table 1 Variation of $V_{Bias}$ with temperature*

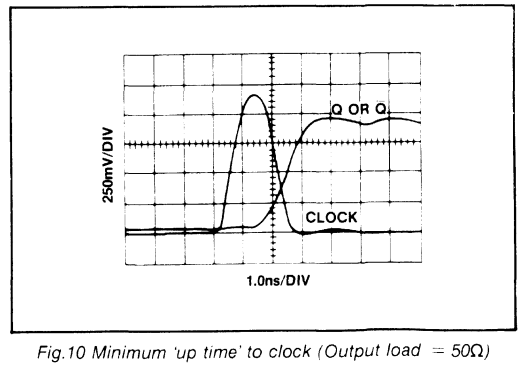



*Fig.10 Minimum 'up time' to clock (Output load = 50Ω)*

## Operation of the Master-Slave Type D Flip-Flop

In the circuit of Fig.11 assume that initially Q, C, R, S and D are at 0 levels and that Q is at the 1 level. Since the clock is low, transistors TR3 and TR22 are conducting. In the slave section only transistors TR25 and TR26 are in series with TR22. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through TR3 and TR9.

Now assume that the data input goes high. The high-input signal on the base of TR4 causes it to conduct, and TR9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base and therefore on the emitter of TR11. Since there is essentially no current flow through RC2, the base of transistor TR10 is in a high state. This is reflected in the emitter, and in turn is transferred to the base of TR6. TR6 is biased for conduction but, since there is no current path, does not conduct.

Now allow the clock to go high. As the clock signal rises, transistor TR2 turns on and transistor TR3 turns off. This provides a current path for the common-emitter transistors TR5, TR6, TR7 and TR8. Since the bases of all these devices except TR6 are in the low state, current flow is through TR6. This maintains the base and emitter of TR11 low, and the base and emitter of TR10 high. The high state on TR10 is transferred to TR23 of the slave section. As the clock continues to rise TR21 begins to turn on and TR22 to turn off. (Reference voltages in the master and slave units are slightly offset to ensure prior clocking of the master section.) With transistor TR21 conducting and the base of TR23 in a high state, the current path now includes TR21, TR23, and resistor RC3. The voltage drop across the resistor places a low state voltage on the base, and therefore the emitter, of TR30. The lack of current flow through RC4 causes a high state input to the base of TR29. These states are fed back to the latch transistors, TR25 and TR26.

As the clock voltage falls, transistor TR21 turns off and TR22 turn on. This provides a current path through the latch transistors, locking-in the slave output.

In the master section the falling clock voltage turns on transistor TR3 and turns off TR2. This enables the input transistor TR4 so that the master section will again track the D input.

The separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs TR2:TR3 and TR21:TR22. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors TR23 and TR28. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly if the D input changes at this time (such as in a counting operation where the Q output is tied back to D). The offsetting resistor also allows a relatively slow-rising clock wveform to be used without the danger of losing information during the transition of the clock.

The set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, TR2 begins to conduct because its base is now being driven through TR19 which is in turn connected to S. Transistor TR5 is now on and the feedback devices TR6 and TR7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors TR21, TR24, TR25, and TR26.

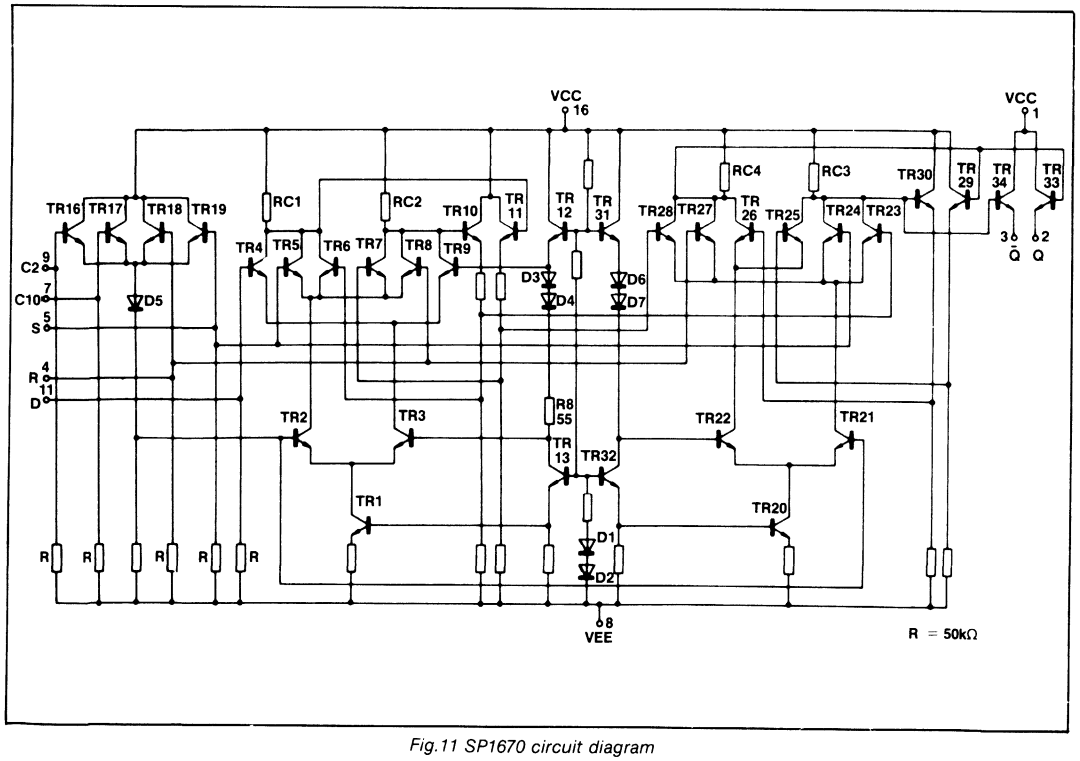



*Fig.11 SP1670 circuit diagram*

# SP1692

## QUAD LINE RECEIVER

Four differential amplifiers with emitter follower outputs are provided.

The device can be configured as a differential line receiver or by using the internal $V_{BB}$ reference single ended ECL signals can be received. The SP1692 is also ideally suited for use in expanding the fan out of ECL circuits, or inverting ECL logic.

### FEATURES

- ECL 10000 Compatible
- 50Ω Line Driving Capability
- Single or Differential Operation
- Operating Temperature Range -30°C to +85°C

### ORDERING INFORMATION

**SP1692DG** (Industrial - Ceramic DIL package)
**SP1692BB DG** (Plessey High Reliability Ceramic DIL package)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\lvert V_{CC} - V_{EE} \rvert$ 8V |
| Input voltages | 0V to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

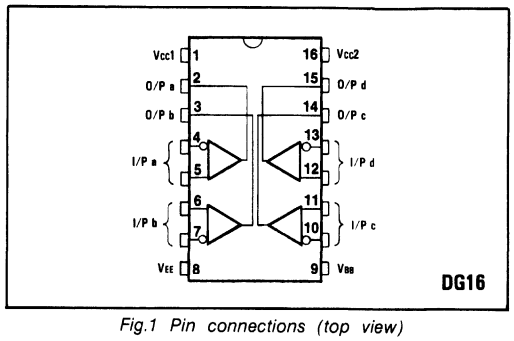



*Fig.1 Pin connections (top view)*

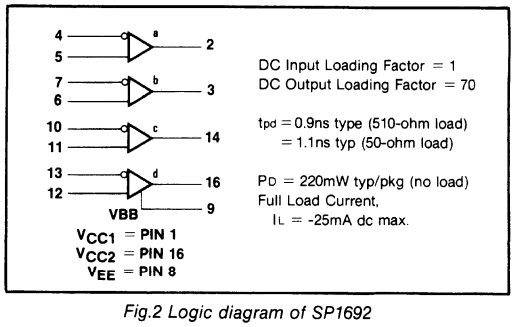



*Fig.2 Logic diagram of SP1692*

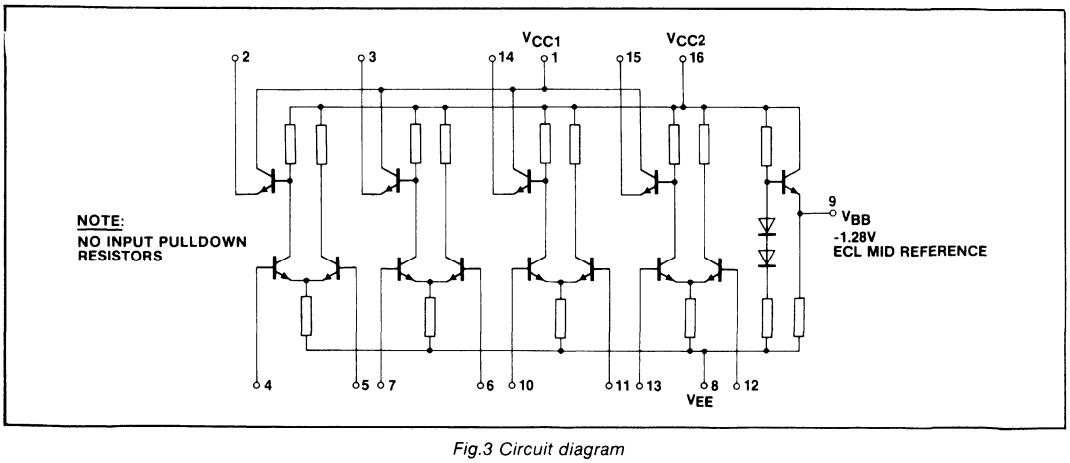



*Fig.3 Circuit diagram*

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0V dc.

| Test temp. | TEST VOLTAGE (V) $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{BB}$ | $V_{EE}$ |
|---|---|---|---|---|---|---|
| -30° C | -0.875 | -1.890 | -1.180 | -1.515 | From | -5.2 |
| +25° C | -0.810 | -1.850 | -1.095 | -1.485 | Pin | -5.2 |
| +85° C | -0.700 | -1.830 | -1.025 | -1.440 | 9 | -5.2 |

| Characteristic | Symbol | Pin under test | SP1692 Test Limits -30° C Min. | -30° C Max. | +25° C Min. | +25° C Max. | +85° C Min. | +85° C Max. | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{BB}$ | $V_{EE}$ | $V_{CC}$ (GND) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | | | | | | | | | |
| Drain current | $I_{EE}$ | 8 | - | - | - | 50 | - | - | mAdc | - | 4,7,10,13 | - | - | 5,6,11,12 | 8 | 1,16 |
| Input current | $I_{INH}$ | 4 | - | - | - | 250 | - | - | μAdc | 4 | 7,10,13 | - | - | 5,6,11,12 | 8 | 1,16 |
| Input leakage current | $I_{INL}$ | 4 | - | - | | 100 | - | - | μAdc | - | 7,10,13 | - | - | 5,6,11,12 | 8,4 | 1,16 |
| Logic '1' output voltage | $V_{OH}$ | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | Vdc | 7,10,13 | 4 | - | - | 5,6,11,12 | 8 | 1,16 |
| Logic '0' output voltage | $V_{OL}$ | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | Vdc | 4 | 7,10,13 | - | - | 5,6,11,12 | 8 | 1,16 |
| Logic '1' threshold | $V_{OHA}$ | 2 | -1.065 | - | -0.980 | - | -0.910 | - | Vdc | - | 7,10,13 | - | 4 | 5,6,11,12 | 8 | 1,16 |
| voltage | | | | | | | | | | | | | | | | |
| Logic '0' threshold | $V_{OLA}$ | 2 | - | -1.630 | - | -1.600 | - | -1.555 | Vdc | - | 7,10,13 | 4 | - | 5,6,11,12 | 8 | 1,16 |
| voltage | | | | | | | | | | | | | | | | |
| Reference voltage | $V_{BB}$ | 9 | -1.420 | -1.280 | -1.350 | -1.230 | -1.295 | -1.150 | Vdc | - | - | - | - | 5,6,11,12 | 8 | 1,16 |
| **SWITCHING TIMES (50 ohm load)** | | | | | | | | | | **Pulse in** | | **Pulse out** | | | **-3.2V** | **+2.0V** |
| Propagation delay | $t_{4-2+}$ | 2 | - | 1.6 | - | 1.5 | - | 1.7 | ns | 4 | | 2 | | 5,6,11,12 | 8 | 1,16 |
| | $t_{4+2-}$ | 2 | - | 1.8 | - | 1.7 | - | 1.9 | ns | 4 | | 2 | | 5,6,11,12 | 8 | 1,16 |
| Rise time | $t_{2+}$ | 2 | - | 2.2 | - | 2.1 | - | 2.3 | ns | 4 | | 2 | | 5,6,11,12 | 8 | 1,16 |
| Fall time | $t_{2-}$ | 2 | - | 2.2 | - | 2.1 | - | 2.3 | ns | 4 | | 2 | | 5,6,11,12 | 8 | 1,16 |

Thermal characteristics $\theta_{JA}$ = 120° C/W
$\theta_{JC}$ = 40° C/W

# Applications Information

# Circuit board design

Devices within this data book are processed on Plessey high speed bipolar processes. The resultant edge speeds obtained will not cause current spikes and voltage ringing if care and attention to layout and line termination is observed. Wire wrap or Vero-board construction is not advised, as it is almost impossible to decouple and provide adequate grounding for the rise times these devices can achieve. This is mostly regardless of the frequency at which the application is functioning. Alternative prototyping circuitry can in most cases be constructed on the Wainwright pad system, as this provides a solid ground plane that ceramic chip capacitors can be soldered to directly. Supply decoupling and tolerancing are the major cause for devices failing to meet the data sheet requirements. Most devices in this data book require a 0V and -5.2V supply. The supply tolerance is $\pm 0.25$V.

Devices can fail if switch on supply transients occur. These can be of such short duration that the offending spike can only be seen using a high bandwidth scope (1GHz).

The decoupling of supplies should be performed close to the device pins. Low frequency decoupling should also be provided in most cases.

# Thermal design

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

where $\theta_{JA}$ is thermal resistance junction-to-ambient °C/W
$\theta_{JC}$ is thermal resistance junction-to-case °C/W
$\theta_{CH}$ is thermal resistance case-to-heatsink °C/W
$\theta_{HA}$ is thermal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$T_j = T_{amb} + P_D (\theta_{JA})$
$T_j$ = junction temperature
$T_{amb}$ = ambient temperature
$P_D$ = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

# Thermal design (contd.)

**Example 1**

An SP1650 is to be used at an ambient temperature of +50 °C. $\theta_{JA}$ for the DG16 package with a chip of approximately 1mm sq is 110 °C/W; from the datasheet, $P_D$ = 330mW and $T_j$ max = 175 °C.

$$T_j = T_{amb} + P_D \theta_{JA}$$
$$= 50 + (0.33 \times 110)$$
$$= 86.3\,°C \text{ (typ.)}$$

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

**Example 2**

An SP1650 is to be used at an ambient temperature of +150 °C. Again, $\theta_{JA}$ = 110 °C/W, $P_D$ = 330mW.

$$T_j = 150 + (0.33 \times 110)$$
$$= +186.3\,°C \text{ (typ.)}$$

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, $\theta_{JA}$ is the sum of the individual thermal resistances; of these, $\theta_{JC}$ is fixed by the design of device and package and so only the case-to-ambient thermal resistance, $\theta_{CA}$, can be reduced.

If $\theta_{CA}$, and therefore $\theta_{JA}$, is reduced by the use of a suitable heatsink, then the maximum $T_{amb}$ can be increased:

**Example 3**

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a $\theta_{JA}$ of 55 °C/W for the DG16 package. Using this heatsink with the SP1650 operated as in Example 2 would result in a junction temperature given by:

$$T_j = 150 + (0.33 \times 55)$$
$$= 168\,°C$$

Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as $\theta_{JC}$ may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the $\theta_{JC}$ is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

## MICROSTRIP TECHNIQUES

**Microstrip techniques have been used in the microwave field for many years and are now well characterised. Relatively recently, the advantages of accurate matching and minimisation of reflections associated with microstrip have been adopted for high speed digital circuitry. When the edge speed in a circuit is comparable with the propagation delay down the lines in use, microstrip is needed.**

A cross-section diagram is shown in Fig.1. Points to note are that the devices are usually mounted on the ground-plane side of the double-sided board; the presence of the ground-plane accurately defines the line impedances, provides low impedance current path for the ground supply and convenient decoupling for the other rails.

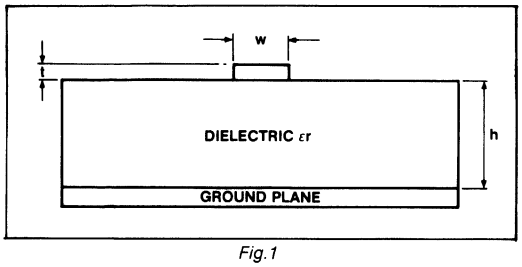



*Fig.1*

The characteristic impedance, $Z_0$, of a microstrip line is:

$$Z_0 = \frac{87}{\sqrt{\varepsilon r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$\varepsilon r$ = relative dielectric constant of the board, typically $\varepsilon r = 5$ for glass-epoxy.
$w$, $h$ and $t$ are defined on Fig.1.

Standard tables and graphs are available in the literature on microstrip to calculate the line width needed for a given $Z_0$ (Fig.2).

In practice, line impedances greater than about 150 ohms are not realisable in the copper-glass-epoxy system.

The technology of microstrip board is relatively straightforward and follows good printed circuit board practice. The use of double-sided board is strongly recommended.

The choice of board thickness and specification depends primarily on the application; best results are obtained with good quality board of reproducible characteristics. The capacitance per unit length of conductor is predictable from modified parallel-plate capacitor formulae; in practice, the graph of Fig.3 is a good guide. Variations in dielectric constant of the board change $Z_0$ in the ratio of about ±2% in $Z_0$ for ±% in $\varepsilon r$.

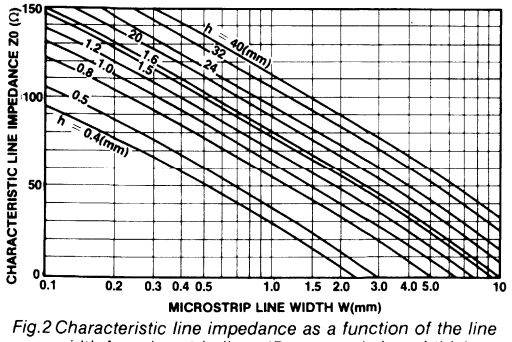



*Fig.2 Characteristic line impedance as a function of the line width for microstrip lines (Parameter is board thickness h(mm εr = 5, t = 35μ)*

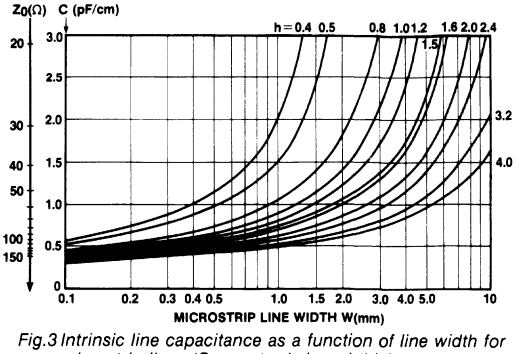



*Fig.3 Intrinsic line capacitance as a function of line width for microstrip lines (Parameter is board thickness εr = 5, t = 35μ)*

The inductance per unit length of the line may be calculated from the formula:

$$L_0 = Z_0^2 C_0$$

where $Z_0$ = characteristic impedance
$C_0$ = capacitance per unit length

The propagation delay of the line is approximately:

$$t_{pd} = 3.3 \times 10^{-2} \times \sqrt{0.475\varepsilon r + 0.67} ns/cm$$

Most glass-epoxy board has $\varepsilon r \simeq 5$, so $t_{pd} = 0.058$ns/cm. The relationship between $t_{pd}$ and $\varepsilon r$ is illustrated in Fig.4.

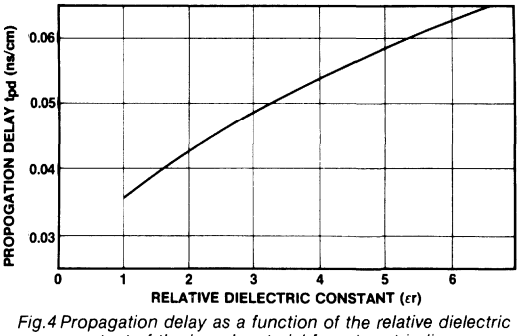



*Fig.4 Propagation delay as a function of the relative dielectric constant of the board material for microstrip lines*

### Line loading

Most devices connected to the microstrip load the lines capacitively. In some cases, such as logic inputs, there is only a single load capacitance on a relatively long line, and the effect can be ignored. On parallel outputs, especially where settling times are important, the effect of loading on the line must be compensated for. Basically, this means that the total load capacitance per unit length of line must be calculated and then the line designed in such a way that the loaded impedance matches the actual working impedance desired. Load capacitance per device is taken from the manufacturer's data or by measurement from the devices.

A fairly accurate assessment of the inter-device spacing is needed, and the types of device must be considered.

Eventually, some figure of $C_D$, the load capacitance per unit line length, can be derived. The standard equation for loaded lines is:

$$Z_0 = \frac{Z_0'}{\sqrt{1 + \frac{C_D}{C_0}}}$$

where $Z_0'$ is the characteristic unloaded impedance
$Z_0$ is the loaded impedance
$C_D$ is the load capacitance in pF/cm
$C_0$ is the line capacitance in pF/cm This is

illustrated in Fig.5.

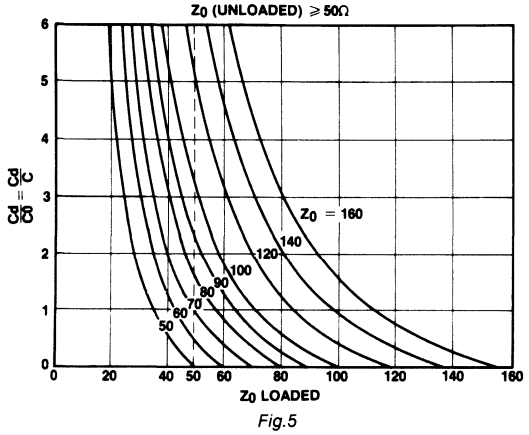



*Fig.5*

Loading in most systems is distributed, in the way described, along the lines but, in reality, does represent discrete 'lumps' of capacitance at finite points, and so any compensation scheme cannot be perfect, but practical systems if well-designed show minimal line impedance disturbance. Of course, the propagation delay is increased by capacitive loading, in the ratio:

$$t_{pd} = t'_{pd} \sqrt{1 + \frac{C_D}{C_0}}$$

where $t_{pd}$ = final delay
$t'_{pd}$ = delay of unloaded transmission line

This function is illustrated in Fig.6.

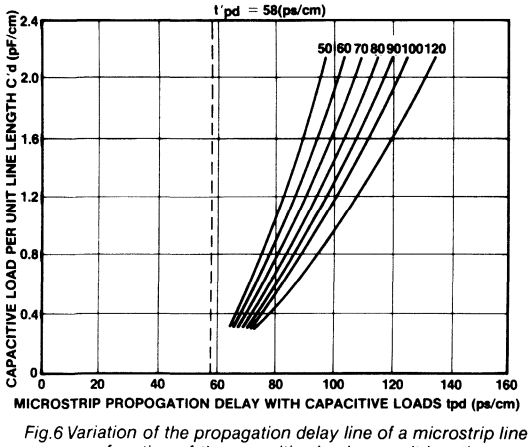



*Fig.6 Variation of the propagation delay line of a microstrip line as a function of the capacitive load per unit length. $\varepsilon r$ = 5, Parameter is $Z_0$*

## ECL IN ANALOG TO DIGITAL CONVERTER SYSTEMS

Plessey A-D products are ECL compatible in terms of input and output logic levels. If full use is to be made of the advantages of ECL, proper transmission line design rules must be observed. Fig.7 shows a simple line with driver and load. Initially, we assume that the line delay is appreciably longer than the rise and fall times, so that reflections occur at full amplitude. The output voltage swing at point A is a function of the internal device voltage swing, the output impedance, and the line impedance.

$$V_A = V_{INT} \times \frac{Z_0}{R_0 + Z_0}$$

Normally, $R_0$ is small, so $V_A \simeq V_{INT}$.

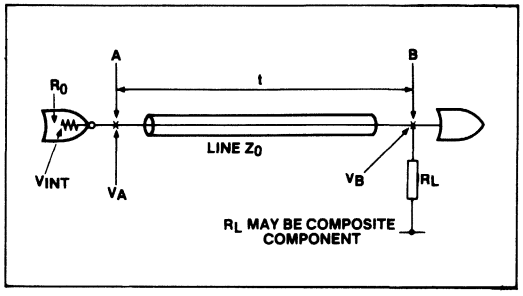



*Fig.7 Transmission line in ECL*

This signal arrives at point B after time $t$. The voltage reflection coefficient at the distant end of the line is $\rho L$, which is given by the formula:

$$\rho L = \frac{R_L - Z_0}{R_L + Z_0}$$

If $R_L = Z_0$ there is no reflection; even if $R_L$ is an approximation to $Z_0$, the reflection will not be large, as a 1% change in $R_L$ changes $\rho L$ by only 0.5%. When a reflection occurs, however, it will return to A, arriving at a time $2t$, and be reflected with a reflection coefficient:

$$\rho s = \frac{R_0 - Z_0}{R_0 + Z_0}$$

In the worst case conditions, the signal will suffer many reflections of significant amplitude: clearly this is not permissible, as it represents 'ringing' on the line. In ECL practice, ringing should be maintained below 15% undershoot and 35% overshoot. Without terminations, these figures can only be maintained for short runs. Table 1 illustrates the maximum lengths allowed, assuming 20%-80% rise/fall time of 3ns.

| Line impedance | Fanout | | | |
|---|---|---|---|---|
| | 1 | 2 | 4 | 8 |
| 50 | 21.1 | 19.1 | 17.0 | 14.5 |
| 68 | 17.8 | 15.7 | 12.7 | 10.2 |
| 75 | 17.5 | 15.0 | 11.7 | 9.1 |
| 82 | 16.8 | 14.5 | 10.7 | 8.4 |
| 90 | 16.5 | 13.7 | 9.9 | 7.6 |
| 100 | 16.0 | 13.0 | 9.1 | 6.6 |

*Table 1*

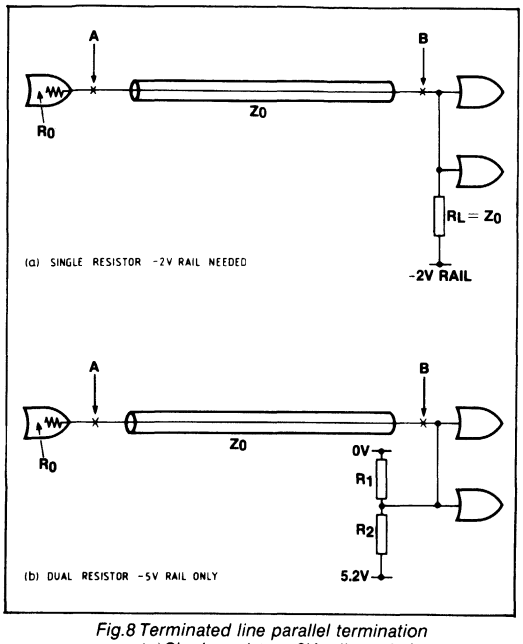



*Fig.8 Terminated line parallel termination*
*(a) Single resistor -2V rail needed*
*(b) Dual resistor -5V rail only*

The simplest termination scheme is shown in Fig.8a. Since the input impedance of ECL parts is relatively high, $R_L$ is made equal to $Z_0$. Then $\rho L = 0$ and the voltage on the line is the full ECL swing. In large systems, this technique is used extensively but has the disadvantage of requiring a -2V rail in addition to the normal supply. Fig.8b shows a convenient realisation of the same circuit using 0 and -5.2V rails only. With parallel terminated lines, the load provides the pulldown for the driving device. This termination is the fastest form for ECL. The full amplitude signal is propagated down the line, undistorted and, as $\rho L \simeq 0$, overshoot and ringing are practically eliminated. The Thevenin form is fully equivalent to the system of Fig.8a but operates on more convenient power rails. Clearly, the parallel combination of $R_1$ and $R_2$ must be equal to $Z_0$, while the defined voltage at the input must be the -2V used in Fig.8a (when the driver output is 'low'). These conditions lead to:

$$\text{for} \quad Z_0 = 50\Omega$$
$$R_1 = 81\Omega$$
$$\text{and} \quad R_2 = 130\Omega$$

General results are given in Fig.9.

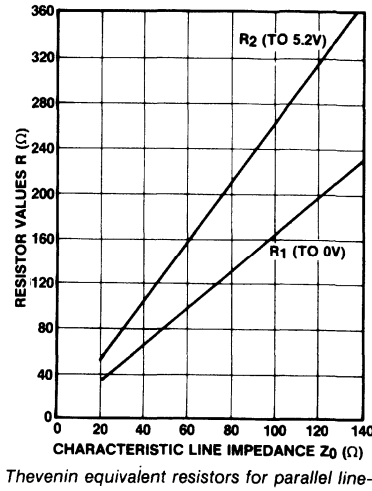



*Fig.9 Thevenin equivalent resistors for parallel line-termination*

When driving a large fanout, loads may be distributed along the full length of a parallel terminated line, although only a single line is permissible at 50Ω.

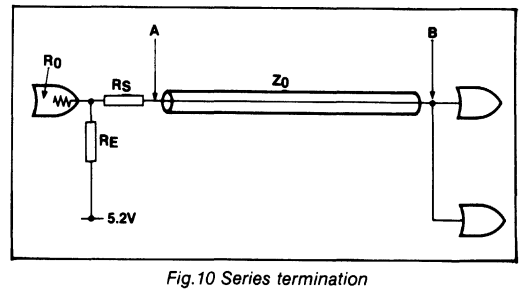



*Fig.10 Series termination*

This represents a 100% reflection at the load end of the line. As the propagated signal is of only half amplitude, the 180° phase change at the load interface is essential to provide the full logic swing at this point.

Typically, $R_0$ for ECL 10k devices is 7Ω, so in 50Ω systems, $R_S = 43\Omega$. $R_E$ is fanout dependent, and is given by:

$$R_{EMAX} = \frac{10Z_0 - R_S}{n} \quad \text{where } n = \text{fanout.}$$

The advantage of series termination is in simplicity, both in configuration and power supplies. Disadvantages are that distributed loading is not permissible, although lumped loading at the line end is satisfactory.

Voltage drops across $R_S$ limit loading to less than 10. However, multiple $Z_0$ lines, with separate $R_S$ resistors may be used. Overall slower propagation delay in series terminated mode may be a disadvantage, partly overcome by multiple transmission lines. This leads to the final line termination form, Fig.11.

It can be seen that the driver is doubly terminated, and resembles both series and parallel systems. At the distant (B) end of the line,

$R_B = Z_0$

so there is no reflection.

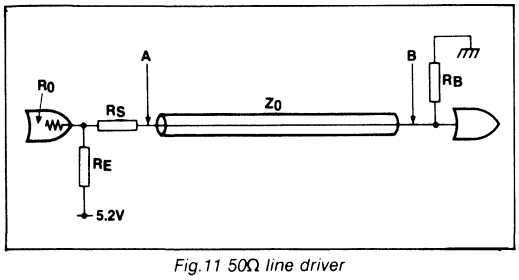



*Fig.11 50Ω line driver*

At the driving end, $R_S$ acts as a series damping resistor, and, although it is not generally possible to accurately match $Z_0$ at this point, any residual reflections on the line are further attenuated. The chief advantage of this scheme is the ability to drive a 50 ohm line terminated directly to ground, while using the conventional 0V and -5.2V supplies. Another advantage is the ability to drive long lines with low reflections; the disadvantage is that the effect of $R_S$ and $R_B$ is to reduce the signal amplitude on the line; the device at B should be some form of line receiver or comparator.

At the driving device output, the 'low' level must be pulled down to -2V. Therefore:

$$\frac{R_S + R_B}{R_S + R_E + R_B} = \frac{2}{5.2}$$

and $R_B = Z_0$ (usually 50Ω for output line driving)
and $R_E$ may be set within limits, arbitrarily, to provide an adequate 'pull-down' current.

Convenient practical values are:

$R_B =$ 50Ω
$R_S =$ 27Ω
$R_E =$ 130Ω
Nearest preferred values.

Further information can be obtained from ECL data and applications handbooks.

## A TYPICAL SYSTEM

Modern equipment practice is heavily weighted in favour of 50Ω systems, and in key items such as coaxial cable and connectors it may not be easy to procure a wide range of alternatives. In this environment, where board-to-board, or board-to-external facility connections are used, coaxial 50Ω design is strongly advised. On an individual board, interconnection at 50Ω is commonly used for analog lines, although digital signals may be conveniently operated at higher impedances. For the ultimate in performance, however, 50Ω (loaded) systems are preferred.

System design demands a range of component blocks with, desirably a high state of integration. However, two circuit blocks currently not economically available in integrated form are the buffer amplifier and the sample-and-hold. Typical applications of the buffer amplifier are high speed driving of 50Ω analog lines, DAC output buffering, and sample-and-hold buffering.

Discrete buffer amplifiers can be constructed, the main parameters being slew rate and phase distortion. The ability to drive 50Ω lines is essential.

A sample-and-hold is needed in those video systems where the aperture time must be short compared with the time taken for the A-D to perform the conversion. Typical examples are systems where series-parallel type converters are used; an input analog sample-and-hold is essential, as the LSBs are encoded some time after the MSBs. Fully parallel analog-to-digital converters can operate without sample-and-hold; this is sometimes known as 'sampling-on-the-fly'. In this case, the parallel converter, by virtue of its latch action, performs an effective sample-and-hold function on the digital output word.

One measure of a sample-and-hold 'quality' is the aperture time, which is the uncertainty in the time at which the sample is taken. The best analog sample-and-holds have $t_{aperture}$ = 20ps rms. Digital sample-and-holds are more difficult to measure, but should be approaching this figure. The aperture time requirement of a sample-and-hold is calculated from the maximum input slew rate and the accuracy required. If the maximum input frequency is $f$, and the number of bits is $n$, then:

$$t_{aperture} < \frac{1}{2^{(n+1)}\pi f}$$

In an 8-bit system, if the input bandwidth is 10MHz, and therefore the sample rate >20MHz, the required aperture time is calculated to be 62ps or better.

Current analog high speed sample-and-hold circuit design is discrete, using a ring of Schottky diodes for fast switching, usually transformer driven. The basic circuit is shown in Fig.12. A long tailed pair of very fast transistors is driven by a narrow ECL-derived pulse.

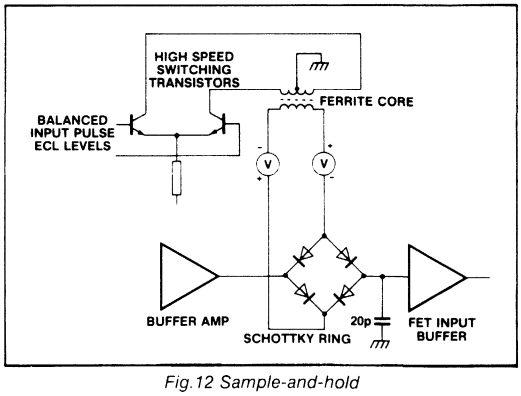



*Fig.12 Sample-and-hold*

Normally, the diode ring is biased 'off' but, during the pulse, a relatively large forward current, of the order of 20-30mA, is driven through the ring. The 'hold' capacitor charges to the voltage present at the output of the driver stage. After the pulse, the only discharge paths for the capacitor are the internal leakage, the diode ring reverse leakage, and the input current of the buffer amplifier. Low discharge rates imply low 'droop' of the signal output from the buffer amplifier; an FET input for the buffer is usually necessry. An advantage of this type of circuit is the full balance, which tends to cancel out feedthrough of the sampling pulse. The limiting factors are the time taken for the input pulse to switch the diodes, the parasitic capacitances

of the diodes, and the finite input current and bandwidth of the buffer amplifier.

Digital sample-and-hold facilities are sometimes provided in all-parallel converters, by supplying a latch signal to all comparator stages in precise synchronism with the input analog voltage. This means that the propagation delays of the lines must be accurately designed. When properly designed, digital sample-and-hold will compare favourably in aperture time with the best analog circuits, and have the additional advantage of an indefinitely long 'hold' time, making them ideal for fast sample, long hold applications.

### Testing the assembled system

The usual test instrument for high speed A-D systems is the oscilloscope, either real-time or sampling. Certainly, the oscilloscope display will illustrate whether the device is operating, and give some idea of the accuracy, limited to about six bits or so in dynamic range by the on-screen resolution. A fast D to A converter can help in A-D projects by reconverting the digital output so the difference between signals can be examined, either in the analog mode by D-A converting the A-D output, or digitally, by D-A converting a digital input and reconverting in the A-D. In either case, the permissible error function is relatively easily described and is amenable to calculation.

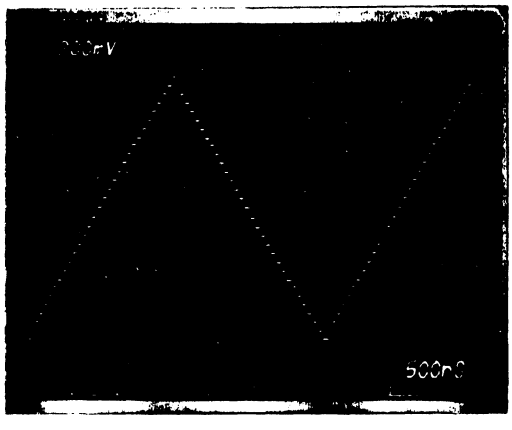


*Fig.13 Response of ADC to 300kHz ramp (clock frequency 100MHz)*

## SETTLING TIME MEASUREMENTS

The high speed of the SP9768, SP97618 and SP98608, 8-bit DAC present problems in dynamic testing, particularly in the characterisation of the precise settling time, the area in which these devices excel.

Oscilloscopes, real time or sampling, do not have sufficient resolution for measurements to better than $\pm\frac{1}{2}$ LSB (1 part in 256). Further, the input VSWR, even of the most modern oscilloscopes, is too high for accurate measurement at high speed. Input VSWR is not usually specified but typical figures are 1.25 or worse; this represents a reflection into the circuit of 11% or 27 LSBs. Reflection 'humps' of this kind can be seen on oscilloscope photographs of the DAC output.

The solution is to run the DAC output, under the 'all bits switched' condition, direct into the input of a high speed comparator set to look for a particular voltage threshold. A defined resistor is used with a minimum of parasitic capacitance.

The comparator output is then viewed on the oscilloscope with a time measurement from the DAC input to the comparator output yielding a figure for the DAC plus comparator delay - a 50% points test which is relatively insensitive to measurement conditions and relatively easily automated. The comparator delay, separately characterised, is subtracted to find the DAC settling time. A convenient arrangement is to use a dual comparator, one to measure delay time from switching to the DAC output coming into a defined settling band, the second to check that the device makes no overshoot out at the other side. See Fig.14.

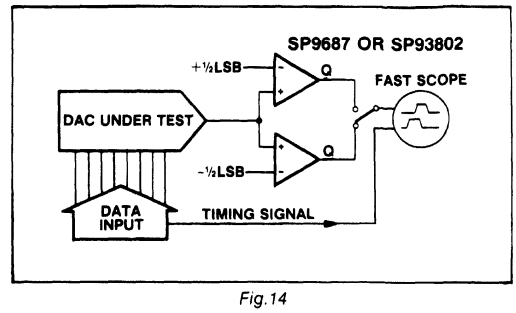
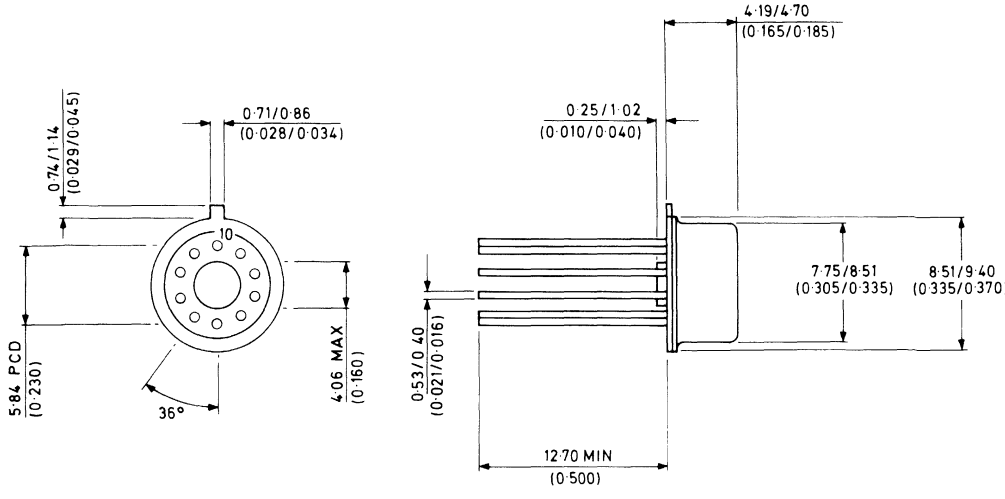


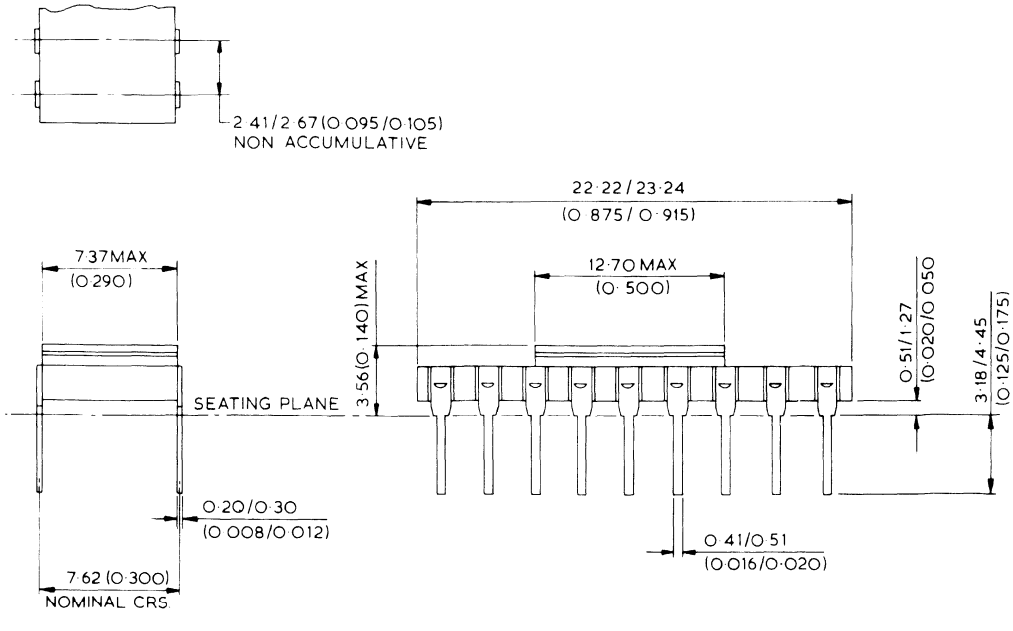

*Fig.14*

# Package Outlines

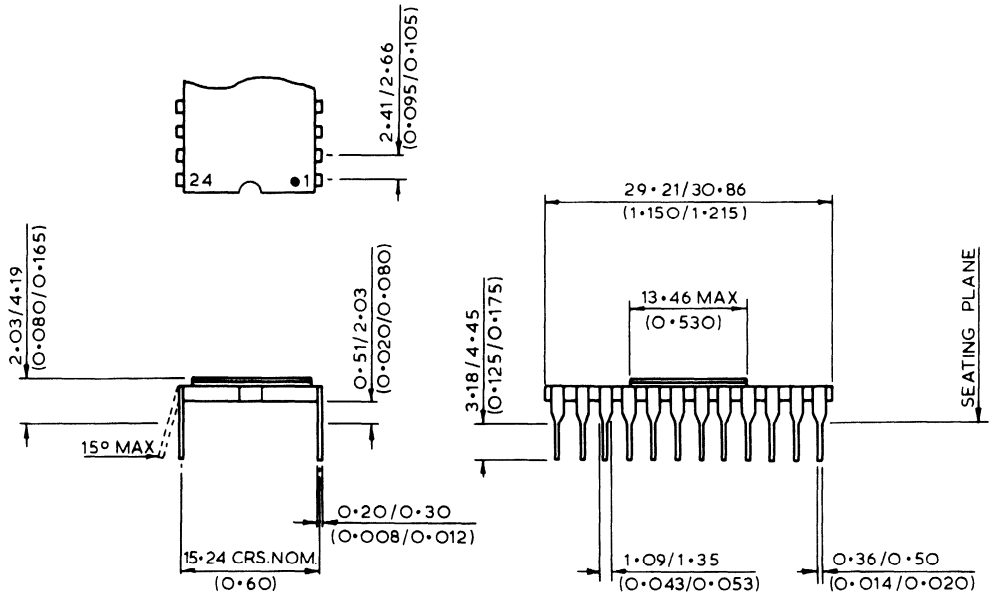
## Ordering Information




**10-LEAD METAL/CERAMIC (5.84mm PCD)
WITH STANDOFF - CM10/S**




**18-LEAD SIDEBRAZED CERAMIC DIL - DC18**

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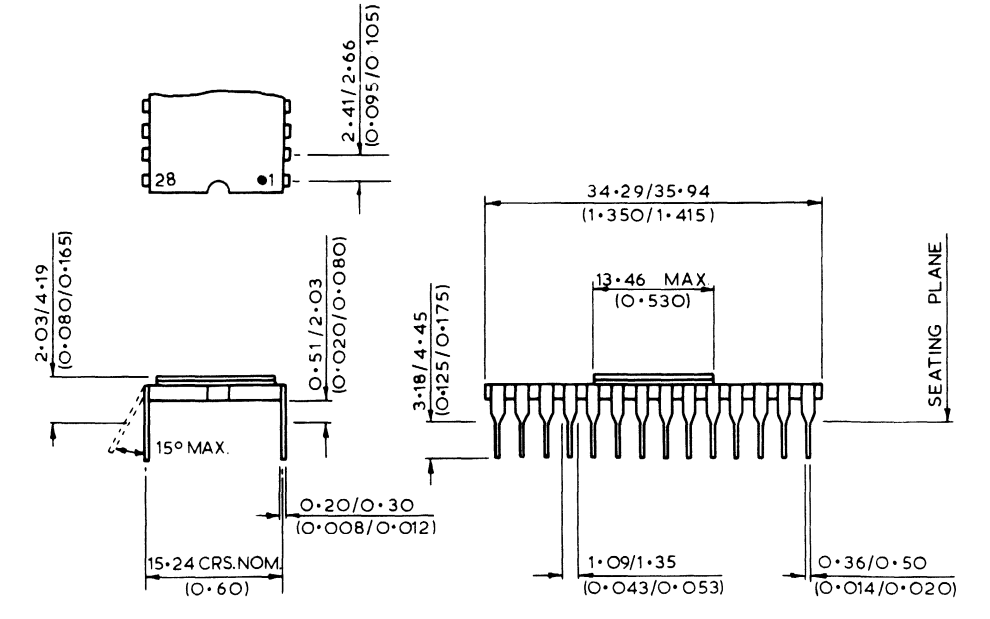


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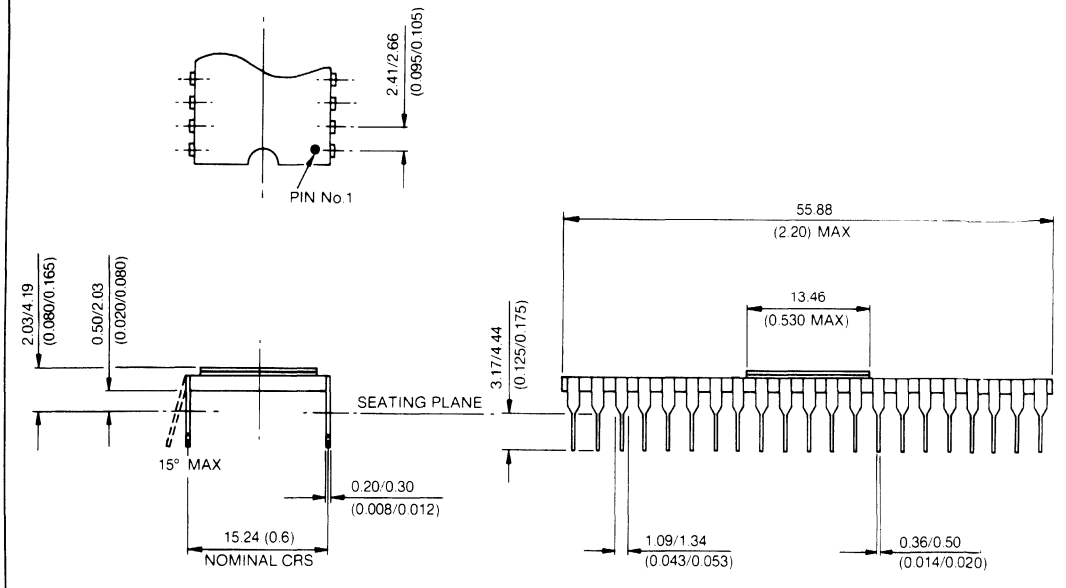
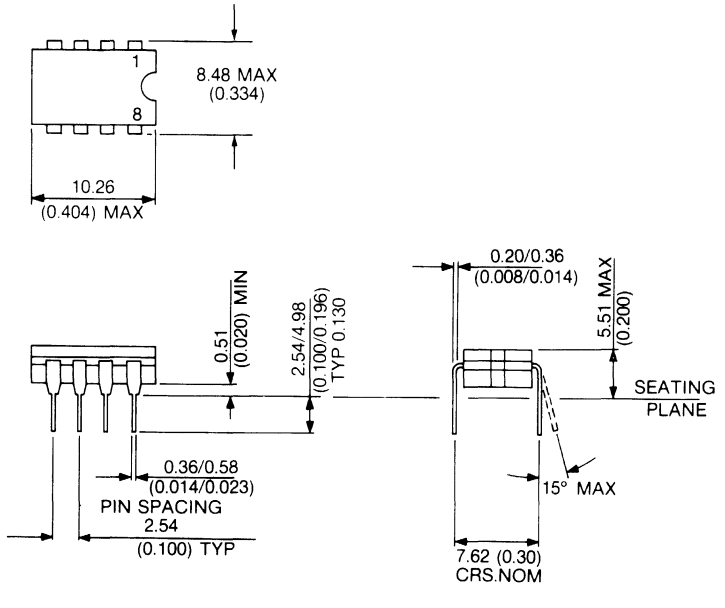
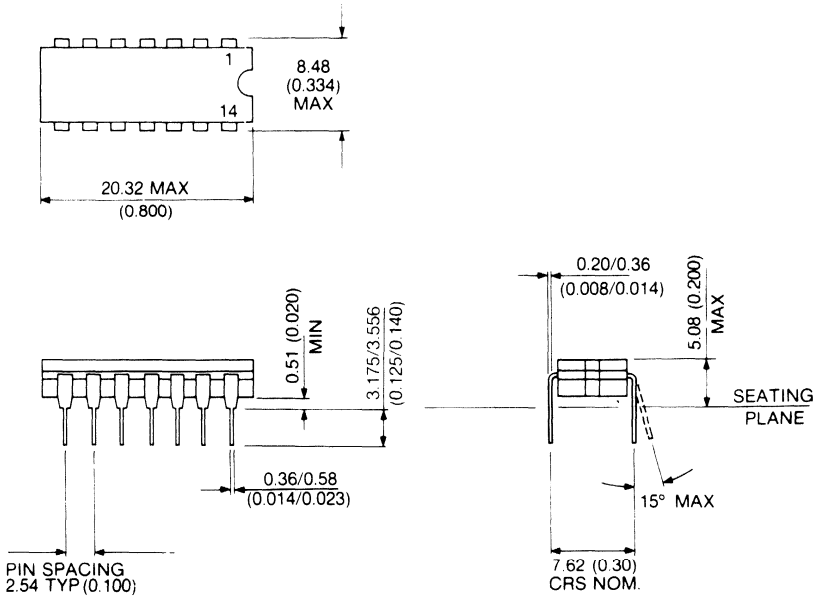



**42 LEAD DILMON - DC42**




**8 LEAD CERAMIC DIL CERDIP - DG8**

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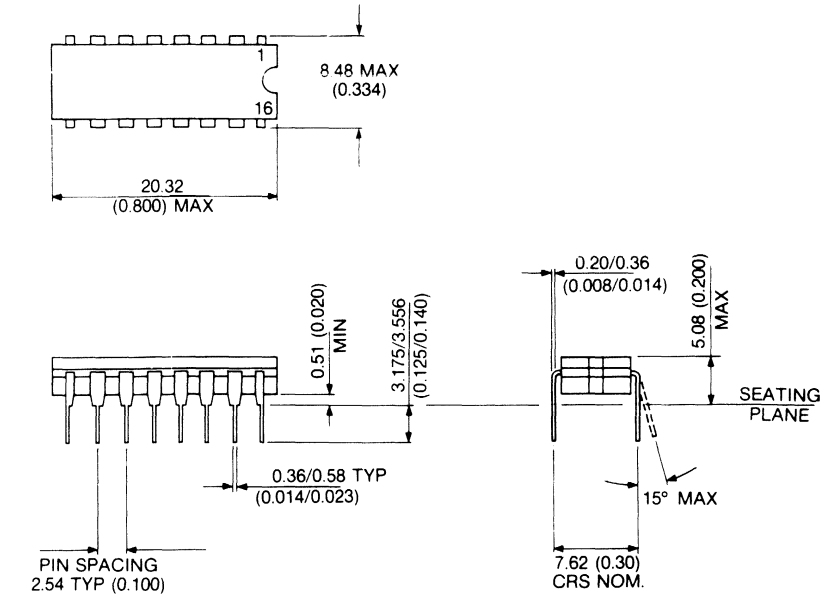


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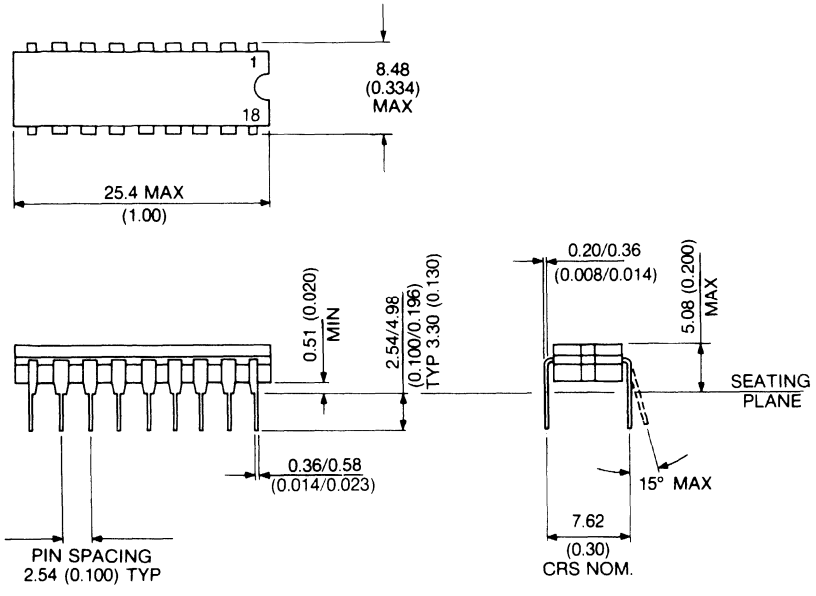


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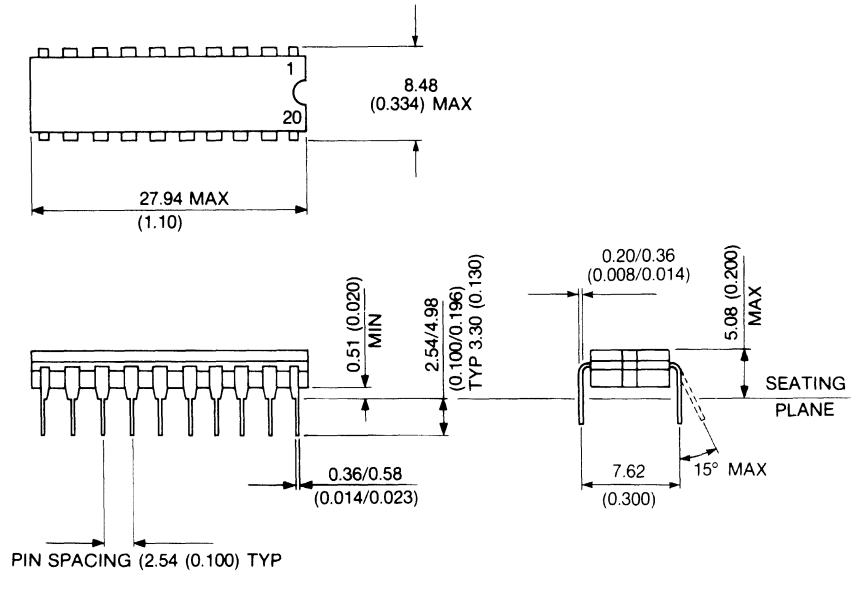


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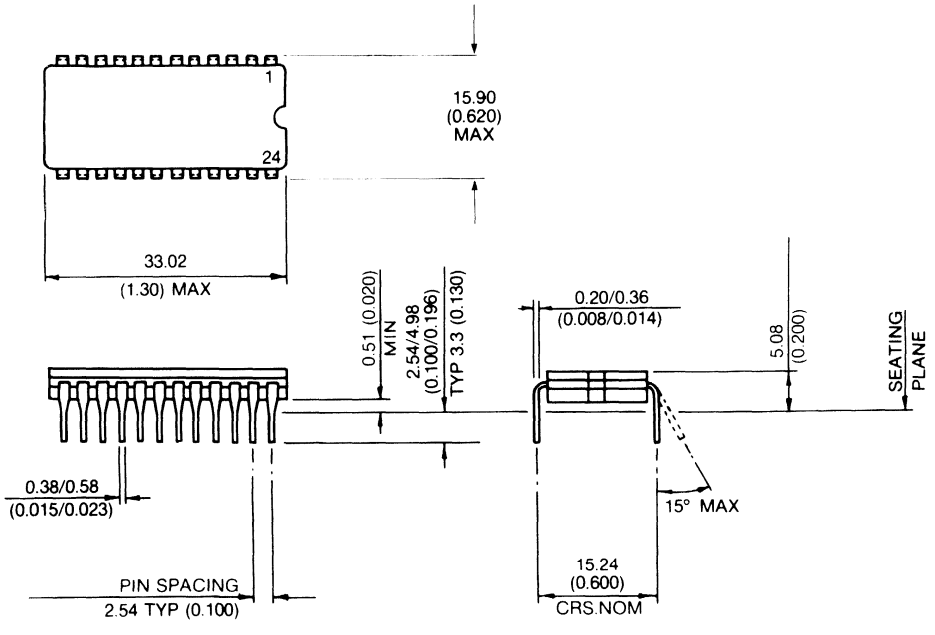


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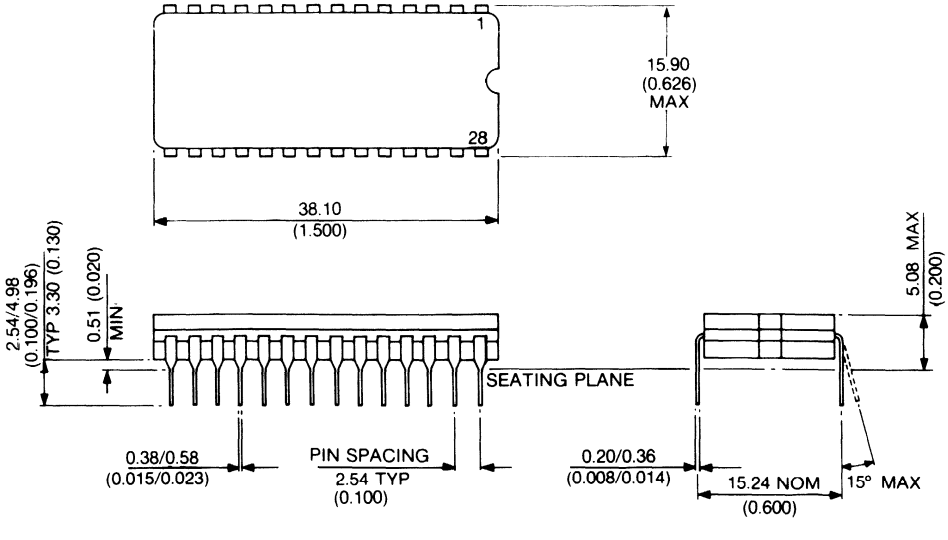


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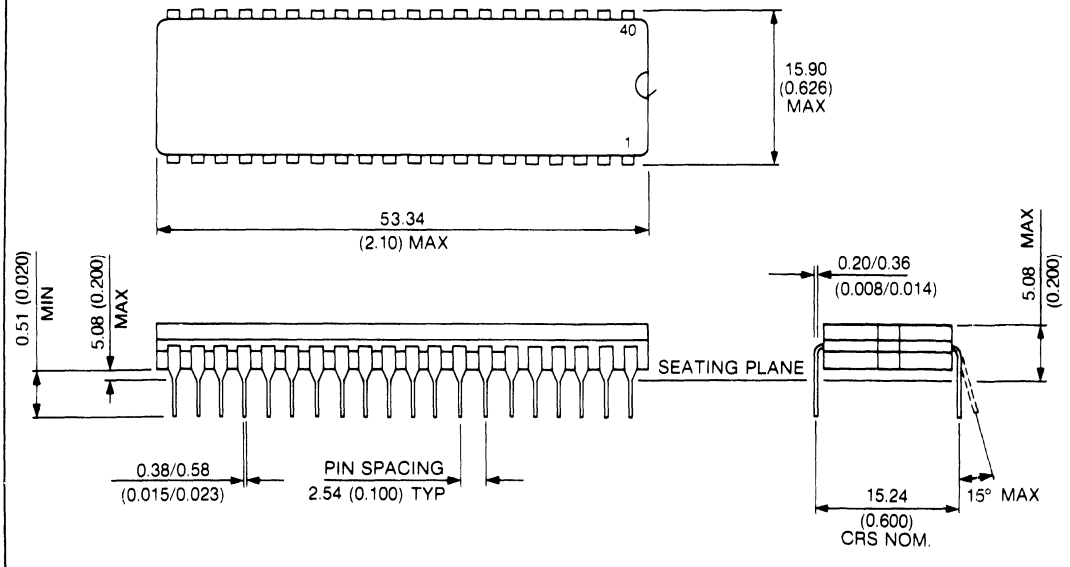


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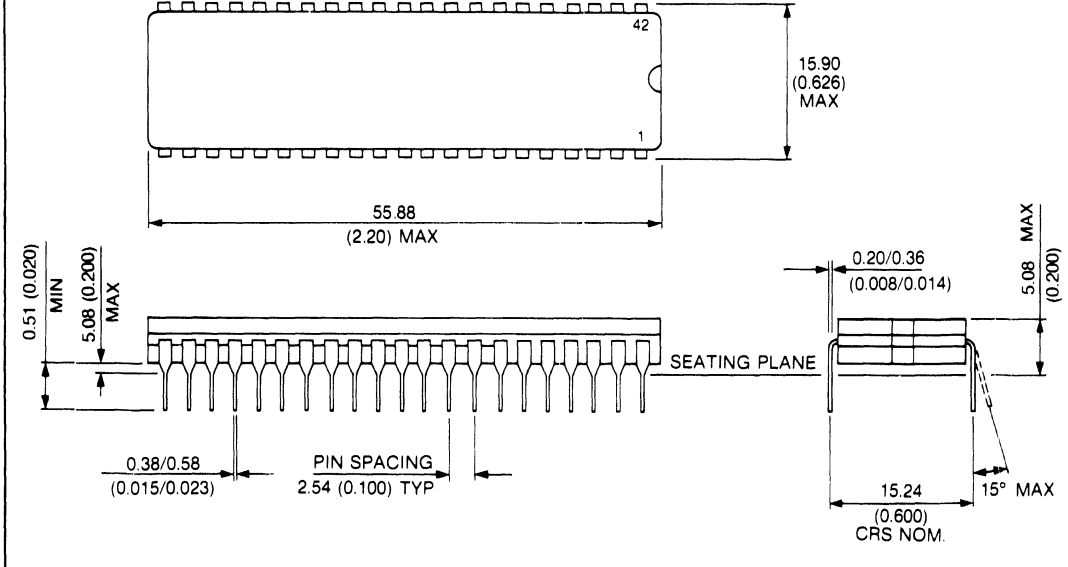


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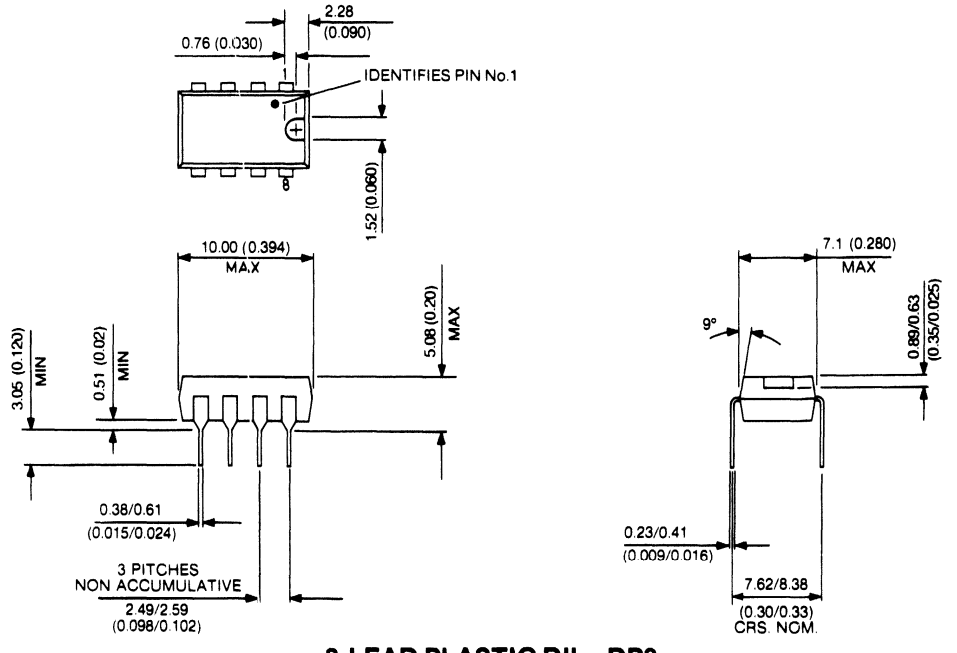
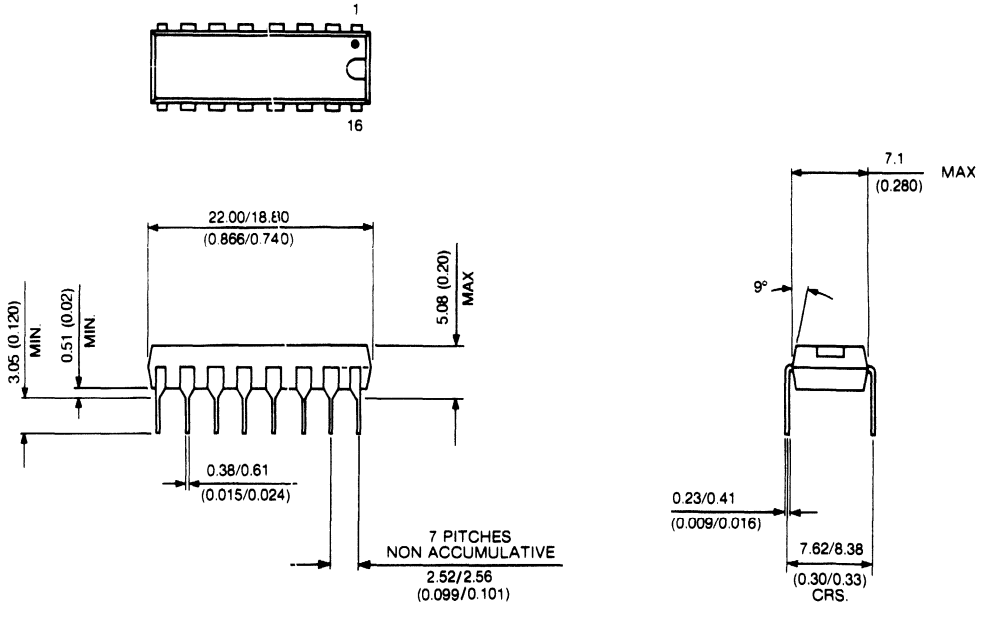



**8-LEAD PLASTIC DIL - DP8**

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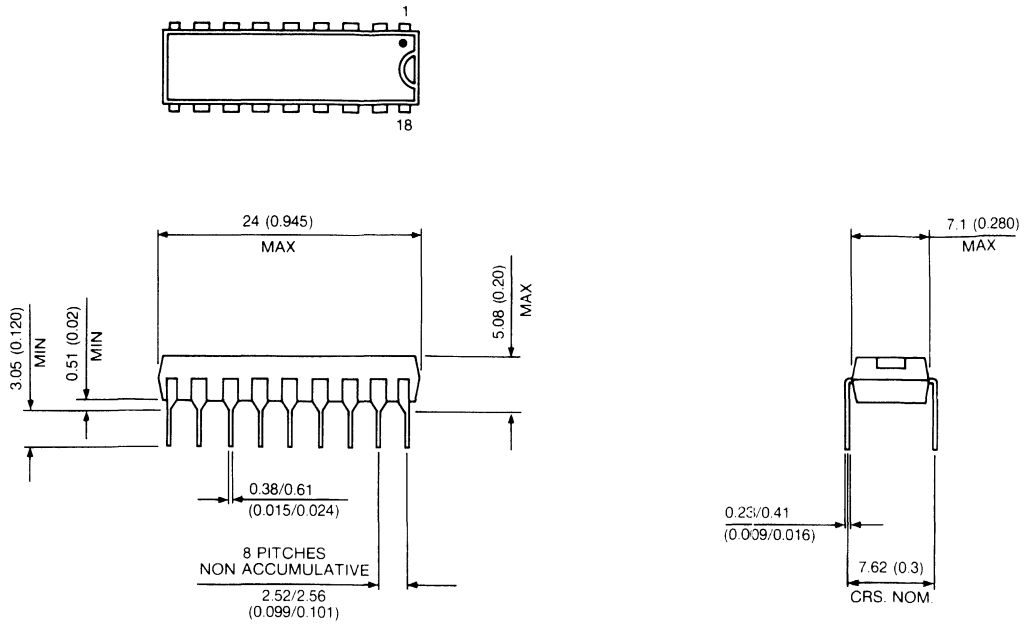


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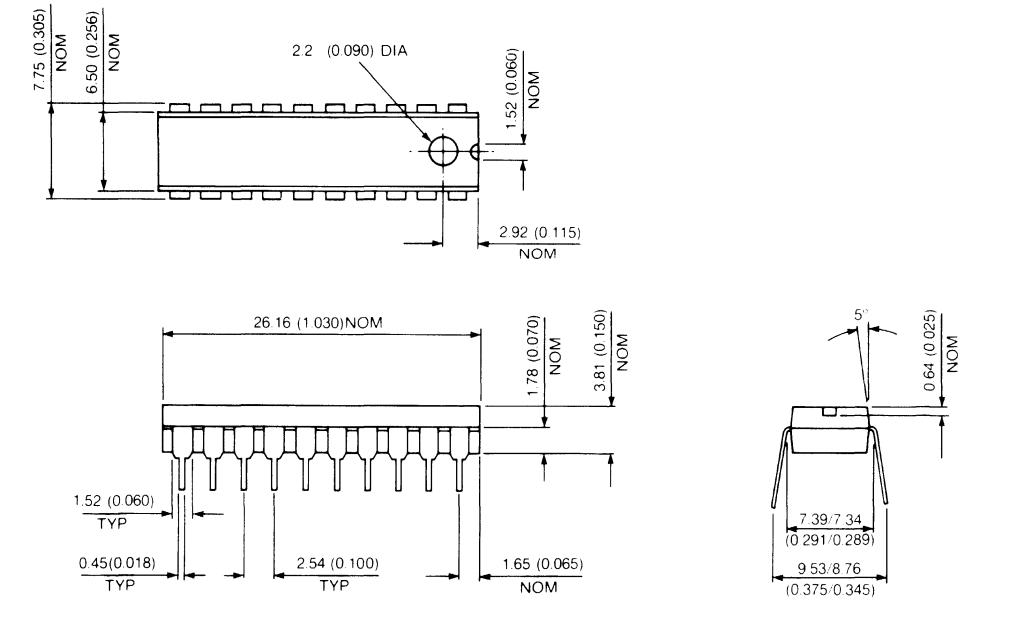


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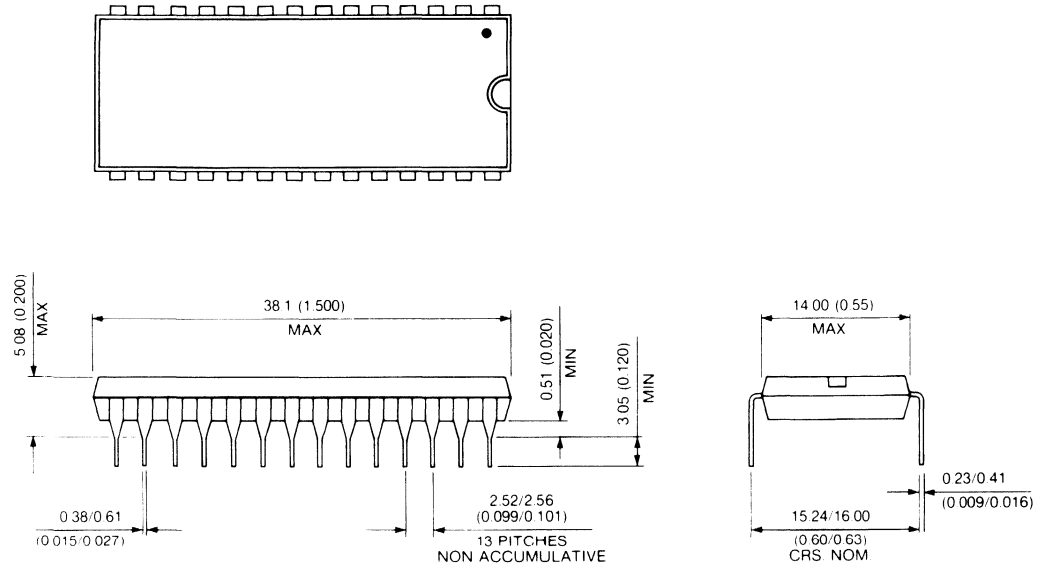
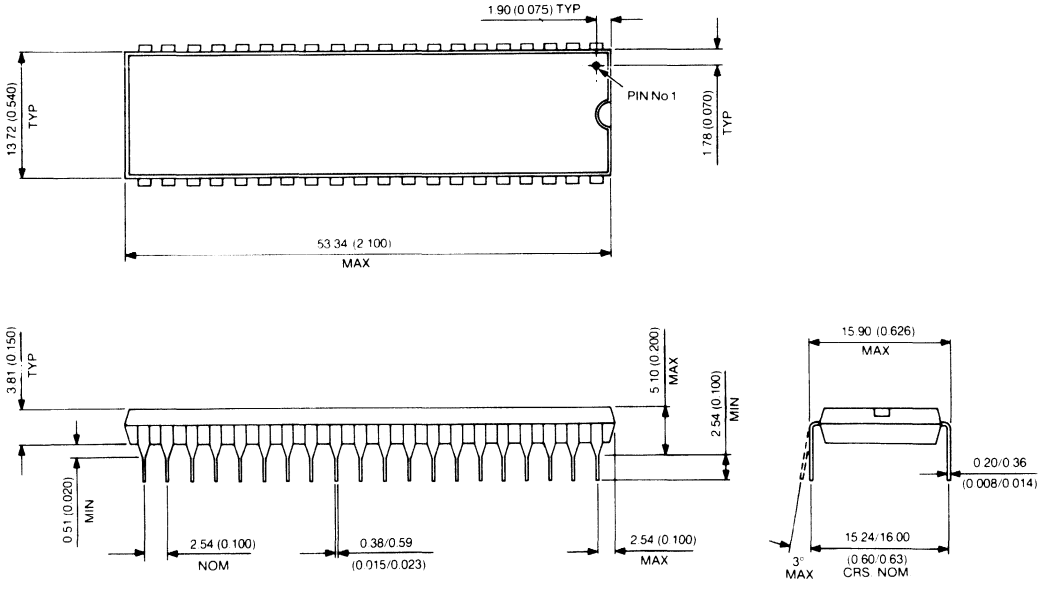



## 28-LEAD PLASTIC DIL - DP28

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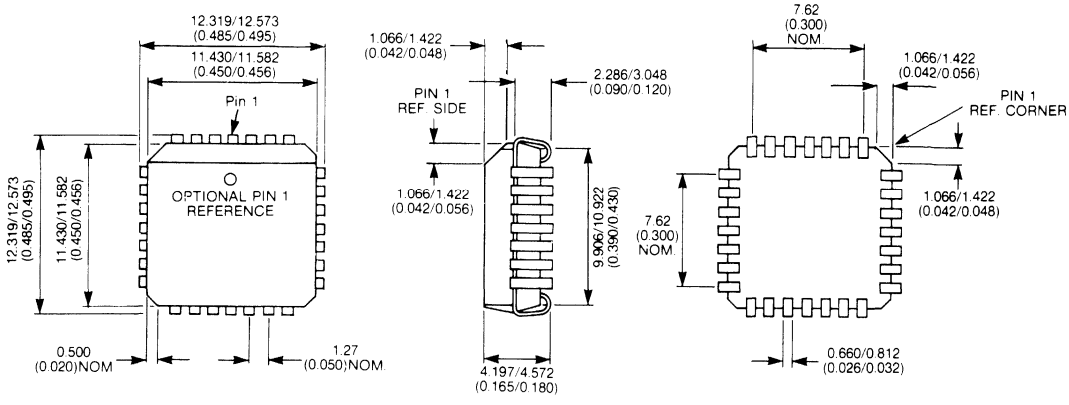
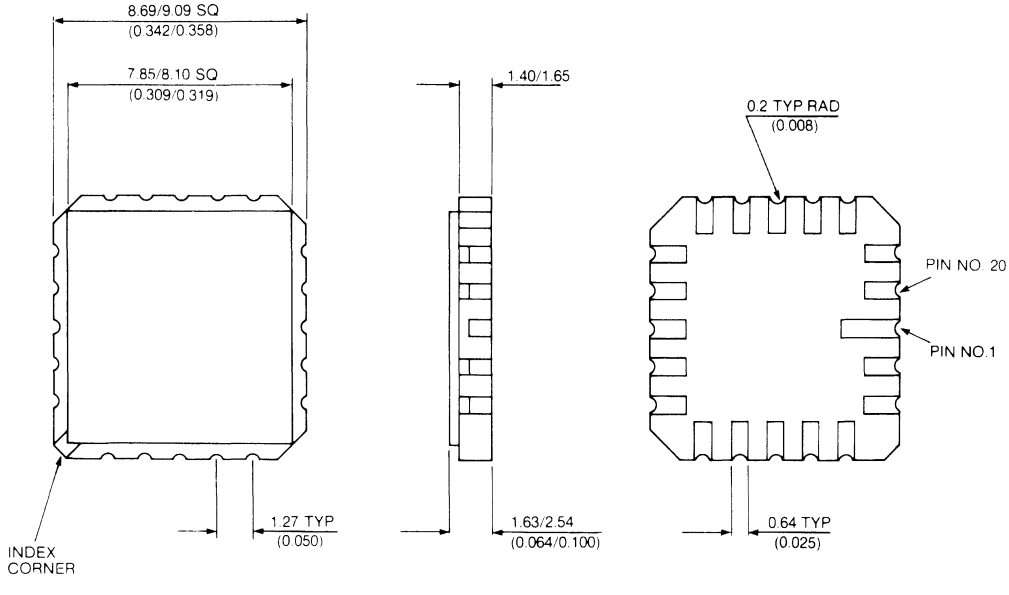
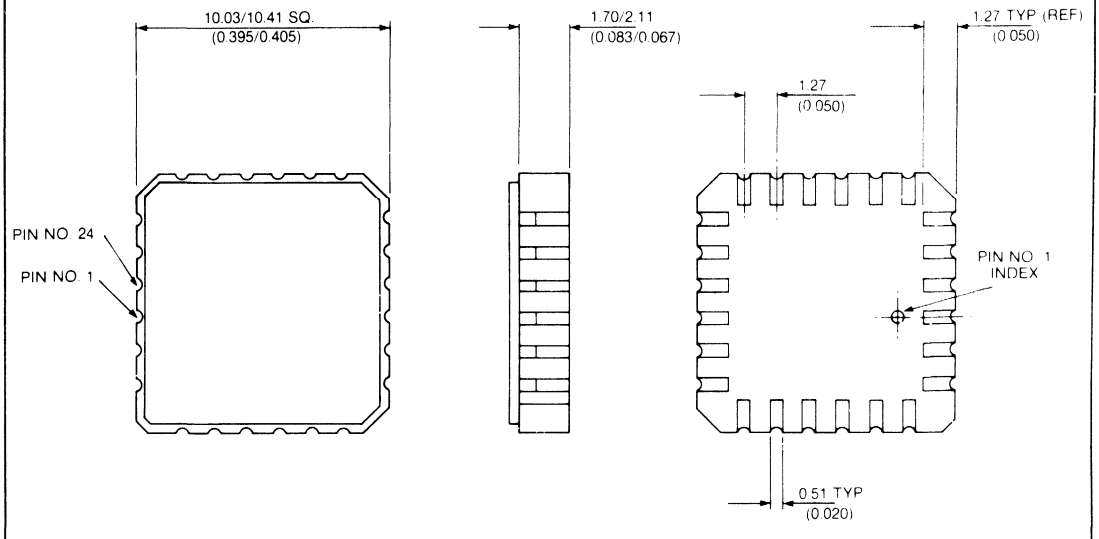


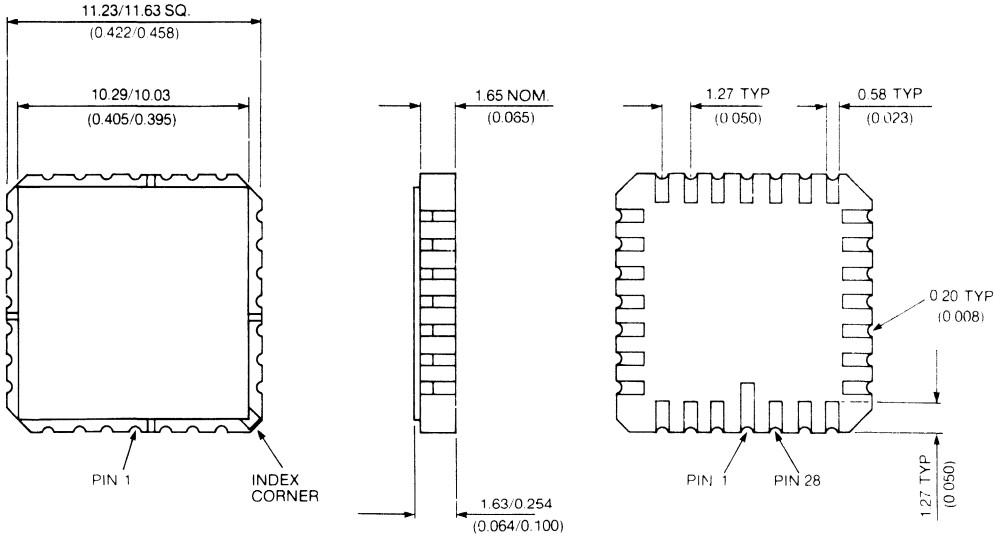

**28-LEAD QUAD PLASTIC J LEAD - HP28**



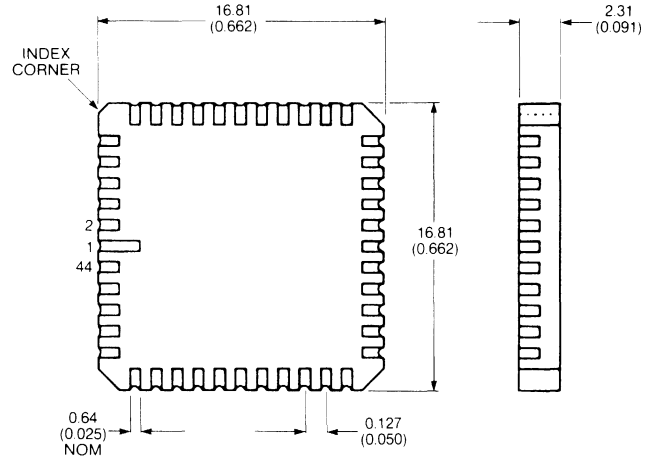

**20-PIN LEADLESS CHIP CARRIER - LC20**
**(HERMETIC)**



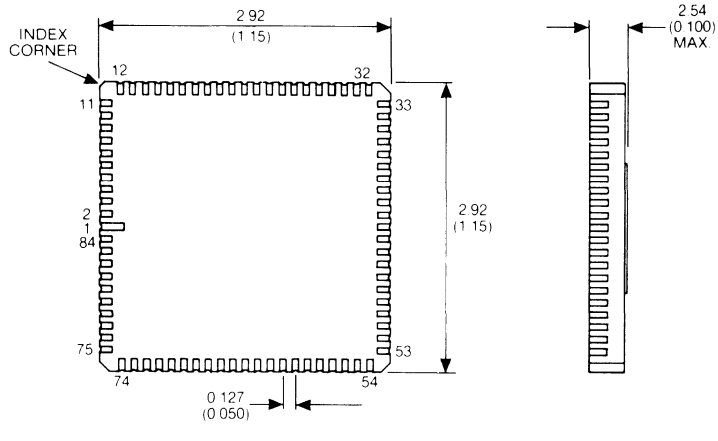

**24-PIN LEADLESS CHIP CARRIER - LC24**
**(HERMETIC)**



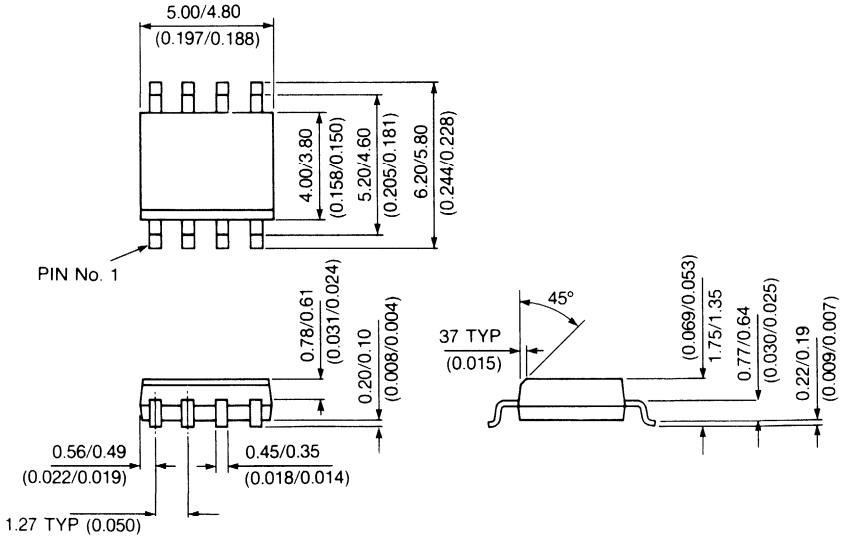

**28-PIN LEADLESS CHIP CARRIER - LC28**
**(HERMETIC)**



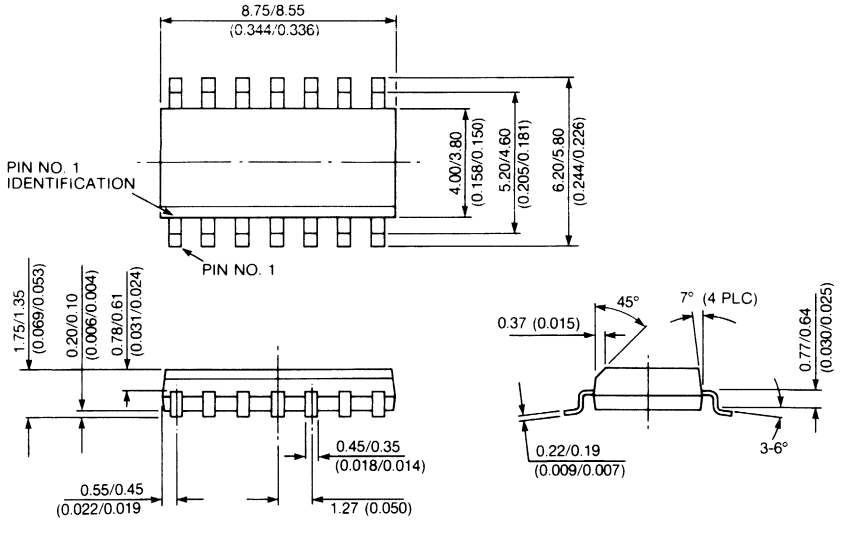

**44-PIN LEADLESS CHIP CARRIER - LC44**
**(HERMETIC)**



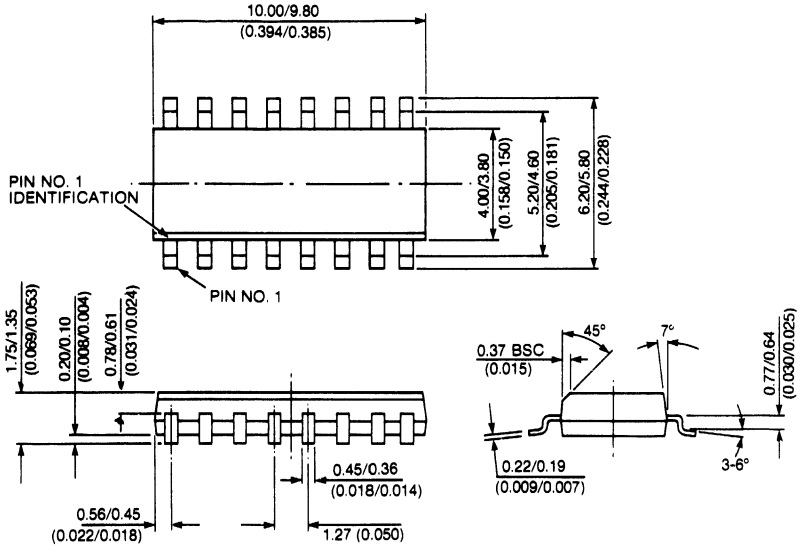

**84-PIN LEADLESS CHIP CARRIER - LC84**
**(HERMETIC)**



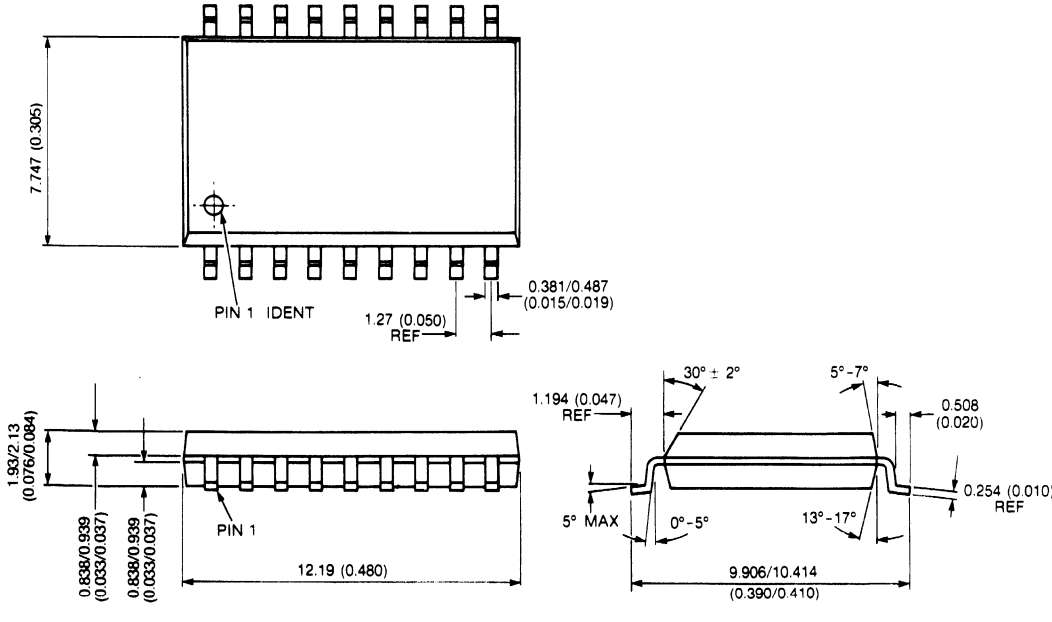

**8-LEAD MINIATURE PLASTIC DIL - MP8**




**14 - LEAD MINIATURE PLASTIC DIL - MP14**




**16-LEAD MINIATURE PLASTIC DIL - MP16**




**18-LEAD MINIATURE PLASTIC DIL - MP18**

# Ordering information

Plessey Semiconductor integrated circuits are allocated type numbers which take the following general form

**WW XXXXX YY ZZ**

where **WW** is a two-letter code identifying the product group and/or technology, **XXXXX** is a three, four or five numeral code uniquely specifying the particular device, **YY** is a one or two letter code denoting the precise electrical or thermal specification for certain devices and **ZZ** is a two-letter code defining the package style. Digits **WW**, **XXXXX** and **YY** must always be used when ordering; digits **ZZ** need only be used where a device is offered in more than one package style. For example, the **SP9131** is offered in **DG** (Ceramic dual-in-line) and **LC** (Leadless chip carrier) packages so the full ordering number for this device in ceramic DIL would be **SP9131/DG** and **SP9131/LC** for the leadless chip carrier version.

The Pro-Electron standard is used for package codes wherever possible. The two letters of this code have the following meanings:

FIRST LETTER (indicates general shape)

**A** Pin-Grid Array
**C** Cylindrical
**D** Dual-in-Line (DIL)
**F** Flat Pack (leads on two sides)
**G** Flat Pack (leads on four sides)
**Q** Quad-in-Line

**M** Miniature (for Small Outline)
**L** Leadless Chip Carrier — Not yet designated by Pro-Electron
**H** Leaded Chip Carrier

SECOND LETTER (indicates material)

**C** Metal-Ceramic (Metal Sealed)
**G** Glass-Ceramic (Glass Sealed)
**M** Metal
**P** Plastic
**E** Epoxy

Please Note:

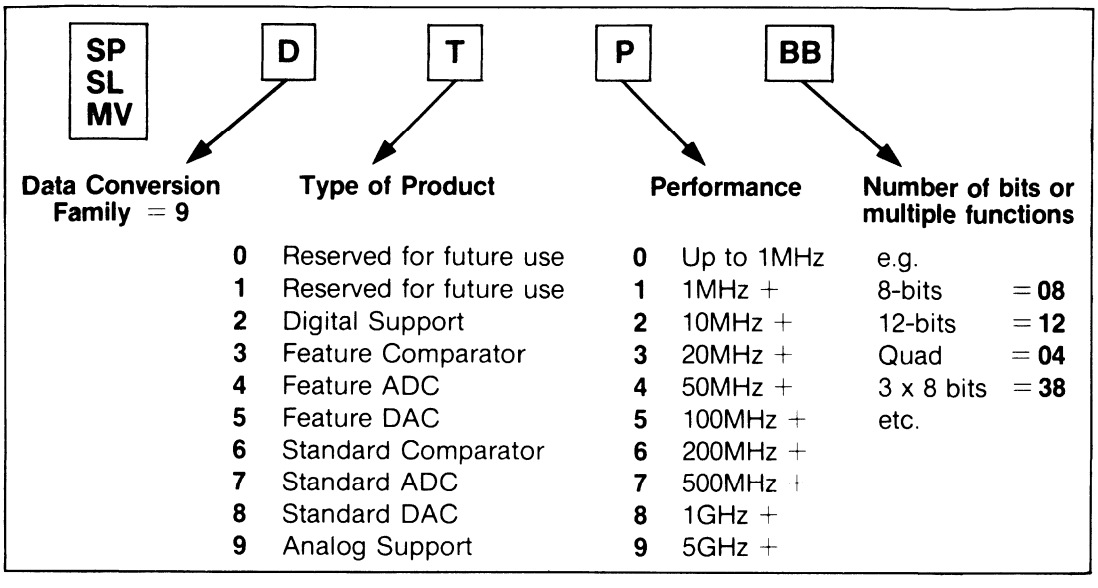
**Leadless Chip Carriers**

**LC** Metal-Ceramic 3 Layer (Metal Sealed)
**LG** Glass-Sealed Ceramic
**LE** Epoxy-Sealed 1 Layer
**LP** Plastic

*Note: The above information refers generally to Plessey Semiconductors integrated circuit products and does not necessarily apply to all the devices contained in this handbook.*

# Part Numbers for New Data Conversion Products

(Derived from the structure shown below and are applied to all 5 digit codes except SP97618).



# Plessey Semiconductors Locations

# Main offices

U.K./EUROPE **Plessey Semiconductors Ltd.**, Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom. Tel: 44 793 36251 Tx: 449637.

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ITALY **Plessey SpA**, Viale Certosa, 49, 20149 Milan. Tel: (2) 390044/5 Tx: 331347.

WEST GERMANY, AUSTRIA, SWITZERLAND **Plessey GmbH**, Altheimer Eck 10, 8000 Munchen 2, West Germany. Tel: 089 23 62-0 Tx: 522197.

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**Mammeas** Representations & Exportations, P.O.Box 181, Piraeus. Tel: 4172597 Tx: 213835 LHGR

INDIA **Semiconductors Ltd.**, Dr Shirodkar Rd., Parel, Bombay 400012. Tel: 4130661/666/667/801 Tx: 01171521 BAOL IN.
**Semiconductors Ltd.**, Unity Buildings, J.C. Road, Bangalore 560-001. Tel: 52072 & 578739
**Semiconductors Ltd.**, 513, Ashoka Estate, 24, Barakhamba Road, New Delhi — 110001. Tel: 44879 Tx: 31 3369

JAPAN **Cornes & Company Ltd.**, Maruzen Building, 2 Chome Nihonbachi, Chuo-Ku, C.P.O.Box 158, Tokyo 100-91. Tel: 010 81 3 272 5771 Tx: 24874.
**Cornes & Company Ltd.**, 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 532 1012 Tx: 525-4496.

HONG KONG **YES Products Ltd.**, Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kok Street, Tsuen Wan, N.T., Hong Kong. Tel: 0-444261-6 Tx: 36590.

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**KML Corporation**, 3rd Floor, Banpo Hall Building, 604-1 Banpo Dong, Kangnam-Ku, P.O.Box 19, Seoul. Tel: (02) 533-9281/2 Tx: KMLCORP K25981 Fax: (02) 533 1986.

NEW ZEALAND **Plessey (NZ) Ltd.**, Te Pai Place, Henderson, Auckland 8. Tel: 8364189 Tx: NZ2851.

SCANDINAVIA

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Finland **Oy Ferrado AB**, P.O.Box 54, SF-00381 Helsinki 38. Tel: 90 55 00 02 Tx: 122214.

Norway **Skandinavisk Elektronikk A/S**, Ostre Aker Vei 99, Oslo 5. Tel: 02 64 11 50 Tx: 71963.

Sweden **Swedesupply AB**, PO Box 1028, 171 21 Solna. Tel: 08/735 81 30 Tx: 13435.

SINGAPORE **Plessey S.E. Asia Pte Ltd.**, 400 Orchard Road, No. 21-07 Orchard Towers, Singapore 0923. Tel: 7325000 Tx: RS22013 Direct Fax: 7329036.

SOUTH AFRICA **Plessey South Africa Ltd.**, 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793, Tx: 4-31421 Fax: (011) 8266704 after hours.

SPAIN **JR Trading**, Apartado de Correos 8432, Madrid 8 Tel: 248 12 18/248 38 82 Tx: 42701.

TAIWAN **Artistex International Inc.**, B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan, Republic of China. Tel: 7526330 Tx: 27113 ARTISTEX Fax: (8862) 721 5446.

TURKEY **Turkelek Elektronic Co.Ltd.**, Hatay Sokak 8, Ankara. Tel: 4-118 94 83, 4-125 21 09, 4-117 83 71, 4-117 55 29 Tx: 44580
**Turkelek Elektronic Co.Ltd.**, Kemeralti Caddesi, Tophane Ishani 406, Istanbul. Tel: (1) 143 12 68, (1) 143 40 46 Tx: 25136.

MALAYSIA **Plessey Malaysia**, 1602 Pernas International Bldg, Jalan Sultan Ismail, Kuala Lumpur 50250. Tel: (03) 2611477 Tlx: 30918 PLESCOMA.

# World-wide distributors

| | |
|---|---|
| AUSTRALIA | **Plessey Semiconductors Australia Pty Ltd**. P.O.Box 2. Villawood. New South Wales 2163. Tel. Sydney (02) 720133 Tx: AA20384 Direct Fax. (02) 7260669. |
| AUSTRIA | **DAHMS Elektronik Ges. mbH**. Wiener Str. 287. A-8051 Graz. Tel. 0316/64030 Tx. 31099. |
| BELGIUM | **Master Chips**. 4 St. Lazarus Laan. 1030 Brussels. Tel. 02/219.58.62 Tx. 62500. |
| FRANCE | **Mateleco**. 66. Rue Augustin Dumont. 92240 Malakoff. Paris. Tel. (1) 46.57.70.55 Tx. 203436F. |
| | **Mateleco Rhône-Alpes**. 2 Rue Emile Zola. 38130 Echirolles. Tel. (76) 40.38.33 Tx. 980837. |
| | **ICC**. 78. Chemin Lanusse. B.P.No. 2147. 31200 Toulouse. Tel. (61) 26-14-10 Tx. 520897 F. |
| | **ICC**. Z.A. du Haut Vigneau. Rue de la Source. 33170 Gradignan. Tel. (56) 31-17-17 Tx. 541539 F. |
| | **ICC**. 2 bis Avenue de Fontmaur. 63400 Chamalieres. Tel. 73.36.71.41 Tx. 990928f. |
| | **ICC**. Z.A. Artizanord II. Lot 600 - bâtiment 19. Traverse de l'Oasis. 13015 Marseille. Tel. (91)-03-12-12 Tx. 441313 F. |
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| | **Eurelettronica**. Via Bertoloni 27. Rome. Tel. 875394 Tx. 610358. |
| | **Alta S.R.L.**. Via Matteo Di Giovanni 6. 50143 Florence. Tel. 055-717402 Tx. 571246. |
| | **Adelsi Spa,** Via Novara 570. 20153 Milan. Tel. 02/3580641 Tx. 332423 Adelsy I. |
| NETHERLANDS | **Heynen B.V**.. Postbus 10. 6590 AA Gennep. Tel. 8851-96111 Tx. 37282. |
| NEW ZEALAND | **Professional Electronics Ltd**. P.O.Box 31-145. Auckland. Tel. 493.029 Tx. 21084. Direct Fax. (09) 493045. |
| SOUTH AFRICA | **Plessey South Africa Ltd**.. 1 Jansen Road. Jet Park. Boksburg. Tel. (011) 8266793. Tx. 4-31421 SA Fax. (011) 8266704 after hours. |
| SWITZERLAND | **Aumann & Co. AG**. Forrlibuckstrasse 150. CH-8037 Zurich. Tel. 01/443300 Tx. 822966. |
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| | **Quarndon Electronics Ltd**.. Slack Lane. Derby DE3 3ED. Tel. 0332 32651 Tx. 37163. |
| | **Semiconductor Specialists (UK) Ltd**.. Carroll House. 159 High Street. Yiewsley. West Drayton. Middlesex UB7 7XB. Tel. 0895 445522 Tx. 21958. |
| | **Unitel Limited**. Unitel House. Fishers Green Road. Stevenage. Herts. SG1 2PT. Tel. 0438 312393 (Direct Sales) 0438 314393 (General) Tx. 825637. 826080 Fax. 0438 316711. |
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| WEST GERMANY | **AS Electronic Vertriebs-GmbH**. Elisabethenstrasse 35. 6380 Bad Homburg. Tel. 06172/2 90 28-29 Tx. 410868. |
| | **Astronic GmbH**. Winzererstrasse 47D. 8000 Munchen 40. Tel. 089/309031 Tx. 5216187. |
| | **Micronetics GmbH**. Weil der Stadter Str. 45. 7253 Renningen 1. Tel. 07159/6019 Tx. 724708. |
| | **Nordelektronik GmbH**. Carl-Zeiss-Str. 6. 2085 Quickborn. Tel. 04106/72072 Tx. 214299. |

# North American sales offices

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|---|---|
| NATIONAL SALES | 9 Parker, Irvine, CA 92718. Tel: (714) 472-0303 Twx: (910) 595-1930 Fax: (714) 770-0627. |
| EASTERN REGION | 1767-42 Veterans Memorial Hwy., Central Islip, NY 11722. Tel: (516) 582-8070 Tlx: 705922 Fax: 516-582-8344. |
| CHESAPEAKE REGION | 9003 F Greentree Commons, Marlton, New Jersey 08053. Tel: (609) 596 2030 Tlx: 62953899 Fax: 609-596-1635. |
| NEW ENGLAND REGION | 132 Central St., 216 Foxboro, MA 02035. Tel: (617) 543-3855 Tlx: 316805 Fax: 617-543-2994. |
| WESTERN REGION | 4633 Old Ironsides Dr. 250, Santa Clara, CA 95054. Tel: (408) 986-8911 Tlx: 62217370 Fax: 408-970-0263. |
| SOUTHEAST REGION | 9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930 Tlx: 510-600-3635 Fax: 214-680-9753. |
| NORTH CENTRAL REGION | 1919 South Highland 120C, Lombard, IL 60148. Tel: (312) 953-1484 Tlx: 705186 Fax: 312-953-0633. |
| FLORIDA & DIXIE REGION | 541 S.Orlando Ave., Suite 310, Maitland, FL 32751. Tel: (305) 539-0080 Fax: 317-844-4753. |
| SOUTHWEST REGION | 9 Parker, Irvine, CA 92718. Tel: (714) 472-2530 Tlx: 989096 Fax: 714-458-7084. |
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| ALABAMA | **Electronic Marketing Associates, Inc. (EMA),** 1200 Jordan Lane, Suite 4, Jordan Center, Huntsville, AL 35805. Tel: (205) 536-3044 Twx: 910-997-0551. |
| ARIZONA | **Chaparral Electronics,** 2024 N. 7th Street 200, Phoenix, AZ 85006. Tel: (602) 252-0897 Fax: 602-254-9912. |
| CALIFORNIA | **Cerco,** 5230 Carrol Canyon Rd. 214, San Diego, CA 92121. Tel: (619) 450-1754 Twx: 910-335-1220 Fax: 619-450-3681.<br>**Pinnacle Sales Corp.,** 275 Saratoga Ave., Suite 200, Santa Clara, CA 95050. Tel: (408) 249-7400 Fax: 408-249-5129.<br>**Select Electronics,** 14730 Beach Blvd-Bldg F, Suite 106, La Mirada, CA 90638. Tel: (714) 739-8891 Twx: 910-596-2818 Fax: 714-739-1604.<br>**Select Electronics,** 2106 Waterby, Westlake Village, CA 91361. Tel: (805) 496-8877. |
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| CONNECTICUT | **Scientific Components,** 1185 S. Main St., Cheshire, CT 06410. Tel: (203) 272-2963 Twx: 710-455-2078 Fax: 203-271-3048. |
| FLORIDA | **Lawrence Associates,** 711 Turnbull Av., Altamonte Springs, FL 32701. Tel: (305) 339-3855 Fax: 305-767-0973.<br>**Lawrence Associates,** 5021 N. Dixie Highway, Boca Raton, FL 33431. Tel: (305) 368-7373 Fax: 305-394-5442.<br>**Lawrence Associates,** 1605 S. Missouri Ave., Clearwater, FL 33516. Tel: (813) 787-2773 Fax: 813-584-5865. |
| GEORGIA | **Electronic Marketing Associates, Inc. (EMA),** 6695 Peachtree Industrial Blvd., Suite 101, Atlanta, GA 30360. Tel: (404) 448-1215 Twx: 810-766-0483. |
| INDIANA | **Corrao Marsh, Inc.,** 6211 Stoney Creek Drive, Fort Wayne, IN 46825. Tel: (219) 482-2725 Twx: 910-333-8892 Fax: 219-484-7491.<br>**Corrao Marsh, Inc.,** 3117 West U.S. 40, Greenfield, IN 46140. Tel: (317) 462-4446. |
| ILLINOIS | **Micro Sales, Inc.,** 54 West Seegars Road, Arlington Heights, IL 60006. Tel: (312) 956-1000 Twx: 510-600-0756 Fax: 312-956-0189. |
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| MASSACHUSETTS | **Stone Components,** 2 Pierce Street, Framingham, MA 01701. Tel: (617) 875-3266 Twx: 310-374-6662 Fax: 617-875-0537. |
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MINNESOTA **Electronics Sales Agency,** 8053 Bloomington Freeway, Bloomington, MN 55420. Tel: (612) 884-8291 Fax: 612-884-8294.

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**Tai Corporation,** 12 S. Black Horse Pike, Bellmawr NJ 08031. Tel: (609) 933-2600 Fax: (609) 933-3329.

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